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- Extended Instructions
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- On-Chip Oscillator/Generator
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- Clocked Serial I/O Port
- Two 16-Bit Counter/Timers
- Two UARTs
- Clock Speeds: 6, 8, and 10 MHz
- 6-MHz version supports 6.144-MHz CPU Clock Operation
- Operating Range: 5V
- Operating Temperature Range: 0ºC to +70ºC
- Three Packaging Styles
  - 68-Pin PLCC
  - 64-Pin DIP
  - 80-Pin QFP

General Description

The Z80180™ is an 8-bit Microprocessor Unit (MPU) which provides the benefits of reduced system costs while also providing full backward compatibility with existing ZiLOG Z80 devices.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are wait-state generators, a clock oscillator, and an interrupt controller.

The Z80180 is housed in 80-pin QFP, 68-pin PLCC, and 64-pin DIP packages.

Note: All Signals with an overline are active Low. For example, B/$\overline{\text{W}}$, in which WORD is active Low); and $\overline{\text{B}}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions as shown in Table 1.

Table 1. Power Connection Conventions

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

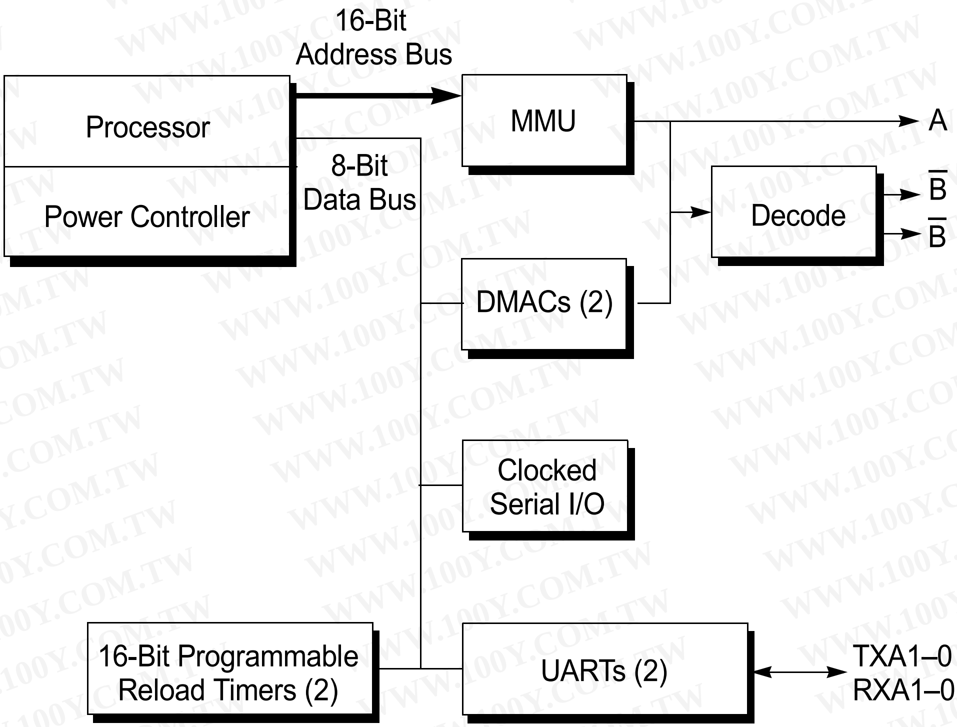


Figure 1. Z80180 Functional Block Diagram

Pin Configuration

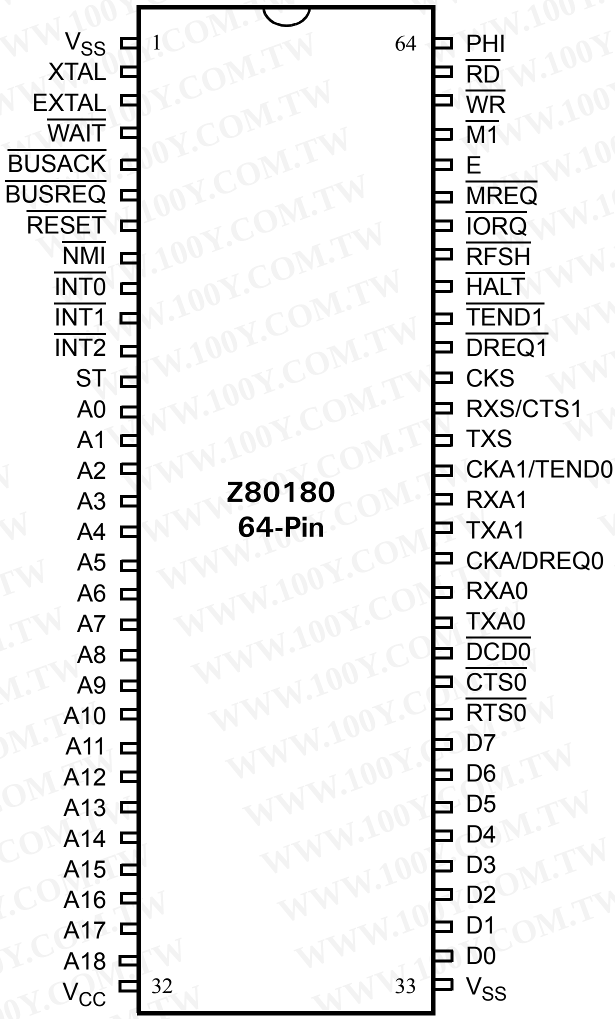


Figure 2. Z80180 64-Pin Dip Configuration

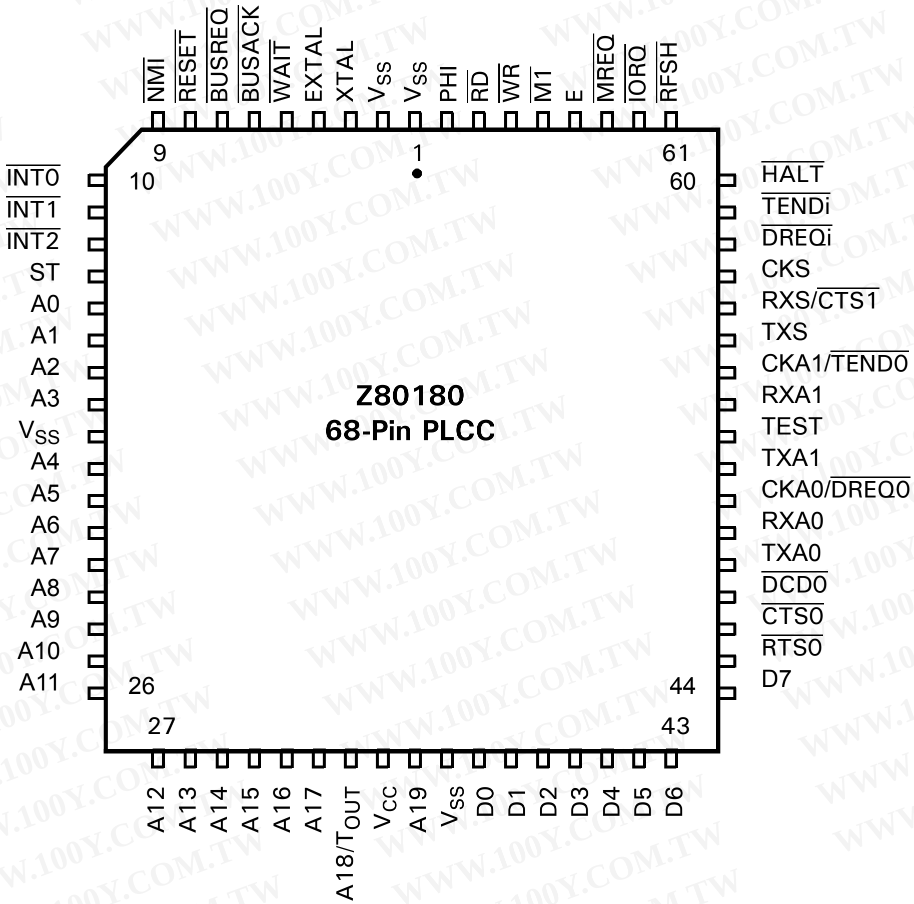


Figure 3. Z80180 68-Pin PLCC Configuration

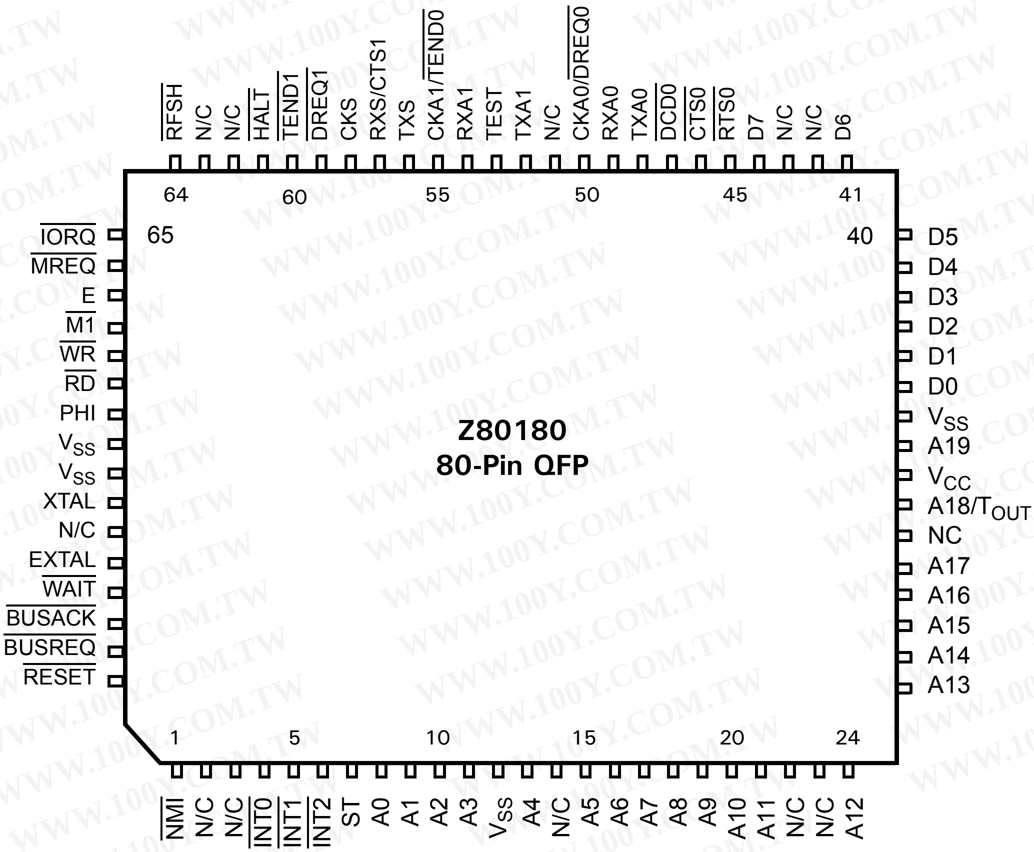


Figure 4. Z80180 80-Pin QFP Configuration

Table 2. Pin Status During RESET BUSACK and SLEEP

Pin Number and Package Type			Default Function	Secondary Function	Pin Status		
QFP	PLCC	DIP			RESET	BUSACK	SLEEP
1	9	8	$\overline{NMI}$		IN	IN	IN
2			NC				
3			NC				
4	10	9	$\overline{INT0}$		IN	IN	IN
5	11	10	$\overline{INT1}$		IN	IN	IN
6	12	11	$\overline{INT2}$		IN	IN	IN
7	13	12	ST		1	?	1
8	14	13	A0		3T	3T	1
9	15	14	A1		3T	3T	1
10	16	15	A2		3T	3T	1
11	17	16	A3		3T	3T	1
12	18		V_{SS}		GND	GND	GND
13	19	17	A4		3T	3T	1
14			NC				
15	20	18	A5		3T	3T	1
16	21	19	A6		3T	3T	1
17	22	20	A7		3T	3T	1
18	23	21	A8		3T	3T	1
19	24	22	A9		3T	3T	1
20	25	23	A10		3T	3T	1
21	26	24	A11		3T	3T	1
22			NC				
23			NC				
24	27	25	A12		3T	3T	1

Table 2. Pin Status During RESET BUSACK and SLEEP (continued)

Pin Number and Package Type			Default Function	Secondary Function	Pin Status		
QFP	PLCC	DIP			RESET	BUSACK	SLEEP
25	28	26	A13		3T	3T	1
26	29	27	A14		3T	3T	1
27	30	28	A15		3T	3T	1
28	31	29	A16		3T	3T	1
29	32	30	A17		3T	3T	1
30			NC				
31	33	31	A18	T_{OUT}	3T	3T	1
32	34	32	V_{CC}		V_{CC}	V_{CC}	V_{CC}
33	35		A19		3T	3T	1
34	36	33	V_{SS}		GND	GND	GND
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{RTS0}$		1	OUT	1
46	46	43	$\overline{CTS0}$		IN	OUT	IN
47	47	44	$\overline{DCD0}$		IN	IN	IN
48	48	45	TXA0		1	OUT	OUT
49	49	46	RXA0		IN	IN	IN

Table 2. Pin Status During RESET BUSACK and SLEEP (continued)

Pin Number and Package Type			Default	Secondary	Pin Status		
QFP	PLCC	DIP	Function	Function	RESET	BUSACK	SLEEP
50	50	47	CKA0	DREQ0	3T	OUT	OUT
51			NC				
52	51	48	TXA1		1	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1	TEND0	3T	IN	IN
56	55	51	TXS		1	OUT	OUT
57	56	52	RXS	CTS1	IN	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{\text{DREQ1}}$		IN	3T	IN
60	59	55	$\overline{\text{TEND1}}$		1	OUT	1
61	60	56	$\overline{\text{HALT}}$		1	1	0
62			NC				
63			NC				
64	61	57	$\overline{\text{RFSH}}$		1	OUT	OUT
65	62	58	$\overline{\text{IORQ}}$		1	3T	1
66	63	59	$\overline{\text{MREQ}}$		1	3T	1
67	64	60	E		0	OUT	OUT
68	65	61	$\overline{\text{M1}}$		1	1	1
69	66	62	$\overline{\text{WR}}$		1	3T	1
70	67	63	$\overline{\text{RD}}$		1	3T	1
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V_{SS}		GND	GND	GND
73	2		V_{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT

Table 2. Pin Status During RESET BUSACK and SLEEP (continued)

Pin Number and Package Type			Default Function	Secondary Function	Pin Status		
QFP	PLCC	DIP			RESET	BUSACK	SLEEP
75			NC				
76	4	3	EXTAL		IN	IN	IN
77	5	4	$\overline{\text{WAIT}}$		IN	IN	IN
78	6	5	$\overline{\text{BUSACK}}$		1	OUT	OUT
79	7	6	$\overline{\text{BUSREQ}}$		IN	IN	IN
80	8	7	$\overline{\text{RESET}}$		IN	IN	IN

Pin Descriptions

A0–A19. Address Bus (output, active High, 3-state). A_0–A_{19} form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges, up to 1 MB, and I/O data bus exchanges, up to 64 KB. The address bus enters a high-impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset) and address line A19 is not available in DIP versions of the Z80180.

$\overline{\text{BUSACK}}$. Bus Acknowledge (output, active Low). $\overline{\text{BUSACK}}$ indicates the requesting device, the MPU address and data bus, and some control signals that enter their high-impedance state.

$\overline{\text{BUSREQ}}$. Bus Request (input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request demands a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions and places address and data buses, and other control signals, into the high-impedance state.

CKA0, CKA1. Asynchronous Clock 0 and 1 (bidirectional, active High). When in output mode, these pins are the transmit and receive clock outputs from the ASCI baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCI baud rate generators. CKA0 is multiplexed with DREQ0, and CKA1 is multiplexed with TEND0.

CKS. Serial Clock (bidirectional, active High). This line is the clock for the CSIO channel.

CLOCK. System Clock (output, active High). The output is used as a reference clock for the MPU and the external system. The frequency of this output is equal to one-half that of the crystal or input clock frequency.

CTS0–CTS1. Clear to send 0 and 1 (inputs, active Low). These lines are modem control signals for the ASCI channels. CTS1 is multiplexed with RXS.

D0–D7. Data Bus (bidirectional, active High, 3-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

DCD0. Data Carrier Detect 0 (input, active Low). A programmable modem control signal for ASCI channel 0.

DREQ0, DREQ1. DMA Request 0 and 1 (input, active Low). DREQ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a READ or WRITE operation. These inputs can be programmed to be either level or edge sensed. DREQ0 is multiplexed with CKA0.

E. Enable Clock (output, active High). Synchronous machine cycle clock output during bus transactions.

EXTAL. External Clock Crystal (input, active High). Crystal oscillator connections. An external clock can be input to the Z80180 on this pin when a crystal is not used. This input is Schmitt-triggered.

$\overline{\text{HALT}}$. HALT/SLEEP (output, active Low). This output is asserted after the CPU executes either the HALT or SLEEP instruction, and is waiting for either nonmaskable or maskable interrupt before operation can resume. It is also used with the $\overline{\text{M1}}$ and ST signals to decode status of the CPU machine cycle.

$\overline{\text{INT0}}$. Maskable Interrupt Request 0 (input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$ and $\overline{\text{BUSREQ}}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ signals become active.

$\overline{\text{INT1}}$, **$\overline{\text{INT2}}$.** Maskable Interrupt Request 1 and 2 (inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$, $\overline{\text{BUSREQ}}$, and $\overline{\text{INT0}}$ signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{\text{INT0}}$, during this cycle neither the $\overline{\text{M1}}$ or $\overline{\text{IORQ}}$ signals become active.

$\overline{\text{IORQ}}$. I/O Request (output, active Low, 3-state). $\overline{\text{IORQ}}$ indicates that the address bus contains a valid I/O address for an I/O READ or I/O WRITE operation. $\overline{\text{IORQ}}$ is also generated, along with $\overline{\text{M1}}$, during the acknowledgment of the $\overline{\text{INT0}}$ input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the $\overline{\text{IOE}}$ signal of the Z64180.

$\overline{\text{M1}}$. Machine Cycle 1 (output, active Low). Together with $\overline{\text{MREQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is the op code fetch cycle of and instruction execution. Together with $\overline{IORQ}$, $\overline{M1}$ indicates that the current cycle is for an interrupt acknowledge. It is also used with the $\overline{HALT}$ and ST signal to decode status of the CPU machine cycle. This signal is analogous to the $\overline{LIR}$ signal of the Z64180.

$\overline{MREQ}$. Memory Request (output, active Low, 3-state). $\overline{MREQ}$ indicates that the address bus holds a valid address for a memory READ or memory WRITE operation. This signal is analogous to the $\overline{ME}$ signal of Z64180.

$\overline{NMI}$. Nonmaskable Interrupt (input, negative edge triggered). $\overline{NMI}$ demands a higher priority than $\overline{INT}$ and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location 0066h.

$\overline{RD}$. Op Code Reinitialized (output, active Low, 3-state). $\overline{RD}$ indicated that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

$\overline{RFSH}$. Refresh (output, active Low). Together with $\overline{MREQ}$, $\overline{RFSH}$ indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low order 8 bits of the address bus (A7–A10) contain the refresh address. This signal is analogous to the REF signal of the Z64180.

$\overline{RTS0}$. Request to Send 0 (output, active Low). A programmable modem control signal for ASCI channel 0.

RXA0, RXA1. Receive Data 0 and 1 (input, active High). These signals are the receive data to the ASCI channels.

RXS. Clocked Serial Receive Data (input, active High). This line is the receiver data for the CSIO channel. RXS is multiplexed with the CTS1 signal for ASCI channel 1.

ST. Status (output, active High). This signal is used with the $\overline{\text{M1}}$ and $\overline{\text{HALT}}$ output to decode the status of the CPU machine cycle.

Table 3. Status Summary

ST	$\overline{\text{HALT}}$	$\overline{\text{M1}}$	Operation
0	1	0	CPU Operation (1st op code fetch)
1	1	0	CPU Operation (2nd op code and 3rd op code fetch)
1	1	1	CPU Operation(MC except for op code fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (including SYSTEM STOP Mode)

Notes:
X = Reserved.
MC = Machine Cycle.

TEND0, TEND1. Transfer End 0 and 1 (outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{\text{TEND0}}$ is multiplexed with CKA1.

TEST. Test (output, not in DIP version). This pin is for test and should be left open.

TOUT. Timer Out (output, active High). T_{OUT} is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. Transmit Data 0 and 1 (outputs, active High). These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. Clocked Serial Transmit Data (output, active High). This line is the transmitted data from the CSIO channel.

$\overline{\text{WAIT}}$. Wait (input, active Low). $\overline{\text{WAIT}}$ indicated to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is sampled on the falling edge of T2 (and subsequent wait states). If the input is sampled Low, then the additional wait states are inserted until the $\overline{\text{WAIT}}$ input is sampled high, at which time execution continues.

$\overline{\text{WR}}$. WRITE (output, active Low, 3-state). $\overline{\text{WR}}$ indicated that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. Crystal (input, active High). Crystal oscillator connection. This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see DC Characteristics). Several pins are used for different conditions, depending on the circumstance.

Multiplexed Pin Descriptions

Table 4: Multiplexed Pin Descriptions

Pin	Description
A18/T_{OUT}	During RESET, this pin is initialized as A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, T_{OUT} function is selected. If TOC1 and TOC0 are cleared to 0, A18 function is selected.
CKA0/DREQ0	During RESET, this pin is initialized as CKA0 pin. If either DM1 or SM1 in DMA Mode Register (DMODE) is set to 1, $\overline{\text{DREQ0}}$ function is always selected.
CKA1/TEND0	During RESET, this pin is initialized as CKA1 pin. If CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, $\overline{\text{TEND0}}$ function is selected. If CKA1D bit is set to 0, CKA1 function is selected.

Table 4: Multiplexed Pin Descriptions (continued)

RXS/CTS1	During RESET, this pin is initialized as RXS pin. If CTS1E bit in ASCI status register ch1 (STAT1) is set to 1, $\overline{\text{CTS1}}$ function is selected. If CTS1E bit is set to 0, RXS function is selected.

Architecture

The Z180® combines a high-performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller, Interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four function blocks: direct memory access (DMA) control (2 channels), asynchronous serial communication interface (ASCI, 2 channels) programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSIO) channel.

Clock Generator. Generates system clock from an external crystal or clock input. The external clock is divided by two or one and provided to both internal and external devices.

Bus State Controller. This logic performs all of the status and bus control activity associated with both the CPU and some on-chip peripherals. Included are wait-state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

Interrupt Controller. This logic monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To maintain compatibility with the Z80® CPU, three different interrupts modes are supported.

Memory Management Unit. The MMU allows the user to *map* the memory used by the CPU (logically only 64 KB) into the 1-MB addressing range supported by the Z80180. The organization of the MMU object code allows maintenance compatibility with the Z80 CPU, while offering access to an extended memory space. This organization is achieved by using an effective *common area-banked area* scheme.

Central Processing Unit. The CPU is microcoded to provide a core that is object-code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiply. The core is modified to allow many of the instructions to execute in fewer clock cycles.

DMA Controller. The DMA controller provides high speed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory to/from I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1 MB address range with a block length up to 64 KB, and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASC). The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communication format as well as break detection and generation.

Programmable Reload Timers (PRT). This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

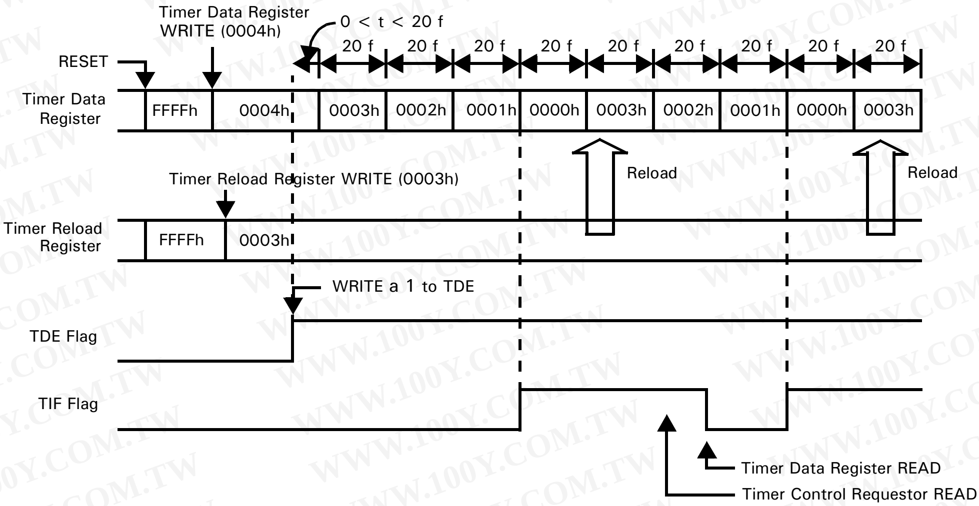


Figure 5. Timer Initialization, Count Down, and Reload Timing

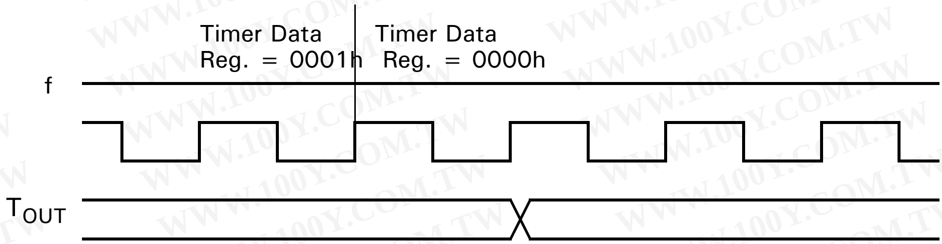


Figure 6. Timer Data Register

Clocked Serial I/O (CSIO). The CSIO channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSIO transmission and reception. The system design must ensure that the constraints of half-duplex operation are met. Transmit and Receive operations cannot occur simultaneously. For example, if a CSIO transmission is attempted while the CSIO is receiving data, a CSIO does not work.

Note: TRDR is not buffered. Attempting to perform a CSIO transmit while the previous transmit data is still being shifted out causes the shift data to be immediately updated, corrupting the transmit operation in progress. Reading TRDR while a transmit or receive is in progress should be avoided.

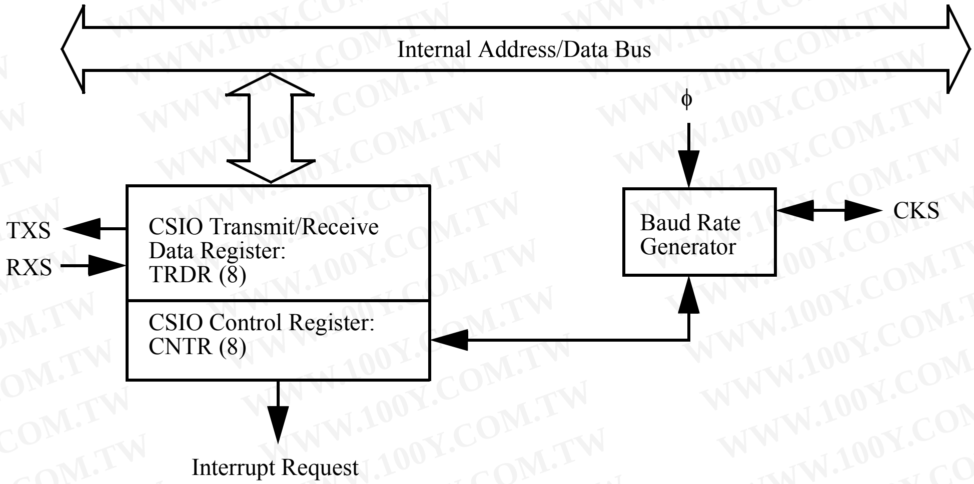


Figure 7. CSIO Block Diagram

Operation Modes

Z80® versus 64180 Compatibility

The Z80180 is descended from two different *ancestor* processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR), illustrated in Figure 8, can be programmed to select between certain Z80 and 64180 differences.

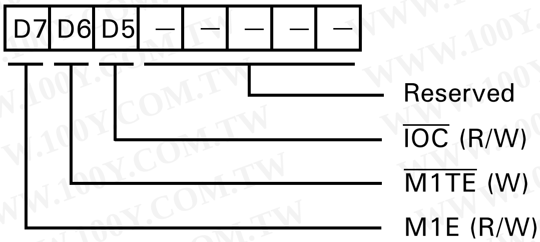


Figure 8. Operating Control Register (OMCR: I/O Address = 3Eh)

M1E (M1 Enable) This bit controls the M1 output and is set to a 1 during RESET.

When M1E = 1, the M1 output is asserted Low during the op code fetch cycle, the INT0 acknowledge cycle, and the first machine cycle of the NMI acknowledge.

On the Z80180, this choice makes the processor fetch a RETI instruction one time only, and when fetching a RETI from zero-wait-state memory uses three clock machine cycles, which are not fully Z80-timing compatible but are compatible with the on-chip CTCs.

When M1E = 0, the processor does not drive $\overline{\text{M1}}$ Low during instruction fetch cycles. After fetching a RETI instruction one time only, with normal timing, the processor goes back and refetches the instruction using fully Z80-compatible cycles that include driving $\overline{\text{M1}}$ Low. Some external Z80 peripherals may require properly decoded RETI instructions. Figure 9 illustrates the RETI sequence when M1E = 0.

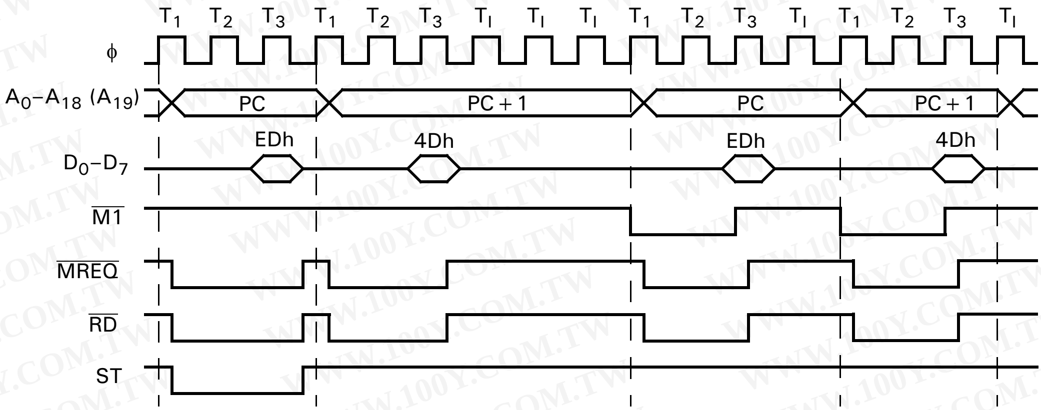


Figure 9. RETI Instruction Sequence with MIE = 0

M1TE (M1 Temporary Enable) This bit controls the temporary assertion of the $\overline{M1}$ signal. It is always read back as a 1 and is set to 1 during RESET.

When M1E is set to 0 to accommodate certain external Z80 peripheral(s), those same device(s) may require a pulse on M1 after programming certain of their registers to complete the function being programmed.

For example, when a control word is written to the Z80 PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{M1}$ signal. When $\overline{M1TE}$ = 1, there is no change in the operation of the $\overline{M1}$ signal and M1E controls its function. When $\overline{M1TE}$ = 0, the M1 output is asserted during the next op code fetch cycle regardless of the state programmed into the M1E bit. This instance is only momentary (one time only) and the user is not required to preprogram a 1 to disable the function (see Figure 10).

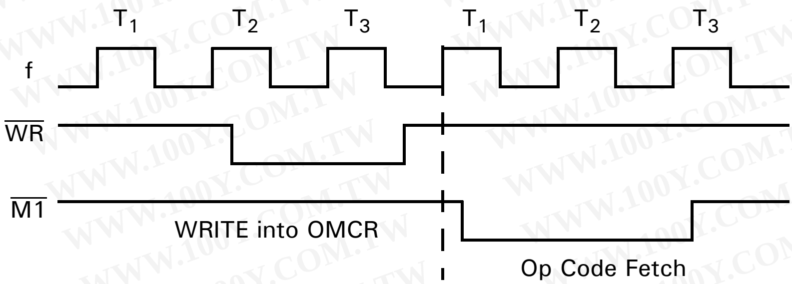


Figure 10. M1 Temporary Enable Timing

IOC This bit controls the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals. It is set to 1 by RESET. When $\overline{IOC}$ = 1, the $\overline{IORQ}$ and $\overline{RD}$ signals function the same as the Z64180 (Figure 11).

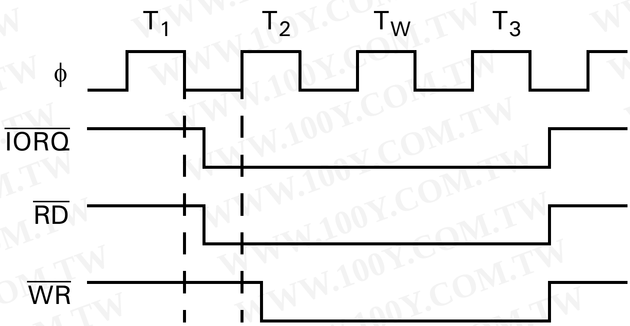


Figure 11. I/O READ and WRITE Cycles with $\overline{IOC}$ = 1

When $\overline{IOC}$ = 0, the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals match the timing of the Z80. The $\overline{IORQ}$ and $\overline{RD}$ signals go active as a result of the rising edge of T2. (Figure 12.)

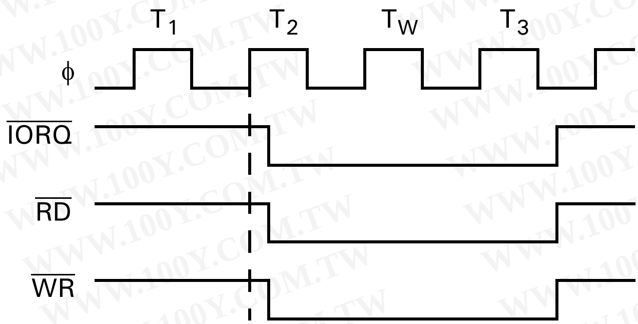


Figure 12. I/O READ and WRITE Cycles with $\overline{IOC}$ = 0

HALT and Low-Power Operating Modes. The Z80180 can operate in five modes with respect to activity and power consumption:

- Normal Operation
- HALT mode
- IOSTOP mode
- SLEEP mode
- SYSTEM STOP mode

Normal Operation. The Z80180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the $\overline{HALT}$ pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z80180 processor continually fetches the following op code but does not execute it, and drives the $\overline{HALT}$, ST and $\overline{M1}$ pins all Low. The oscillator and PHI pin remain active, interrupts and bus granting to external masters, and DRAM refresh can occur and all on-chip I/O devices continue to operate including the DMA channels.

The Z80180 leaves HALT mode in response to a Low on $\overline{\text{RESET}}$, on to an interrupt from an enabled on-chip source, an external request on $\overline{\text{NMI}}$, or an enabled external request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, or $\overline{\text{INT2}}$. In case of an interrupt, the return address is the instruction following the HALT instruction; at that point the program can either branch back to the HALT instruction to wait for another interrupt, or can examine the new state of the system/application and respond appropriately.

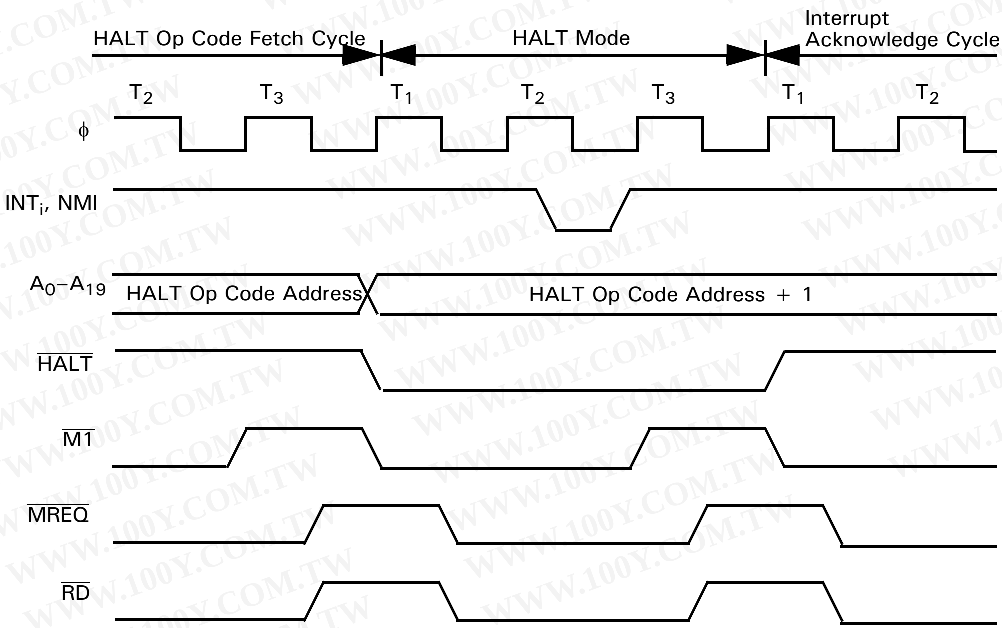


Figure 13. HALT Timing

SLEEP Mode Enter SLEEP mode by keeping the IOSTOP bit (ICR5) bits 3 and 6 of the CPU Control Register (CCR3, CCR6) all zero and executing the SLEEP instruction. The oscillator and PHI output continue operating, but are blocked from the CPU core and DMA channels to reduce power consumption. DRAM refresh stops but interrupts and granting to external master can occur. Except when the bus is granted to an external master, A19–0 and all control signals except $\overline{\text{HALT}}$ are maintained High. $\overline{\text{HALT}}$ is Low. I/O operations continue as before the SLEEP instruction, except for the DMA channels.

The Z80180 leaves SLEEP mode in response to a Low on $\overline{\text{RESET}}$, an interrupt request from an on-chip source, an external request on $\overline{\text{NMI}}$, or an external request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, or $\overline{\text{INT2}}$.

If an interrupt source is individually disabled, it cannot bring the Z80180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 1 so that interrupts are globally enabled (by an EI instruction), the highest priority active interrupt occurs, with the return address being the instruction after the SLEEP instruction. If an interrupt source is individually enabled, but the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z80180 leaves SLEEP mode by simply executing the following instruction(s).

This provides a technique for synchronization with high- speed external events without incurring the latency imposed by an interrupt response sequence. Figure 14 shows the timing for exiting SLEEP mode due to an interrupt request.

Note: The Z80180 takes about 1.5 clocks to restart.

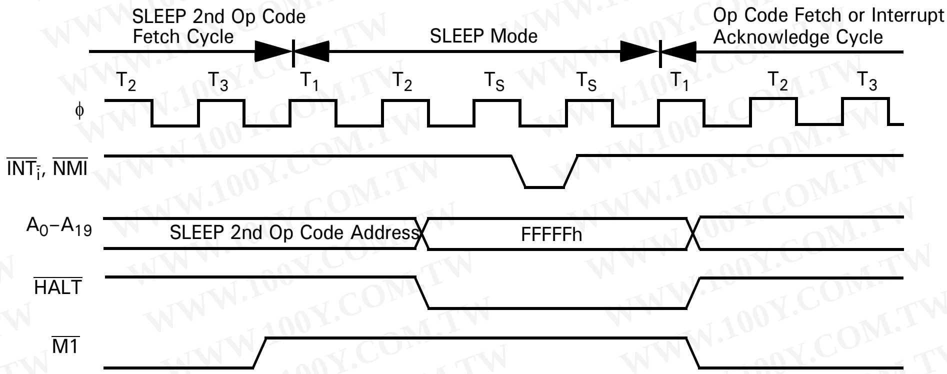


Figure 14. SLEEP Timing

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSIO, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLEEP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

Standard Test Conditions

The DC Characteristics section applies to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows in to the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points). The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. See Figure 15.

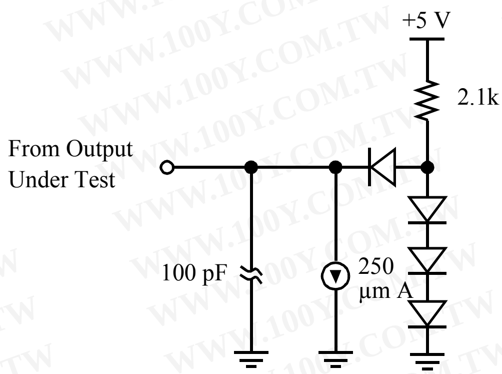


Figure 15. AC Load Capacitance Parameters

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 ~ +7.0	V
Input Voltage	V_{IN}	–0.3 ~ V_{CC} +0.3	V
Operating Temperature	T_{opr}	0 ~ 70	°C
Extended Temperature	T_{ext}	–40 ~ 85	°C
Storage Temperature	T_{stg}	–55 ~ +150	°C

Note: Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

DC Characteristics

Table 6. DC Characteristics

Sym.	Item	Condition	Min.	Typ.	Max.	Unit
V_{IH1}	Input *H* Voltage $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$		V_{CC} –0.6	–	V_{CC} +0.3	V
V_{IH2}	Input *H* Voltage Except $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$		2.0	–	V_{CC} +0.3	V

Note: *V_{IHmin} = V_{CC} –1.0V, V_{ILmax} = 0.8V (all output terminals are at no load); V_{CC} = 5.0V.
Note: V_{CC} = 5V + 10%, V_{SS} = 0V over specified temperature range, unless otherwise noted

Table 6. DC Characteristics (continued)

Sym.	Item	Condition	Min.	Typ.	Max.	Unit
V_{IL1}	Input *L* Voltage $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$		–0.3	–	0.6	V
V_{IL2}	Input *L* Voltage Except $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$		–0.3	–	0.8	V
V_{OH}	Outputs *H* Voltage All outputs	I_{OH} = –200µA	2.4	–	–	V
		I_{OH} = –20µA	V_{CC} –1.2	–	–	
V_{OL}	Outputs *L* Voltage All outputs	I_{OL} = –2.2µA	–	–	0.45	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	V_{IN} = 0.5 ~ V_{CC} –0.5	–	–	1.0	µA
I_{TL}	Three State Leakage Current	V_{IN} = 0.5 ~ V_{CC} –0.5	–	–	1.0	µA
I_{CC}*	Power Dissipation* (Normal Operation)	F = 6 MHz	–	15	40	MA
		F = 8 MHz	–	20	50	
		F = 10 MHz**	–	25	60	
	Power Dissipation* (SYSTEM STOP mode)	F = 6 MHz	–	3.8	12.5	
		F = 8 MHz	–	5	15	
		F = 10 MHz**	–	6.3	17.5	
C_P	Pin Capacitance	$V_{IN}V_{in}$ = 0V, ϕ = 1 MHzT_A = 25° C	–	–	12	pF

Note: *V_{IHmin} = V_{CC} –1.0V, V_{ILmax} = 0.8V (all output terminals are at no load); V_{CC} = 5.0V.
Note: V_{CC} = 5V + 10%, V_{SS} = 0V over specified temperature range, unless otherwise noted

AC Characteristics

Tables 7, 8, and 9 provide AC characteristics for the Z80180-6, Z80180-8, and Z80180-10 respectively. V_{CC} = 5V + 10%, V_{SS} = 0V, T_A – 0°C to +70°C, unless otherwise noted.

Table 7. Z80180-6 AC Characteristics

No.	Symbol	Item	Z80180-6 Min.	Z80180-6 Max.	Unit
1	t_{cyc}	Clock Cycle Time	162	2000	ns
2	t_{CHW}	Clock *H* Pulse Width	65	–	ns
3	t_{CLW}	Clock *L* Pulse Width	65	–	ns
4	t_{cf}	Clock Fall Time	–	15	ns
5	t_{cr}	Clock Rise Time	–	15	ns
6	t_{AD}	ØRise to Address Valid Delay	–	90	ns
7	t_{AS}	Address Valid to $\overline{MREQ}$ Fall or $\overline{IORQ}$ Fall)	30	–	ns
8	t_{MED1}	Ø Fall to $\overline{MREQ}$ Fall Delay	–	60	ns
9	t_{RDD1}	Ø Fall to $\overline{RD}$ Fall Delay $\overline{IOC}$ = 1	–	60	ns
		Ø Rise to $\overline{RD}$ Rise Delay $\overline{IOC}$ = 0	–	65	
10	t_{M1D1}	Ø Rise to $\overline{M1}$ Fall Delay	–	80	ns
11	t_{AH}	Address Hold Time from ($\overline{MREQ}$, $\overline{IOREQ}$, $\overline{RD}$, $\overline{WR}$)	35	–	ns
12	t_{MED2}	Ø Fall to $\overline{MREQ}$ Rise Delay	–	60	ns
13	t_{RDD2}	Ø Fall to $\overline{RD}$ Rise Delay	–	60	ns
14	t_{M1D2}	Ø Rise to $\overline{M1}$ Rise Delay	–	80	ns
15	t_{DRS}	Data Read Set-up Time	40	–	ns
16	t_{DRH}	Data Read Hold Time	0	–	ns
17	t_{STD1}	Ø Fall to ST Fall Delay	–	90	ns
18	t_{STD2}	Ø Fall to ST Rise Delay	–	90	ns
19	t_{WS}	$\overline{WAIT}$ Set-up Time to Ø Fall	40	–	ns
20	t_{WH}	$\overline{WAIT}$ Hold Time from Ø Fall	40	–	ns

Table 7. Z80180-6 AC Characteristics (continued)

			Z80180-6		
No.	**Symbol**	**Item**	**Min.**	**Max.**	**Unit**
21	t_{WDZ}	Ø Rise to Data Float Delay	–	95	ns
22	t_{WRD1}	Ø Rise to $\overline{WR}$ Fall Delay	–	65	ns
23	t_{WDD}	Ø Fall to WRITE Data Delay Time	–	90	ns
24	t_{WDS}	WRITE Data Set-up Time to $\overline{WR}$ Fall	40	–	ns
25	t_{WRD2}	Ø Fall to $\overline{WR}$ Rise Delay	–	80	ns
26	t_{WRP}	$\overline{WR}$ Pulse Width	170	–	ns
26a		$\overline{WR}$ Pulse Width (I/O WRITE Cycle)	332	–	ns
27	t_{WDH}	WRITE Data Hold Time from ($\overline{WR}$ Rise)	40	–	
28	t_{IOD1}	Ø Fall to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 1	–	60	ns
		Ø Rise to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 1	–	65	
29	t_{IOD2}	Ø Fall to $\overline{IORQ}$ Rise Delay	–	60	ns
30	t_{IOD3}	$\overline{M1}$ Fall to $\overline{IORQ}$Fall Delay	340	–	ns
31	t_{INTS}	$\overline{INT}$ Set-up Time to Ø Fall	40	–	ns
32	t_{INTS}	$\overline{INT}$ Hold Time from Ø Fall	40	–	ns
33	t_{NMIW}	$\overline{NMI}$ Pulse Width	120	–	ns
34	t_{BRS}	$\overline{BUSREQ}$ Set-up Time to Ø Fall	40	–	ns
35	t_{BRH}	$\overline{BUSREQ}$ Hold Time from Ø Fall	40	–	ns
36	t_{BAD1}	Ø Rise to $\overline{BUSACK}$ Fall Delay	–	95	ns
37	t_{BAD2}	Ø Fall to $\overline{BUSACK}$ Rise Delay	–	90	ns
38	t_{BZD}	Ø Rise to Bus Floating Delay Time	–	125	ns
39	t_{MEWH}	$\overline{MREQ}$ Pulse Width (High)	110	–	ns
40	t_{MEWL}	$\overline{MREQ}$ Pulse Width (Low)	125	–	ns
41	t_{RFD1}	Ø Rise to $\overline{RFSH}$ Fall Delay	–	90	ns
42	t_{RFD2}	Ø Rise to $\overline{RFSH}$Rise Delay	–	90	ns
43	t_{HAD1}	Ø Rise to $\overline{HALT}$ Fall Delay	–	90	ns
44	t_{HAD2}	Ø Rise to $\overline{HALT}$Rise Delay	–	90	ns
45	t_{DRQS}	/DREQi Set-up Time to Ø Rise	40	–	ns
46	t_{DRQH}	/DREQi Hold Time from Ø Rise	40	–	ns

Table 7. Z80180-6 AC Characteristics (continued)

No.	Symbol	Item	Z80180-6 Min.	Max.	Unit
47	t_{TED1}	Ø Fall to $\overline{\text{TENDi}}$ Fall Delay	–	70	ns
48	t_{TED2}	Ø Fall to $\overline{\text{TENDi}}$Rise Delay	–	70	ns
49	t_{ED1}	Ø Rise to E Rise Delay	–	95	ns
50	t_{ED2}	Ø Fall or Rise to E Fall Delay	–	95	ns
51	P_{WEH}	E Pulse Width (High)	75	–	ns
52	P_{WEL}	E Pulse Width (Low)	180	–	ns
53	t_{Er}	Enable Rise Time	–	20	ns
54	t_{Ef}	Enable Fall Time	–	20	ns
55	t_{TOD}	Ø Fall to Timer Output Delay	–	300	ns
56	t_{STDI}	CSIO Transmit Data Delay Time (Internal Clock Operation)	–	200	ns
57	t_{STDE}	CSIO Transmit Data Delay Time (External Clock Operation)	–	7.5tcyc +300	ns
58	t_{SRSI}	CSIO Receive Data Set-up Time (Internal Clock Operation)	1	–	tcyc
59	t_{SRHI}	CSIO Receive Data Hold Time (Internal Clock Operation)	1	–	tcyc
60	t_{SRSE}	CSIO Receive Data Set-up Time (External Clock Operation)	1	–	tcyc
61	t_{SRHE}	CSIO Receive Data Hold Time (External Clock Operation)	1	–	tcyc
62	t_{RES}	$\overline{\text{RESET}}$ Set-up Time to Ø Fall	120	–	ns
63	t_{REH}	$\overline{\text{RESET}}$ Hold Time from Ø Fall	80	–	ns
64	t_{OSC}	Oscillator Stabilization Time	–	20	ns
65	t_{EXr}	External Clock Rise Time (EXTAL)	–	25	ns
66	t_{EXf}	External Clock Fall Time (EXTAL)	–	25	ns
67	t_{Rr}	$\overline{\text{RESET}}$ Rise Time	–	50	ns
68	t_{Rf}	$\overline{\text{RESET}}$ Fall Time	–	50	ns

Table 7. Z80180-6 AC Characteristics (continued)

			Z80180-6		
No.	Symbol	Item	Min.	Max.	Unit
69	t_{Ir}	Input Rise Time (except EXTAL, $\overline{\text{RESET}}$)	–	100	ns
70	t_{If}	Input Fall Time (except EXTAL, $\overline{\text{RESET}}$)	–	100	ns

Table 8. Z80180-8 AC Characteristics

			Z80180-8		
No.	Symbol	Item	Min.	Max.	Unit
1	t_{cyc}	Clock Cycle Time	125	2000	ns
2	t_{CHW}	Clock *H* Pulse Width	50	–	ns
3	t_{CLW}	Clock *L* Pulse Width	50	–	ns
4	t_{cf}	Clock Fall Time	–	15	ns
5	t_{cr}	Clock Rise Time	–	15	ns
6	t_{AD}	ØRise to Address Valid Delay	–	80	ns
7	t_{AS}	Address Valid to $\overline{\text{MREQ}}$ Fall or $\overline{\text{IORQ}}$ Fall)	20	–	ns
8	t_{MED1}	Ø Fall to $\overline{\text{MREQ}}$ Fall Delay	–	50	ns
9	t_{RDD1}	Ø Fall to $\overline{\text{RD}}$ Fall Delay $\overline{\text{IOC}}$ = 1	–	50	ns
		Ø Rise to $\overline{\text{RD}}$ Rise Delay $\overline{\text{IOC}}$ = 0	–	60	
10	t_{M1D1}	Ø Rise to $\overline{\text{M1}}$ Fall Delay	–	70	ns
11	t_{AH}	Address Hold Time from ($\overline{\text{MREQ}}$, $\overline{\text{IOREQ}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$)	20	–	ns
12	t_{MED2}	Ø Fall to $\overline{\text{MREQ}}$ Rise Delay	–	50	ns
13	t_{RDD2}	Ø Fall to $\overline{\text{RD}}$ Rise Delay	–	50	ns

Table 8. Z80180-8 AC Characteristics (continued)

			Z80180-8		
No.	**Symbol**	**Item**	**Min.**	**Max.**	**Unit**
14	t_{M1D2}	Ø Rise to $\overline{\text{M1}}$ Rise Delay	–	70*	ns
15	t_{DRS}	Data Read Set-up Time	30	–	ns
16	t_{DRH}	Data Read Hold Time	0	–	ns
17	t_{STD1}	Ø Fall to ST Fall Delay	–	70	ns
18	t_{STD2}	Ø Fall to ST Rise Delay	–	70	ns
19	t_{WS}	$\overline{\text{WAIT}}$ Set-up Time to Ø Fall	40	–	ns
20	t_{WH}	$\overline{\text{WAIT}}$ Hold Time from Ø Fall	40	–	ns
21	t_{WDZ}	Ø Rise to Data Float Delay	–	70	ns
22	t_{WRD1}	Ø Rise to $\overline{\text{WR}}$ Fall Delay	–	60	ns
23	t_{WDD}	Ø Fall to WRITE Data Delay Time	–	80	ns
24	t_{WDS}	WRITE Data Set-up Time to $\overline{\text{WR}}$ Fall	20	–	ns
25	t_{WRD2}	Ø Fall to $\overline{\text{WR}}$ Rise Delay	–	60	ns
26	t_{WRP}	$\overline{\text{WR}}$ Pulse Width	130	–	ns
26a		$\overline{\text{WR}}$ Pulse Width (I/O WRITE Cycle)	255	–	ns
27	t_{WDH}	WRITE Data Hold Time from ($\overline{\text{WR}}$ Rise)	15	–	
28	t_{IOD1}	Ø Fall to $\overline{\text{IORQ}}$ Fall Delay $\overline{\text{IOC}}$ = 1	–	50	ns
		Ø Rise to $\overline{\text{IORQ}}$ Fall Delay $\overline{\text{IOC}}$ = 1	–	60	
29	t_{IOD2}	Ø Fall to $\overline{\text{IORQ}}$ Rise Delay	–	50	ns
30	t_{IOD3}	$\overline{\text{M1}}$ Fall to $\overline{\text{IORQ}}$Fall Delay	250	–	ns
31	t_{INTS}	$\overline{\text{INT}}$ Set-up Time to Ø Fall	40	–	ns
32	t_{INTS}	$\overline{\text{INT}}$ Hold Time from Ø Fall	40	–	ns

Table 8. Z80180-8 AC Characteristics (continued)

No.	Symbol	Item	Z80180-8 Min.	Z80180-8 Max.	Unit
33	t_{NMIW}	$\overline{\text{NMI}}$ Pulse Width	100	–	ns
34	t_{BRS}	$\overline{\text{BUSREQ}}$ Set-up Time to Ø Fall	40	–	ns
35	t_{BRH}	$\overline{\text{BUSREQ}}$ Hold Time from Ø Fall	40		ns
36	t_{BAD1}	Ø Rise to $\overline{\text{BUSACK}}$ Fall Delay	–	70	ns
37	t_{BAD2}	Ø Fall to $\overline{\text{BUSACK}}$ Rise Delay	–	70	ns
38	t_{BZD}	Ø Rise to Bus Floating Delay Time	–	90	ns
39	t_{MEWH}	$\overline{\text{MREQ}}$ Pulse Width (High)	90	–	ns
40	t_{MEWL}	$\overline{\text{MREQ}}$ Pulse Width (Low)	100	–	ns
41	t_{RFD1}	Ø Rise to $\overline{\text{RFSH}}$ Fall Delay	–	80	ns
42	t_{RFD2}	Ø Rise to $\overline{\text{RFSH}}$Rise Delay	–	80	ns
43	t_{HAD1}	Ø Rise to $\overline{\text{HALT}}$ Fall Delay	–	80	ns
44	t_{HAD2}	Ø Rise to $\overline{\text{HALT}}$Rise Delay	–	80	ns
45	t_{DRQS}	/DREQi Set-up Time to Ø Rise	40	–	ns
46	t_{DRQH}	/DREQi Hold Time from Ø Rise	40	–	ns
47	t_{TED1}	Ø Fall to $\overline{\text{TENDi}}$ Fall Delay	–	60	ns
48	t_{TED2}	Ø Fall to $\overline{\text{TENDi}}$Rise Delay	–	60	ns
49	t_{ED1}	Ø Rise to E Rise Delay	–	70	ns
50	t_{ED2}	Ø Fall or Rise to E Fall Delay	–	70	ns
51	P_{WEH}	E Pulse Width (High)	65	–	ns
52	P_{WEL}	E Pulse Width (Low)	130	–	ns
53	t_{Er}	Enable Rise Time	–	20	ns

Table 8. Z80180-8 AC Characteristics (continued)

No.	Symbol	Item	Z80180-8 Min.	Z80180-8 Max.	Unit
54	t_{Ef}	Enable Fall Time	–	20	ns
55	t_{TOD}	Ø Fall to Timer Output Delay	–	200	ns
56	t_{STDI}	CSIO Transmit Data Delay Time (Internal Clock Operation)	–	200	ns
57	t_{STDE}	CSIO Transmit Data Delay Time (External Clock Operation)	–	7.5tcyc +200	ns
58	t_{SRSI}	CSIO Receive Data Set-up Time (Internal Clock Operation)	1	–	tcyc
59	t_{SRHI}	CSIO Receive Data Hold Time (Internal Clock Operation)	1	–	tcyc
60	t_{SRSE}	CSIO Receive Data Set-up Time (External Clock Operation)	1	–	tcyc
61	t_{SRHE}	CSIO Receive Data Hold Time (External Clock Operation)	1	–	tcyc
62	t_{RES}	$\overline{\text{RESET}}$ Set-up Time to Ø Fall	100	–	ns
63	t_{REH}	$\overline{\text{RESET}}$ Hold Time from Ø Fall	70	–	ns
64	t_{OSC}	Oscillator Stabilization Time	–	20	ns
65	t_{EXr}	External Clock Rise Time (EXTAL)	–	25	ns
66	t_{EXf}	External Clock Fall Time (EXTAL)	–	25	ns
67	t_{Rr}	$\overline{\text{RESET}}$ Rise Time	–	50	ns
68	t_{Rf}	$\overline{\text{RESET}}$ Fall Time	–	50	ns
69	t_{Ir}	Input Rise Time (except EXTAL, $\overline{\text{RESET}}$)	–	100	ns

Table 8. Z80180-8 AC Characteristics (continued)

			Z80180-8		
No.	**Symbol**	**Item**	**Min.**	**Max.**	**Unit**
70	t_{If}	Input Fall Time (except EXTAL, $\overline{\text{RESET}}$)	–	100	ns

Table 9. Z80180-10 AC Characteristics

			Z80180-10		
No.	**Symbol**	**Item**	**Min.**	**Max.**	**Unit**
1	t_{cyc}	Clock Cycle Time	100	2000	ns
2	t_{CHW}	Clock *H* Pulse Width	40	–	ns
3	t_{CLW}	Clock *L* Pulse Width	40	–	ns
4	t_{cf}	Clock Fall Time	–	10	ns
5	t_{cr}	Clock Rise Time	–	10	ns
6	t_{AD}	ØRise to Address Valid Delay	–	70	ns
7	t_{AS}	Address Valid to $\overline{\text{MREQ}}$ Fall or $\overline{\text{IORQ}}$ Fall)	10	–	ns
8	t_{MED1}	Ø Fall to $\overline{\text{MREQ}}$ Fall Delay	–	50	ns
9	t_{RDD1}	Ø Fall to $\overline{\text{RD}}$ Fall Delay $\overline{\text{IOC}}$ = 1	–	50	ns
		Ø Rise to $\overline{\text{RD}}$ Rise Delay $\overline{\text{IOC}}$ = 0	–	55	
10	t_{M1D1}	Ø Rise to $\overline{\text{M1}}$ Fall Delay	–	60	ns
11	t_{AH}	Address Hold Time from ($\overline{\text{MREQ}}$, $\overline{\text{IOREQ}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$)	10	–	ns
12	t_{MED2}	Ø Fall to $\overline{\text{MREQ}}$ Rise Delay	–	50	ns
13	t_{RDD2}	Ø Fall to $\overline{\text{RD}}$ Rise Delay	–	50	ns

Table 9. Z80180-10 AC Characteristics (continued)

			Z80180-10		
No.	**Symbol**	**Item**	**Min.**	**Max.**	**Unit**
14	t_{M1D2}	Ø Rise to $\overline{\text{M1}}$ Rise Delay	–	60	ns
15	t_{DRS}	Data Read Set-up Time	25	–	ns
16	t_{DRH}	Data Read Hold Time	0	–	ns
17	t_{STD1}	Ø Fall to ST Fall Delay	–	60	ns
18	t_{STD2}	Ø Fall to ST Rise Delay	–	60	ns
19	t_{WS}	$\overline{\text{WAIT}}$ Set-up Time to Ø Fall	30	–	ns
20	t_{WH}	$\overline{\text{WAIT}}$ Hold Time from Ø Fall	30	–	ns
21	t_{WDZ}	Ø Rise to Data Float Delay	–	60	ns
22	t_{WRD1}	Ø Rise to $\overline{\text{WR}}$ Fall Delay	–	50	ns
23	t_{WDD}	Ø Fall to WRITE Data Delay Time	–	60	ns
24	t_{WDS}	WRITE Data Set-up Time to $\overline{\text{WR}}$ Fall	15	–	ns
25	t_{WRD2}	Ø Fall to $\overline{\text{WR}}$ Rise Delay	–	50	ns
26	t_{WRP}	$\overline{\text{WR}}$ Pulse Width	110	–	ns
26a		$\overline{\text{WR}}$ Pulse Width (I/O WRITE Cycle)	210	–	ns
27	t_{WDH}	WRITE Data Hold Time from ($\overline{\text{WR}}$ Rise)	10	–	
28	t_{IOD1}	Ø Fall to $\overline{\text{IORQ}}$ Fall Delay $\overline{\text{IOC}}$ = 1	–	50	ns
		Ø Rise to $\overline{\text{IORQ}}$ Fall Delay $\overline{\text{IOC}}$ = 1	–	55	
29	t_{IOD2}	Ø Fall to $\overline{\text{IORQ}}$ Rise Delay	–	50	ns
30	t_{IOD3}	$\overline{\text{M1}}$ Fall to $\overline{\text{IORQ}}$Fall Delay	200	–	ns
31	t_{INTS}	$\overline{\text{INT}}$ Set-up Time to Ø Fall	30	–	ns
32	t_{INTS}	$\overline{\text{INT}}$ Hold Time from Ø Fall	30	–	ns

Table 9. Z80180-10 AC Characteristics (continued)

			Z80180-10		
No.	**Symbol**	**Item**	**Min.**	**Max.**	**Unit**
33	t_{NMIW}	$\overline{\text{NMI}}$ Pulse Width	80	–	ns
34	t_{BRS}	$\overline{\text{BUSREQ}}$ Set-up Time to Ø Fall	30	–	ns
35	t_{BRH}	$\overline{\text{BUSREQ}}$ Hold Time from Ø Fall	30		ns
36	t_{BAD1}	Ø Rise to $\overline{\text{BUSACK}}$ Fall Delay	–	60	ns
37	t_{BAD2}	Ø Fall to $\overline{\text{BUSACK}}$ Rise Delay	–	60	ns
38	t_{BZD}	Ø Rise to Bus Floating Delay Time	–	80	ns
39	t_{MEWH}	$\overline{\text{MREQ}}$ Pulse Width (High)	70	–	ns
40	t_{MEWL}	$\overline{\text{MREQ}}$ Pulse Width (Low)	80	–	ns
41	t_{RFD1}	Ø Rise to $\overline{\text{RFSH}}$ Fall Delay	–	60	ns
42	t_{RFD2}	Ø Rise to $\overline{\text{RFSH}}$Rise Delay	–	60	ns
43	t_{HAD1}	Ø Rise to $\overline{\text{HALT}}$ Fall Delay	–	50	ns
44	t_{HAD2}	Ø Rise to $\overline{\text{HALT}}$Rise Delay	–	50	ns
45	t_{DRQS}	/DREQi Set-up Time to Ø Rise	30	–	ns
46	t_{DRQH}	/DREQi Hold Time from Ø Rise	30	–	ns
47	t_{TED1}	Ø Fall to $\overline{\text{TENDi}}$ Fall Delay	–	50	ns
48	t_{TED2}	Ø Fall to $\overline{\text{TENDi}}$Rise Delay	–	50	ns
49	t_{ED1}	Ø Rise to E Rise Delay	–	60	ns
50	t_{ED2}	Ø Fall or Rise to E Fall Delay	–	60	ns
51	P_{WEH}	E Pulse Width (High)	55	–	ns
52	P_{WEL}	E Pulse Width (Low)	110	–	ns
53	t_{Er}	Enable Rise Time	–	20	ns

Table 9. Z80180-10 AC Characteristics (continued)

			Z80180-10		
No.	**Symbol**	**Item**	**Min.**	**Max.**	**Unit**
54	t_{Ef}	Enable Fall Time	–	20	ns
55	t_{TOD}	Ø Fall to Timer Output Delay	–	150	ns
56	t_{STDI}	CSIO Transmit Data Delay Time (Internal Clock Operation)	–	150	ns
57	t_{STDE}	CSIO Transmit Data Delay Time (External Clock Operation)	–	7.5tcyc +150	ns
58	t_{SRSI}	CSIO Receive Data Set-up Time (Internal Clock Operation)	1	–	tcyc
59	t_{SRHI}	CSIO Receive Data Hold Time (Internal Clock Operation)	1	–	tcyc
60	t_{SRSE}	CSIO Receive Data Set-up Time (External Clock Operation)	1	–	tcyc
61	t_{SRHE}	CSIO Receive Data Hold Time (External Clock Operation)	1	–	tcyc
62	t_{RES}	$\overline{\text{RESET}}$ Set-up Time to Ø Fall	80	–	ns
63	t_{REH}	$\overline{\text{RESET}}$ Hold Time from Ø Fall	50	–	ns
64	t_{OSC}	Oscillator Stabilization Time	–	TBD	ns
65	t_{EXr}	External Clock Rise Time (EXTAL)	–	25	ns
66	t_{EXf}	External Clock Fall Time (EXTAL)	–	25	ns
67	t_{Rr}	$\overline{\text{RESET}}$ Rise Time	–	50	ns
68	t_{Rf}	$\overline{\text{RESET}}$ Fall Time	–	50	ns
69	t_{Ir}	Input Rise Time (except EXTAL, $\overline{\text{RESET}}$)	–	100	ns

Table 9. Z80180-10 AC Characteristics (continued)

			Z80180-10		
No.	Symbol	Item	Min.	Max.	Unit
70	t_{If}	Input Fall Time (except EXTAL, $\overline{RESET}$)	–	100	ns

Timing Diagrams

Z80180 Timing signals are shown in Figure 16 through Figure 27.

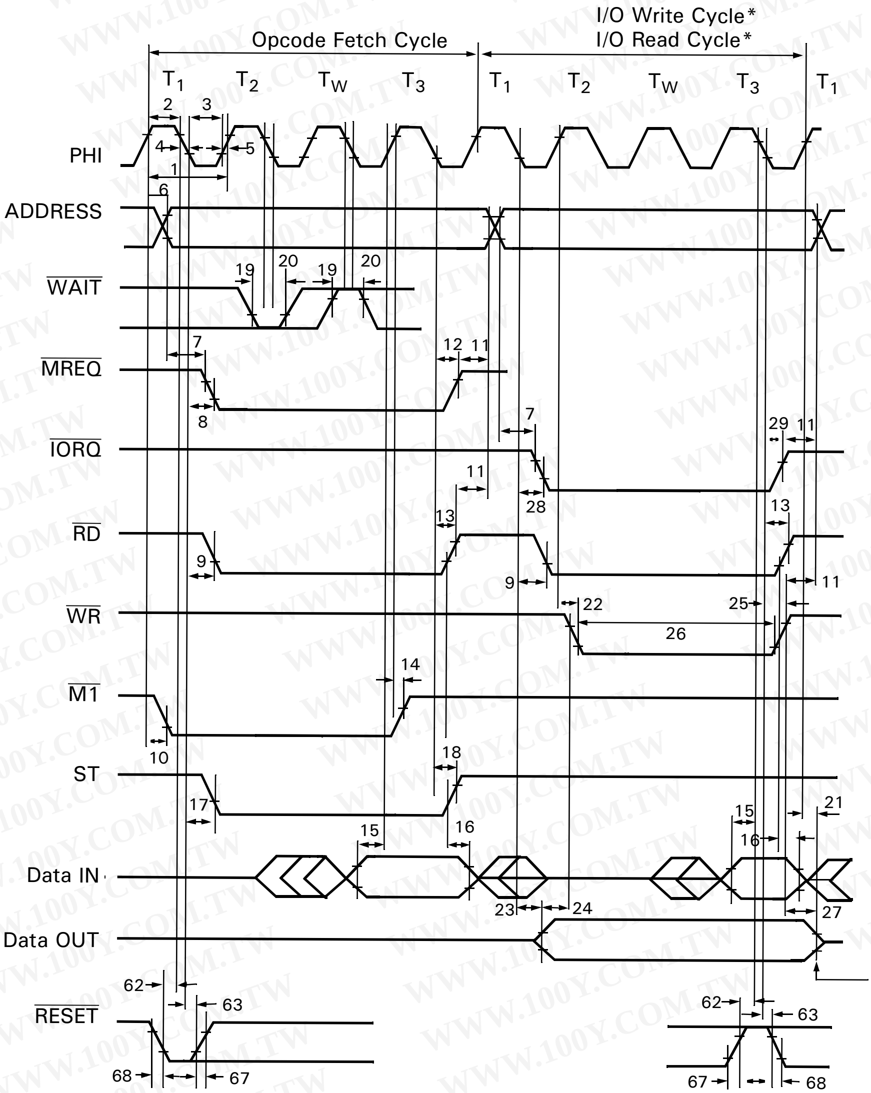


Figure 16. CPU Timing (Op Code Fetch, I/O WRITE, and I/O READ Cycles)

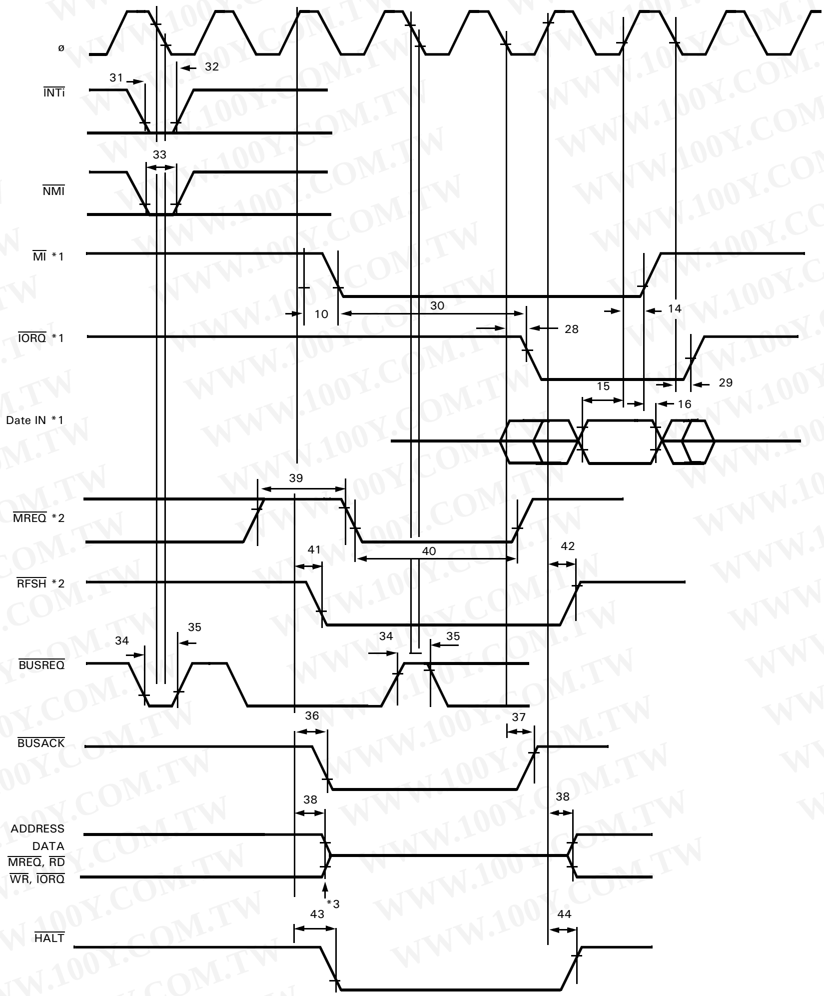


Figure 17. CPU Timing ($\overline{\text{INT0}}$ Acknowledge Cycle, Refresh Cycle)

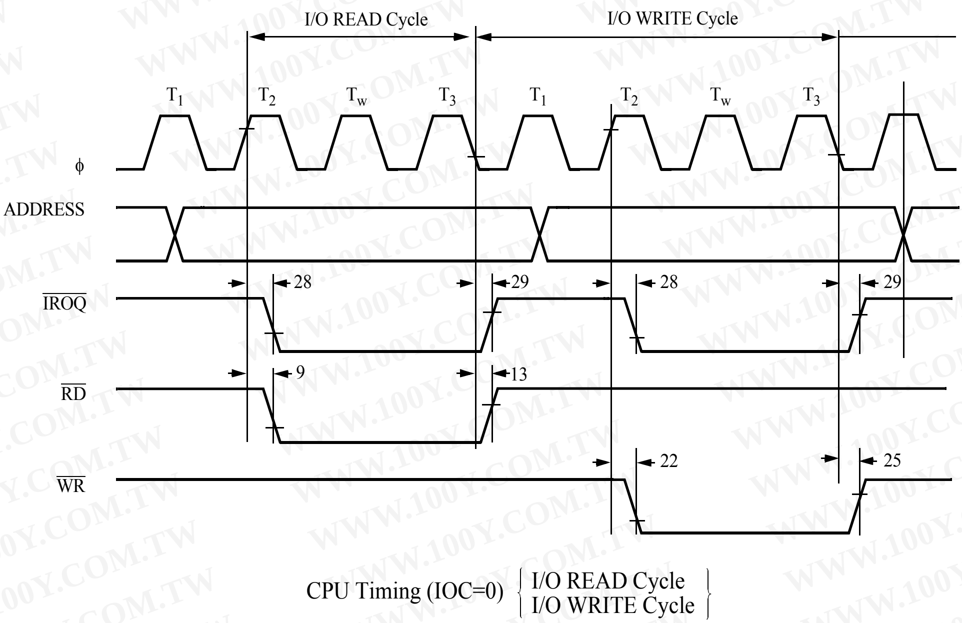
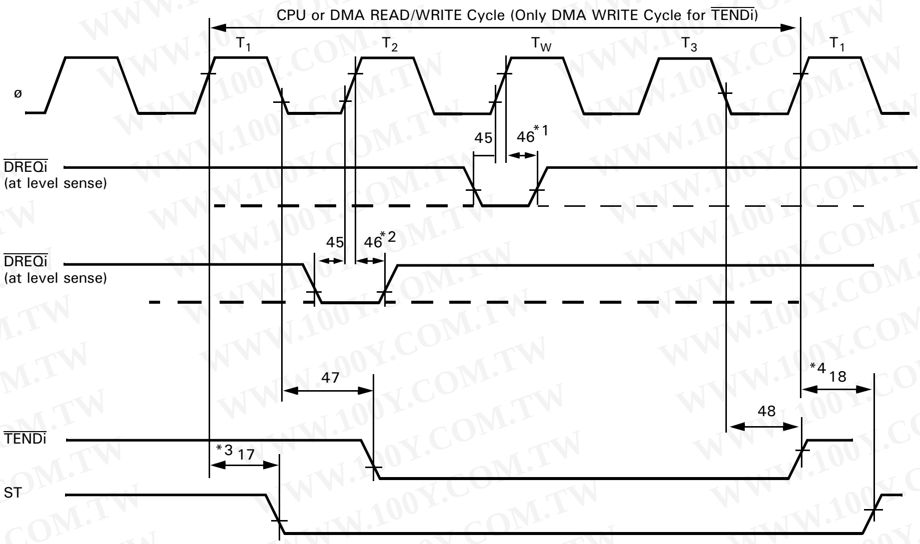


Figure 18. CPU Timing ($\overline{IOC}$ = 0) (I/O READ Cycle, I/O WRITE Cycle)



Notes:

1. t_{DRQS} and t_{DHQH} are specified for the rising edge of clock followed by T_3.
2. t_{DRQS} and t_{DHQH} are specified for the rising edge of clock.
3. DMA cycle starts.
4. CPU cycle starts.

Figure 19. DMA Control Signals

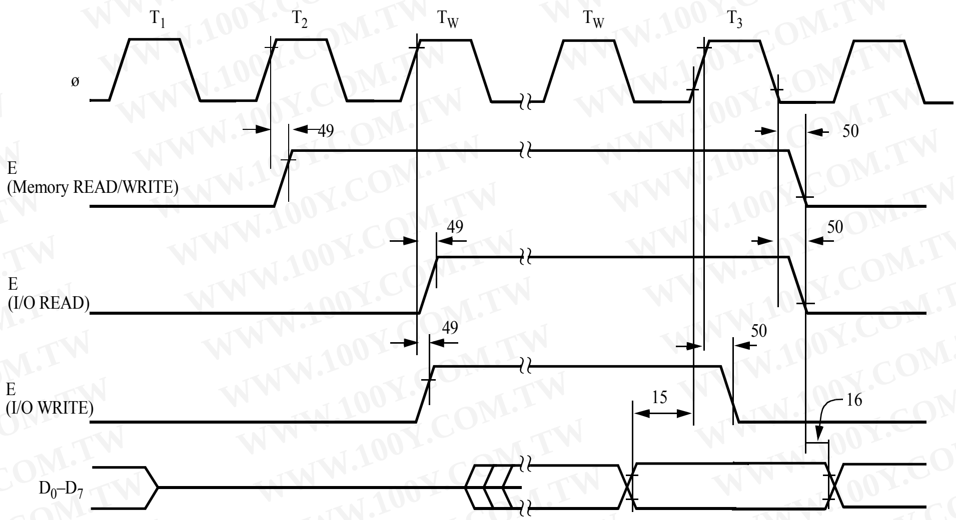


Figure 20. E Clock Timing (Memory R/W Cycle, I/O R/W Cycle)

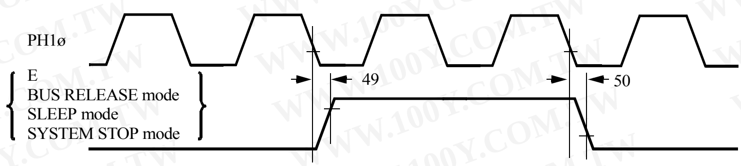


Figure 21. E Clock Timing (Bus Release, Sleep, System Stop Modes

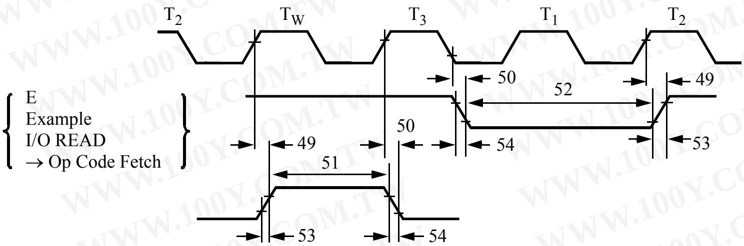


Figure 22. E Clock Timing (P_{WEL} and P_{WEH} Minimum Timing)

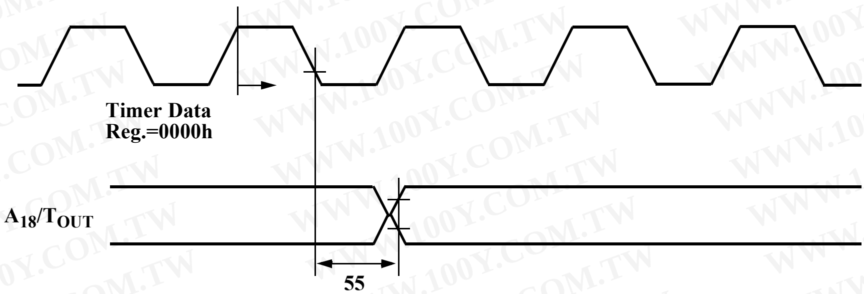


Figure 23. Timer Output Timing

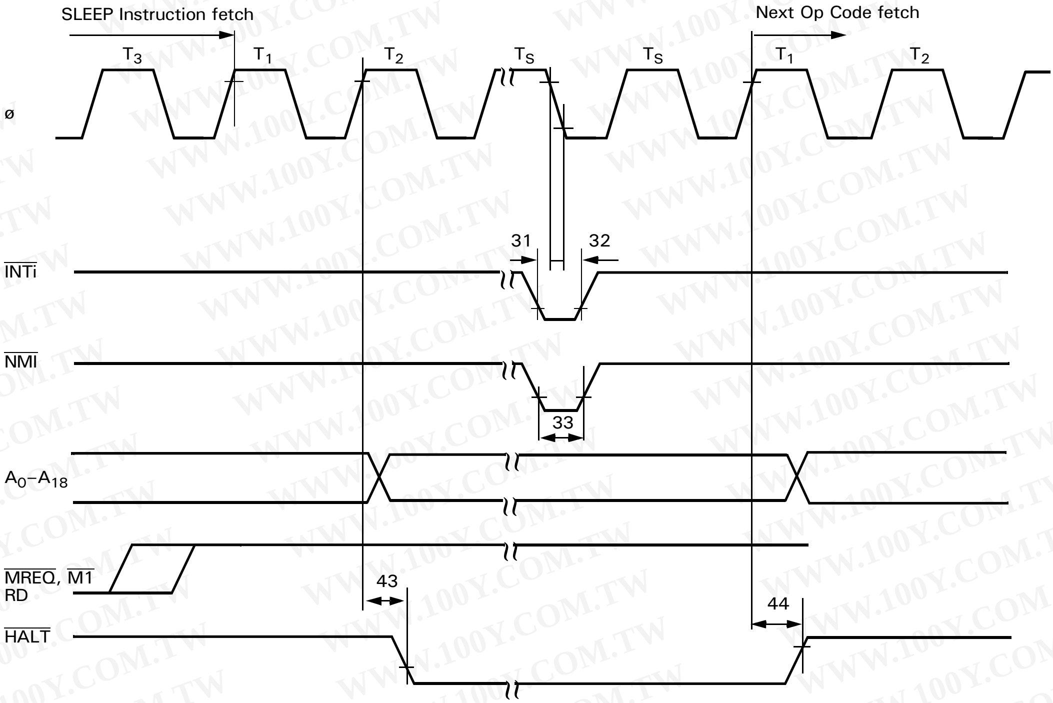


Figure 24. SLEEP Execution Cycle

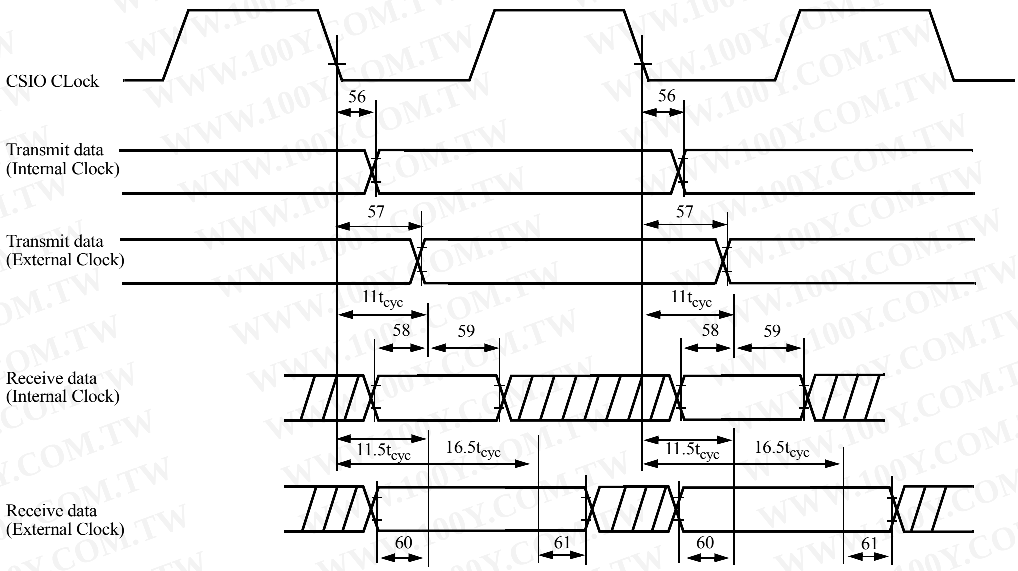


Figure 25. CSIO Receive/Transmit Timing

Input
Rise Time

Exter-
nal

Figure 26. Rise Time and Fall Times

ASCI Register Description

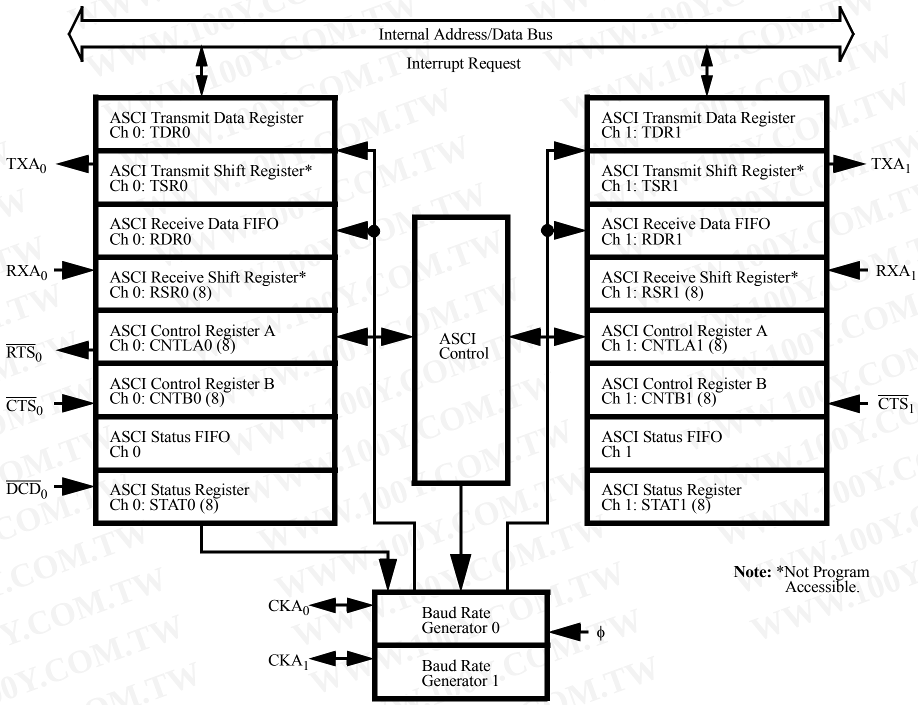


Figure 27. ASCI Block Diagram

ASCI Register Description

The following paragraphs explain the various functions of the ASCI registers.

ASCI Transmit Shift Register 0 (TSR0, TSR1). When the ASCI Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TxA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR IDLEs by outputting a continuous High level. This register is not program accessible

ASCI Transmit Data Register 0,1 (TDR0, TDR1). I/O address = 06h, 07h. Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. The ASCI transmitter is double buffered.

Data can be written into and read from the ASCI Transmit Data Register. If data is read from the ASCI Transmit Data Register, the ASCI data transmit operation is not affected by this READ operation.

ASCI Transmit Data Registers

Register addresses 06h and 07h hold the ASCI transmit data for channel 0 and channel 1, respectively.

Channel 0

Mnemonics TDR0

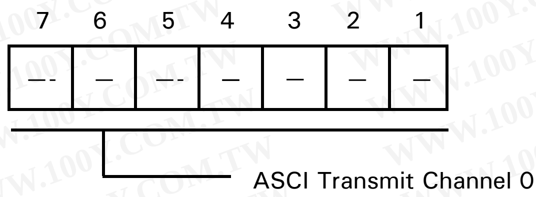


Figure 28. ASCI Register

Channel 1

Mnemonics TDR1

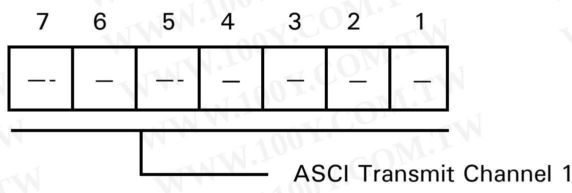


Figure 29. ASCI Register

ASCI Receive Shift Register 0,1 (RSR0, RSR1) This register receives data shifted in on the RxA pin. When full, data is automatically transferred to the ASCI Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

ASCI Receive Data FIFO 0,1 (RDR0, RDR1) I/O Address = 08h, 09h). The ASCI Receive Data Register is a READ-ONLY register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. The ASCI receiver is well buffered.

ASCI Receive Register

Register addresses 08h and 09h hold the ASCI receive data for channel 0 and channel 1, respectively.

Channel 0

Mnemonics TSR0

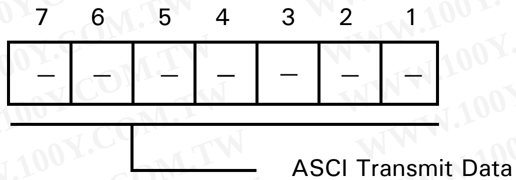


Figure 30. ASCI Receive Register Channel 0

Channel 1

Mnemonics TSR1

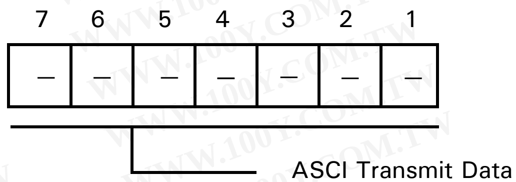


Figure 31. ASCI Receive Register Channel 1R

ASCI Channel Control Register A

ASCI Control Register A 0 (CNTLA0: I/O Address = 00h)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	$\overline{\text{RTS0}}$	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASCI Control Register A 1 (CNTLA1: I/O Address = 01h)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	—	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 32. ASCI Channel Control Register A

MPE: Multi-Processor Mode Enable (bit 7). The ASCI features a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE exhibits no effect. If multiprocessor mode is selected, MPE enables or disables the *wake-up* feature as follows. If MBE is set to 1, only received bytes in which the MPB (multiprocessor bit) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are ignored by the ASCI. If MPE is reset to 0, all bytes, regardless of the state of the

MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

RE: Receiver Enable (bit 6). When RE is set to 1, the ASCI transmitter is enabled. When TE is reset to 0, the transmitter is disables and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

TE: Transmitter Enable (bit 5). When TE is set to 1, the ASCI receiver is enabled. When TE is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

RTS0: Request to Send Channel 0 (bit 4 in CNTLA0 only). If bit 4 of the System Configuration Register is 0, the $\overline{\text{RTS0}}$/TxS pin features the $\overline{\text{RTS0}}$ function. $\overline{\text{RTS0}}$ allows the ASCI to control (START/STOP) another communication devices transmission (for example, by connecting to that device's $\overline{\text{CTS}}$ input). $\overline{\text{RTS0}}$ is essentially a 1 bit output port, having no side effects on other ASCI registers or flags. Bit 4 in CNTLA1 is not used.

MPBR/EFR: Multiprocessor Bit Receive/Error Flag Reset (bit 3). When multiprocessor mode is enabled (MP in CNTLB = 1), MPBR, when read, contains the value of the MPB bit for the most recent receive operation. When written to 0, the EFR function is selected to reset all error flags (OVRN, FE, PE and BRK in the ASEXT register) to 0. MPBR/EFR is undefined during RESET.

MOD2, 1, 0: ASCI Data Format Mode 2, 1, 0 (bits 2–0). These bits program the ASCI data format as shown in Table 8.

Table 10. ASCI Data Formats Mode 2, 1, 0

Bit	Description
MOD2 = 0	0→7 bit data
MOD2 = 1	1→8 bit data
MOD1 = 0	0→No parity
MOD1 = 1	1→Parity enabled
MOD0 = 0	0→1 stop bit
MOD0 = 1	1→2 stop bits

The data formats available based on all combinations of MOD2, MOD1, and MOD0 are indicated in Table 9, Data Formats.

Table 11. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit data + 2 stop
0	1	0	Start + 7 bit data + parity + 1 stop
0	1	1	Start + 7 bit data + parity + 2 stop
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity + 1 stop
1	1	1	Start + 8 bit data + parity + 2 stop

ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02h)
ASCI Control Register B 1 (CNTLB1: I/O Address = 03h)

Bit	7	6	5	4	3	2	1	0
	MPBT	MP	$\overline{\text{CTS}}$/PS	PEO	DR	SS2	SS1	SS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 33. ASCI Channel Control Register B

MPBT: Multiprocessor Bit Transmit (bit 7). When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on the MOD2 (number of data bits) and MOD0 (number of stop bits) bits in CNTLA. The format is as follows.

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP=1) format does not feature any provision for parity.

If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

CTS/PS: Clear to Send/Prescale (bit 5). f bit 5 of the System Configuration Register is 0, the CTS0/RxS pin features the CTS0 function, and the state of the pin can be read in bit 5 of CNTLB0 in a real-time, positive-logic fashion (HIGH = 1, LOW = 0). If bit 5 in the System Configuration Register is 0 to auto-enable CTS0, and the pin is negated (High), the TDRE bit is inhibited (forced to 0). Bit 5 of CNTLB1 reads back as 0.

If the SS2–0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under these circumstances, a 0 indicates a divide-by-10 prescale function, while a 1 indicates divide-by-30. The bit resets to 0.

PEO: Parity Even Odd (bit 4). PEO selects oven or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

DR: Divide Ratio (bit 3). If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide- by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (bits 2–0). If these bits are 111, as they are after RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, these bits specify a power-of-two divider for the PHI clock as indicated in Divide Ratio.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS features the CKAO function when bit 4 of the System Configuration

Register is 0. $\overline{DCD0}$/CKA1 features the CKA1 function when bit 0 of the Interrupt Edge register is 1.

Table 12. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

ASCI Status Register 0, 1 (STAT0, 1)

Each channel status register allows interrogation of ASCI communication, error and modem control signal status, and enabling or disabling of ASCI interrupts.

ASCI Status Register 0 (STAT0: I/O Address = 04h)

Bit	7	6	5	4	3	2	1	0
	RDRF	OVRN	PE	FE	RE	$\overline{\text{DCD}}_0$	TDRE	TIE
	R	R	R	R	R/W	R	R	R/W

ASCI Status Register 1 (STAT1: I/O Address = 05h)

Bit	7	6	5	4	3	2	1	0
	RDRF	OVRN	PE	FE	RE	—	TDRE	TIE
	R	R	R	R	R/W		R	R/W

Figure 34. ASCI Status Registers

RDRF: Receive Data Register Full (bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty RxFIFO.

Note: If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO.

RDRF is cleared to 0 by reading RDR and most recent character in the FIFO from IOSTOP mode, during RESET and for ASCI0 if the $\overline{\text{DCD0}}$ input is auto-enabled and is negated (High).

OVRN: Overrun Error (bit 6). An overrun condition occurs when the receiver finishes assembling a character, but the RxFIFO is full so that there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register, and also by

RESET, in IOSTOP mode, and for ASCI0 if the $\overline{\text{DCD0}}$ pin is auto enabled and is negated (High).

When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the last good character comes to the top of the FIFO so that OVRN is set, and software then writes a 1 to EFR to clear it.

PE: Parity Error (bit 5). A parity error is detected when parity checking is enabled by the MOD1 bit in the CNT1LA register being 1, and a character is assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until or unless the error character becomes the oldest one in the RxFIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register, and also by RESET, in IOSTOP mode, and for ASCI0 if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

FE: Framing Error (bit 4). A framing error is detected when the stop bit of a character is sampled as 0/SPACE. However, this status bit is not set until or unless the error character becomes the oldest one in the RxFIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register, and also by RESET, in IOSTOP mode, and for ASCIO if the $\overline{\text{DCDO}}$ pin is auto-enabled and is negated (High).

REI: Receive Interrupt Enable (bit 3). RIE should be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, the receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel sets its request-routing field to receive data from this ASCI. That is, if SM1–0 are 11 and SAR17–16 are 10, or DIM1 is 1 and IAR17–16 are 10, then ASCI1 does not request an interrupt for RDRF. If RIE is 1, either ASCI requests an interrupt when OVRN, PE or FE is set, and ASCI0 requests an interrupt when $\overline{\text{DCD0}}$ goes High. RIE is cleared to 0 by RESET.

DCD0: Data Carrier Detect (bit 2 STAT0). If bit 0 of the Interrupt Edge Register (IER0) is 0, the DCD0/CKA1 pin features the DCD0 function, and this bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When IER0 is 0, bit 6 of the ASEXT0 register is 0 to select auto-enabling, and the pin is negated (High), the bit 2 of STAT1 is not used.

TDRE: Transmit Data Register Empty (bit 1). TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCIO, if the CTS0 pin is auto-enabled in the ASEXT0 registers and the pin is High, TDRE is reset to 0.

TIE: Transmit Interrupt Enable (bit 0). TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

CSIO Control/Status Register

CNTR: I/O Address = 0Ah. CNTR is used to monitor CSIO status, enable and disable the CSIO, enable and disable interrupt generation, and select the data clock speed and source.

Bit	7	6	5	4	3	2	1	0
	EF	EIE	RE	TE	—	SS2	SS1	SS0
	R	R/W	R/W	R/W		R/W	R/W	R/W

Figure 35. CSIO Control Register

EF: End Flag (bit 7). EF is set to 1 by the CSIO to indicate completion of an 8-bit data transmit or receive operation. If the End Interrupt Enable (EIE) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF = 1. The CSIO clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.

EIE: End Interrupt Enable (bit 6). EIE is set to 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.

RE: Receive Enable (bit 5). A CSIO receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted in on the RXS pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSIO automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are never both set to 1 at the same time. RE is cleared to 0 during RESET and ISTOP mode.

Transmit Enable (bit 4). A CSIO transmit operation is started by setting TE to 1. When TE is set to 1, the data clock is enabled. When in internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted out on the TXS pin synchronous with the (internal or external) data clock. After transmitting 8 bits of data, the CSIO automatically clears TE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. TE and RE are never both set to 1 at the same time. TE is cleared to 0 during RESET and IOSTOP mode.

SS2, 1, 0: Speed Select 2, 1, 0 (bits 2-0). SS2, SS1 and SS0 select the CSIO transmit/receive clock source and speed. SS2, SS1 and

SS0 are all set to 1 during RESET. Table 13 shows CSIO Baud Rate Selection.

Table 13. CSIO Baud Rate Selection

SS2	SS1	SS0	Divide Ratio
0	0	0	÷20
0	0	1	÷40
0	1	0	÷80
0	1	1	÷160
1	0	0	÷320
1	0	1	÷640
1	1	0	÷1280
1	1	1	External Clock Input(less than ÷20)

After RESET, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

CSIO Transmit/Receive Data Register

(TRDR: I/O Address = 0Bh)

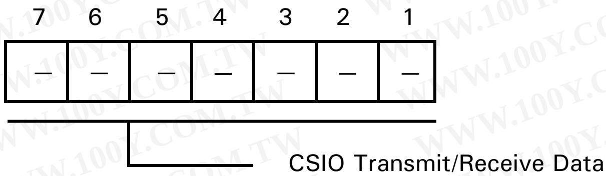


Figure 36. ASCI Receive Register Channel 1R

Timer Data Register Channel 0L

TMDR0L: OCH

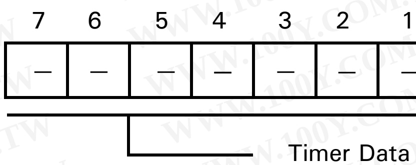


Figure 37. ASCI Receive Register Channel 1R

Timer Data Register Channel 0H

TMDR0H: ODH

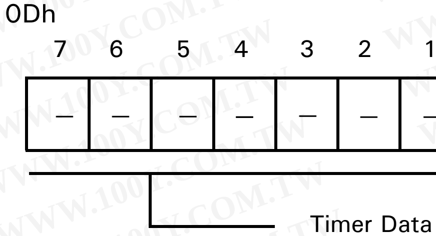


Figure 38. Timer Data Register Channel High

Timer Reload Register 0L

RLDR0L: 0EH

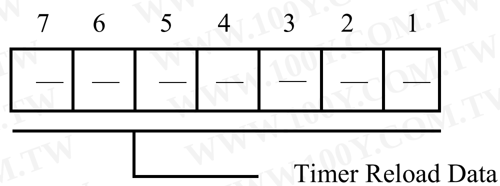


Figure 39. Timer Reload Register Low

Timer Reload Register 0H

RLDR0H

7	6	5	4	3	2	1
–	–	–	–	–	–	–

Timer Reload Data

Figure 40. Timer Reload Register

Timer Control Register (TCR)

TCR monitors both channels (PRT0, PRT1) TMDR status. It also controls enabling and disabling of down counting and interrupts along with controlling output pin A18/T_{OUT} for PRT1.

Bit	7	6	5	4	3	2	1	0
	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Figure 41. Timer Control Register (TCR: I/O Address = 10h)

TIF1: Timer Interrupt Flag 1 (bit 7). When TMDR1 decrements to 0, TIF1 is set to 1, and, when enabled by TIE1 = 1, an interrupt request is generated. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

TIF0: Timer Interrupt Flag 0 (bit 6). When TMDR0 decrements to 0, TIF0 is set to 1, and, when enabled by TIE0 = 1, an interrupt request is generated TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

TIE1: Timer Interrupt Enable 1 (bit 5). When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

TOC1, 0: Timer Output Control (bits 3, 2). TOC1 and TOC0 control the output of PRT1 using the multiplexed T_{OUT}/DREQ pin as indicated in Timer Output Control. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the T_{OUT} function is selected. By programming TOC1 and TOC0, the T_{OUT}/DREQ pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

Table 14. Timer Output Control

TOC1	TOC0	Output	
0	0	Inhibited	The T_{OUT}/DREQ pin is not affected by the PRT.
0	1	Toggled	If bit 3 of IAR1B is 1, the T_{OUT}/DREQ pin toggles or is set Low or High as indicated.
1	0	0	
1	1	1	

TDE1, 0: Timer Down Count Enable (bits 1, 0). TDE1 and TDE0 enable and disable down counting for TMDR1 and TMDR0, respectively. When TDEn (N = 0,1) is set to 1, down counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn do not decrement until TDEn is set to 1.

ASCI Extension Control Register Channels 0 and 1

ASEXT0 and ASEXT1

The ASCI Extension Control Register controls functions newly added to the ASCIs in the Z80180 family.

Note: All bits in this register reset to 0.

ASCI Extension Control Register 0(ASEXT0 I/O Address = 12h)

Bit	7	6	5	4	3	2	1	0
	Reserved	DCDO	CTSO	XI	BRGO Mode	Break Nab	Break	Send Break

ASCI Extension Control Register 1 (ASEXT1 I/O Address = 13h)

Bit	7	6	5	4	3	2	1	0
	Reserved	Reserved	Reserved	XI	BRGI Mode	Break Enab	Break	Send Break

Figure 42. ASCI Extension Control Registers, Channel 0 and 1

DCD0 dis (bit 6, ASCI0 only). If bit 0 of the Interrupt Edge Register is 0 to select the $\overline{\text{DCD0}}$ function for the $\overline{\text{DCD0}}$/CKA1 pin, and this bit is 0, the $\overline{\text{DCD0}}$ pin auto-enables the ASCI0 receiver. When the pin is negated/High, the Receiver is held in a RESET state. If bit 0 of the IER is 0 and this bit is 1, the state of the $\overline{\text{DCD}}$-pin has no effect on receiver operation. In either state of this bit, software can read the state of the $\overline{\text{DCD0}}$ pin in the STAT0 register, and the receiver interrupts on a rising edge of $\overline{\text{DCD0}}$.

CTS0 dis (bit 5, ASCI0 only). If bit 5 of the System Configuration Register is 0 to select the $\overline{\text{CTS0}}$ function of the $\overline{\text{CTS0}}$/RXS pin, and this bit is 0, then the $\overline{\text{CTS0}}$ pin auto-enables the ASCIO transmitter, in that when the pin is negated (High), the TDRE bit in the STAT0 register is forced to 0. If bit 5 of the System Configuration Register is 0 and this bit is 1, the state of the $\overline{\text{CTS0}}$ pin exhibits no effect on the transmitter. Regardless of the state of this bit, software can read the state of the $\overline{\text{CTS0}}$ pin the CNTLB0 register.

X1 (bit 4). If this bit is 1, the clock from the Baud Rate Generator or CKA pin is received as a *1X* bit clock (sometimes called *isochronous* mode). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RXA pin is not required to be synchronized to a clock.

BRG Mode (bit 3). If the SS2–0 bits in the CNTLB register are not 111, and this bit is 0, the ASCI Baud Rate Generator divides PHI by 10 or 30, depending on the DR bit in CNTLB, and then by a power of two selected by the SS2–0 bits, to obtain the clock that is presented to the transmitter and receiver and that can be output on the CKA pin. If SS2–0 are not 111, and this bit is 1, the Baud Rate Generator divides PHI by twice (the 16-bit value programmed into the Time Constant Registers, plus 2). This mode is identical to the operation of the baud rate generator in the ESCC.

Break Enable (bit 2). If this bit is 1, the receiver detects break conditions and report them in bit 1, and the transmitter sends breaks under the control of bit 0.

Break Detect (bit 1). The receiver sets this READ-ONLY bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the RxFIFO. The bit is cleared when software writes a 0 to the EFR bit in CNTLA register, also by RESET, by IOSTOP mode, and for ASCIO if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

Send Break (bit 0). If this bit and bit 2 are both 1, the transmitter holds the TXA pin Low to send a break condition. The duration of the break is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

Timer Data Register Channel 1L

Mnemonic TMDR1L:14H

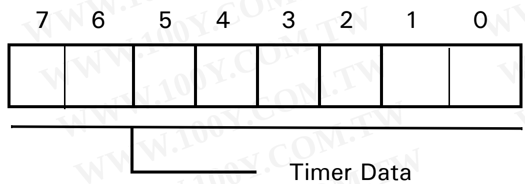


Figure 43. Timer Data Register

Timer Data Register Channel 1H

Mnemonic TMDR1H: 15H

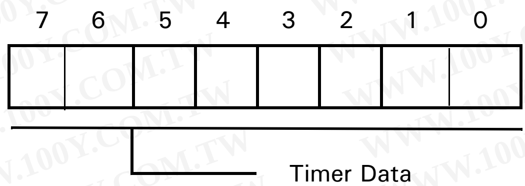


Figure 44. Timer Data Register

Timer Reload Register Channel 1L

Mnemonic RLDR1L: 16H

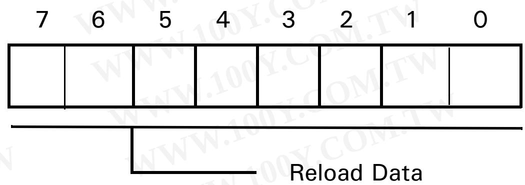


Figure 45. Timer Data Register

Timer Reload Register Channel 1L

Mnemonic RLDR1L: 16H

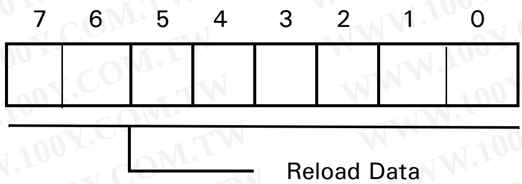


Figure 46. Timer Data Register

Free Running Counter I/O Address = 18H

Mnemonic FRC: 18H

If data is written into the free running counter, the interval of DRAM refresh cycle and baud rates for the ASCI and CSI/O are not guaranteed. In IOSTOP mode, the free running counter continues counting down. It is initialized to FFH,during RESET.

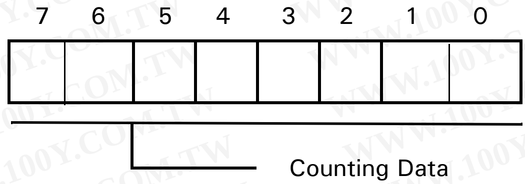


Figure 47. Timer Data Register

DMA Source Address Register Channel 0

(SAR0: I/O ADDRESS = 20h to 22h) specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the REQUEST HANDSHAKE signal.

DMA Source Address Register, Channel 0L

Mnemonic SAR0L

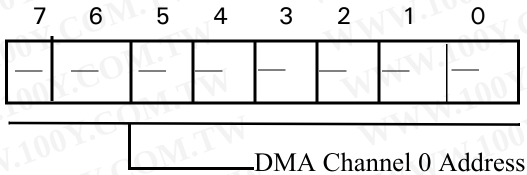


Figure 48. DMA Channel 0L

DMA Source Address Register, Channel 0H

Mnemonic SAR0H

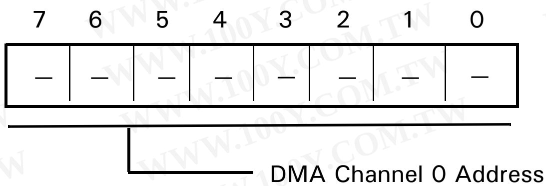


Figure 49. DMA Channel 0H

DMA Source Address Register Channel 0B

Mnemonics SAR0B

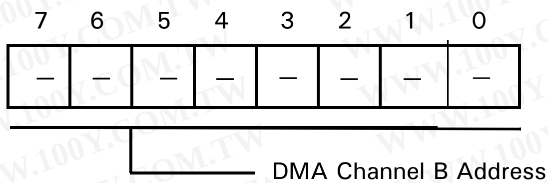


Figure 50. DMA Channel 0B

DMA Destination Address Register Channel 0

(DAR0: I/O ADDRESS = 23h to 25h) specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the REQUEST HANDSHAKE signal for channel 0.

DMA Destination Address Register Channel 0L

Mnemonic DAR0L

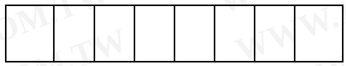


Figure 51. DMA Destination Address Register Channel 0L

DMA Destination Address Register Channel 0H

Mnemonic DAR0H

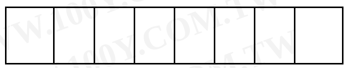


Figure 52. DMA Destination Address Register Channel 0H

DMA Destination Address Register Channel 0B

Mnemonic DAR0B

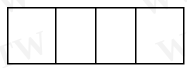


Figure 53. DMA Destination Address Register Channel 0B

Note: In the R1 and Z Mask, these DMA registers are expanded from 4 bits to 3 bits in the package version of CP-68.

Table 15. DMA Transfer Requests

A19*	A18	A17	A16	DMA Transfer Request
X	X	0	0	DREQ0
X	X	0	1	TDR0 (ASCI0)
X	X	1	0	TDR1 (ASCI1)
X	X	1	1	Not Used

DMA Byte Count Register Channel 0

(BCRO: I/O ADDRESS = 26h to 27h) specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64-KB transfers. When one byte is transferred, the register is decremented by 1. If *n* bytes should be transferred, *n* must be stored before the DMA operation.

Note: All DMA Count Register channels are undefined during RESET.

DMA Byte Count Register Channel 0L

Mnemonic BCR0L

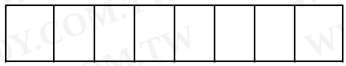


Figure 54. DMA Byte Count Register 0L

DMA Byte Count Register Channel 0H

Mnemonic BCR0H

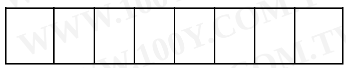


Figure 55. DMA Byte Count Register 0H

DMA Byte Count Register Channel 1L

Mnemonic BCR1L

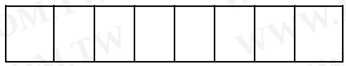


Figure 56. DMA Byte Count Register 1L

DMA Byte Count Register Channel 0H

Mnemonic BCR1H

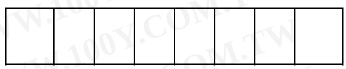


Figure 57. DMA Byte Count Register 0H

DMA Memory Address Register Channel 1

(MAR1: I/O ADDRESS = 28h to 2Ah) specifies the physical memory address for channel 1 transfers, which may also be a destination or source memory address. The register contains 20 bits and may specify up to 1024-KB memory address.

DMA Memory Address Register, Channel 1L

Mnemonic MAR1L

Figure 58. DMA Memory Address Register, Channel 1L

DMA Memory Address Register, Channel 1H

Mnemonic MAR1H

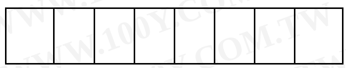


Figure 59. DMA Memory Address Register, Channel 1H

Mnemonic MAR1B

Figure 60. DMA Memory Address Register, Channel 1B

DMA I/O Address Register Channel 1

(IAR1: I/O ADDRESS = 2Bh to 2Dh) specifies the I/O address for channel 1 transfers, which may also be a destination or source I/O address. The register contains 16 bits of I/O address; its most significant byte identifies the REQUEST HANDSHAKE signal and controls the Alternating Channel feature.

All bits in IAR1B reset to 0.

Bit	7	6	5	4	3	2	1	0
	A/T F	A/T C			T_{OUT} DREQ	Req 1 Sel		

Figure 61. IAR MS Byte Register (IARIB: I/O Address 2Dh

DMA I/O Address Register Channel 1L

Mnemonic IAR1L

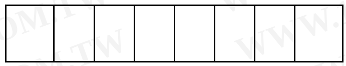


Figure 62. DMA I/O Address Register Channel 1L

DMA I/O Address Register Channel 1H

Mnemonic IAR1H

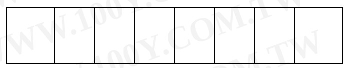


Figure 63. DMA I/O Address Register Channel 1H

DMA I/O Address Register Channel 1B

Mnemonic IAR1B

Figure 64. DMA I/O Address Register Channel 1B

DMA Status Register (DSTAT)

DSTAT is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also indicates DMA transfer status, in other words, completed or in progress.

Mnemonic DSTAT

Address 30

Bit	7	6	5	4	3	2	1	0
	DE1	DE0	$\overline{\text{DWE1}}$	$\overline{\text{DWE0}}$	DIE1	DIE0	—	DME
	R/W	R/W	W	W	R/W	R/W		R

Figure 65. DMA Status Register (DSTAT: I/O Address = 30h)

DE1: DMA Enable Channel 1 (bit 7). When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE1, DWE1 should be written with 0 during the same register WRITE access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DME (DMA Main Enable) to 1. DE1 is cleared to 0 during RESET.

DE0: DMA Enable Channel 0 (bit 6). When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE0, DWE0 should be written with 0 during the same register WRITE access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DME (DMA Main Enable) to 1. DE0 is cleared to 0 during RESET.

$\overline{\text{DWE1}}$: DE1 Bit WRITE Enable (bit 5). When performing any software WRITE to DE1, DWE1 should be written with 0 during the same access. DWE1 always reads as 1.

$\overline{\text{DWE0}}$: DE0 Bit WRITE Enable (bit 4). When performing any software WRITE to DE0, DWE0 should be written with 0 during the same access. DWE0 always reads as 1.

DIE1: DMA Interrupt Enable Channel 1 (bit 3). When DIE0 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DIE0: DMA Interrupt Enable Channel 0 (bit 2). When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DME: DMA Main Enable (bit 0). A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When $\overline{\text{NMI}}$ occurs, DME is reset to 0, disabling DMA activity during the $\overline{\text{NMI}}$ interrupt service routine. To restart DMA, DE– and/or DE1 should be written with a 1 (even if the contents are already 1). This WRITE automatically sets DME to 1, allowing DMA operations to continue.

Note: DME cannot be directly written. It is cleared to 0 by $\overline{\text{NMI}}$ or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

DMA Mode Register (DMODE)

DMODE is used to set the addressing and transfer mode for channel 0.

Mnemonic DMODE

Address 31h

Bit	7	6	5	4	3	2	1	0
	—	—	DM1	DM0	SM1	SM0	MMOD	—
			R/W	R/W	R/W	R/W	R/W	

Figure 66. DMA Mode Register (DMODE: I/O Address = 31h)

DM1, DM0: Destination Mode Channel 0 (bits 5,4). Specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET. See Table 16.

Table 16. Channel 0 Destination

DM1	DM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	–1
1	0	Memory	fixed
1	1	I/O	fixed

SM1, SM0: Source Mode Channel 0 (bits 3, 2). Specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. See Table 17.

Table 17. Channel 0 Source

SM1	SM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	–1
1	0	Memory	fixed
1	1	I/O	fixed

Channel 1 Transfer Mode describes all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

MMOD: Memory Mode Channel 0 (bit 1). When channel 0 is configured for memory to/from memory transfers there is no REQUEST HANDSHAKE signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (the byte count register is 0). In CYCLE STEAL mode, the CPU is provided a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected REQUEST HANDSHAKE signal times the transfer and MMOD is ignored. MMOD is cleared to 0 during RESET.

DMA/WAIT Control Register (DCNTL)

DCNTL controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. DCNTL also defines the Request signal for each channel as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.

Bit	7	6	5	4	3	2	1	0
	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 67. DMA/WAIT Control Register (DCNTL: I/O Address = 32h

MWI1, MWI0: Memory Wait Insertion (bits 7-6). Specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET. (See Wait-State Generator for details.)

IWI1, IWI0: I/O Wait Insertion (bits 5-4). Specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET. See Wait-State Generator for details.

DMS1, DMS0: DMA Request Sense (bits 3-2). DMS1 and DMS0 specify the DMA request sense for channel 0 and channel 1 respectively. When reset to 0, the input is level sense. When set to 1, the input is edge sense. DMS1 and DMS0 are cleared to 0 during RESET.

Typically, for an input/source device, the associated DMS bit should be programmed as 0 for level sense because the device undertakes a relatively long period to update its REQUEST signal after the DMA channel reads data from it in the first of the two machine cycles involved in transferring a byte.

An output/destination device takes much less time to update its REQUEST signal, after the DMA channel starts a WRITE operation to it, as the second machine cycle of the two cycles involved in transferring a byte. With zero-wait state I/O cycles, which apply only to the ASCIs, it is impossible for a device to update its REQUEST signal in time, and edge sensing must be used.

With one-wait-state I/O cycles (the fastest possible except for the ASCIs), it is unlikely that an output device is able to update its REQUEST in time, and edge sense is required for output to the ESCC and bidirectional Centronics controller, and is recommended for external output devices connected to T_{OUT}/DREQ.

With two or more wait states in I/O cycles, external output devices on T_{OUT}/DREQ can use edge or level sense depending on their characteristics; edge sense is still recommended for output on the ESCC and bidirectional Centronics controller.

DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (bits 1-0). Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. DIM1 and DIM0 are cleared to 0 during RESET.

Interrupt Vector Low Register

Table 18. Channel 1 Transfer Mode

DIM1	DMI0	Transfer Mode	Address Increment/Decrement
0	0	Memory→I/O	MAR1 +1, IAR1 fixed
0	1	Memory→I/O	MAR1–1, IAR1 fixed
1	0	I/O→Memory	IAR1 fixed, MAR1 + 1
1	1	I/O→Memory	IAR1 fixed, MAR1 –1

Mnemonic: IL

Address 33

Bits 7–5 of IL are used as bits 7–5 of the synthesized interrupt vector during interrupts for the $\overline{INT1}$ and $\overline{INT2}$ pins and for the DMAs, ASCIs, PRTs, and CSIO. These three bits are cleared to 0 during RESET (Figure).

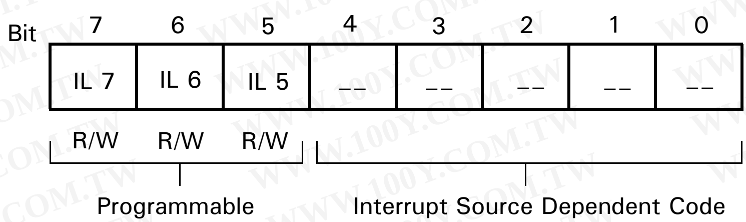


Figure 68. Interrupt Vector Low Register (IL: I/O Address = 33h)

Int/TRAP Control Register

Mnemonics ITC

Address 34

INT/TRAP Control Register (ITC, I/O Address 34h)

This register is used in handling TRAP interrupts and to enable or disable Maskable Interrupt Level 0 and the $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ pins.

Bit	7	6	5	4	3	2	1	0
	TRAP	UFO	--	--	--	ITE2	ITE1	ITE0
	R/W	R				R/W	R/W	R/W

Figure 69. Int/TRAP Control Register

TRAP (bit 7). This bit is set to 1 when an undefined op code is fetched. TRAP can be reset under program control by writing it with a 0, however, it cannot be written with 1 under program control. TRAP is reset to 0 during RESET.

UFO: Undefined Fetch Object (bit 6). When a TRAP interrupt occurs, the contents of a UFO allow the starting address of the undefined instruction to be determined. However, the TRAP may occur on either the second or third byte of the op code. A UFO allows the stacked Program Counter (PC) value to be correctly adjusted. If UFO = 0, the first op code should be interpreted as the stacked PC-1. If UFO = 1, the first op code address is stacked PC-2. UFO is READ-ONLY.

ITE2, 1, 0: Interrupt Enable 2, 1, 0 (bits 2-0). ITE2 and ITE1 enable and disable the external interrupt inputs $\overline{INT2}$ and $\overline{INT1}$, respectively. ITE0 enables and disables interrupts from the on-chip ESCC, CTCs and bidirectional Centronics controller as well as the external interrupt input $\overline{INT0}$. A 1 in a bit enables the corresponding interrupt level while a 0 disables it. A RESET clears ITE0 to 1 and clears ITE1 and ITE2 to 0.

TRAP Interrupt

The Z80180 generates a nonmaskable (not affected by the state of IEF1) TRAP interrupt when an undefined op code fetch occurs. This feature can be used to increase software reliability, implement an *extended* instruction set, or both. TRAP may occur during op code fetch cycles and also if an undefined op code is fetched during the interrupt acknowledge cycle for $\overline{INT0}$ when Mode 0 is used.

When a TRAP interrupt occurs, the Z80180 operates as follows:

1. The TRAP bit in the Interrupt TRAP/Control (ITC) register is set to 1.
2. The current Program Counter (PC) value, reflecting the location of the undefined op code, is saved on the stack.
3. The Z80180 vectors to logical address 0.

Note: If logical address 0000h is mapped to physical address 00000h, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC reveals whether the restart at physical address 00000h was caused by RESET or TRAP.

All TRAP interrupts occur after fetching an undefined second op code byte following one of the *prefix* op codes CBh, DDh, EDh, or FDh, or after fetching an undefined third op code byte following one of the *double-prefix* op codes DDCBh or FDCBh.

The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the op code generated the TRAP. If UFO = 0, the starting address of the invalid instruction is equal to the stacked PC-1. If UFO = 1, the starting address of the invalid instruction is equal to the stacked PC-2.

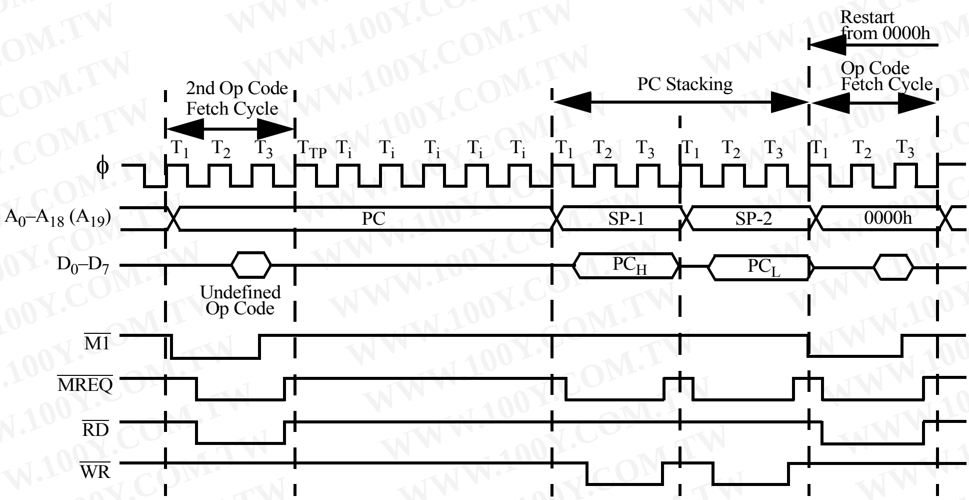


Figure 70. TRAP Timing—2nd Op Code Undefined

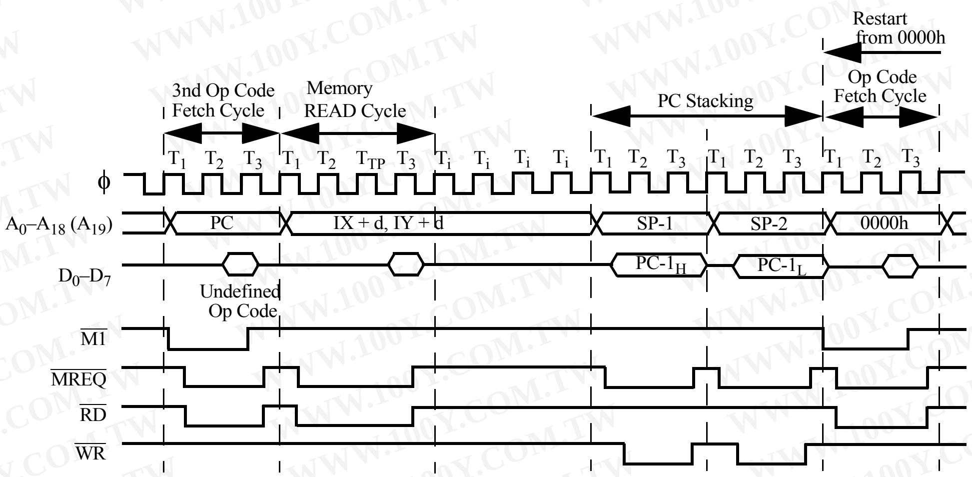


Figure 71. TRAP Timing—3rd Op Code Undefined

Refresh Control Register

Mnemonic RCR

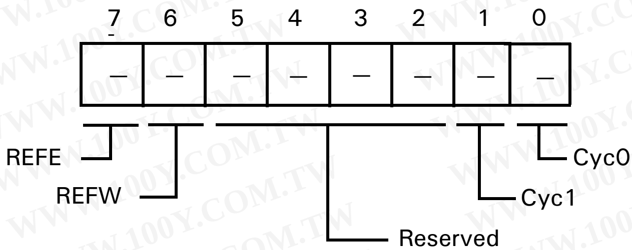


Figure 72. Refresh Control Register (RCA: I/O Address = 36h)

The RCR specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

REFE: Refresh Enable (bit 7). REFE = 0 disables the refresh controller, while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

REFW: Refresh Wait (bit 6). REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET.

CYC1, 0: Cycle Interval (bit 1,0). CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. In the case of dynamic RAMs requiring 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. The underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see DRAM Refresh Intervals).

Table 19. DRAM Refresh Intervals

			Time Interval				
CYC1	**CYC0**	**Insertion Interval**	**Ø: 10 MHz**	**8 MHz**	**6 MHz**	**4 MHz**	**2.5 MHz**
0	0	10 states	(1.0 µs)*	(1.25 µs)*	1.66 µs	2.5 µs	4.0 µs
0	1	20 states	(2.0 µs)*	(2.5 µs)*	3.3 µs	5.0 µs	8.0 µs
1	0	40 states	(4.0 µs)*	(5.0 µs)*	6.6 µs	10.0 µs	16.0 µs
1	1	80 states	(8.0 µs)*	(10.0 µs)*	13.3 µs	20.0 µs	32.0 µs

NOTE: *Calculated interval.

Refresh Control and RESET

After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

Dynamic RAM Refresh Operation

1. REFRESH CYCLE insertion is stopped when the CPU is in the following states:
   a. During RESET
   b. When the bus is released in response to $\overline{\text{BUSREQ}}$
   c. During SLEEP mode
   d. During $\overline{\text{WAIT}}$ states
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to

operate. The time at which the first refresh cycle occurs after the Z80180 reacquires the bus depends on the refresh timer, and possesses no timing relationship with the bus exchange.

3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally latched (until replaced with the next refresh request). The *latched* refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and carries no relationship with the exit from SLEEP mode.

4. The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Independent of the number of missed refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

MMU Common Base Register

Mnemonic CBR

Address 38

MMU Common Base Register (CBR). CBR specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

Bit	7	6	5	4	3	2	1	0
	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 73. MMU Bank Base Register (BBR: I/O Address = 39h)

MMU Bank Base Register (BBR)

Mnemonic BBR

Address 39

BBR specifies the base address (on 4-KB boundaries) used to generate a 19-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

Bit	7	6	5	4	3	2	1	0
	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 74. MMU Bank Base Register (BBR: I/O Address = 39h)

MMU Common/Bank Area Register (CBAR)

Mnemonic CBAR

Address 3A

CBAR specifies boundaries within the Z80180 64-KB logical address space for up to three areas: Common Area, Bank Area and Common Area 1.

Bit	7	6	5	4	3	2	1	0
	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 75. MMU Common/Bank Area Register (CBAR: I/O Address = 3 AH

CA3–CA0:CA (bits 7-4). CA specifies the start (Low) address (on 4-KB boundaries) for the Common Area 1, and also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

BA–BA0 (bits 3-0). BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area, and also determines the most recent address of the Common Area 0. All bits of BA are set to 1 during RESET.

Operation Mode Control Register

Mnemonic OMCR

Address 3E

The Z80180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

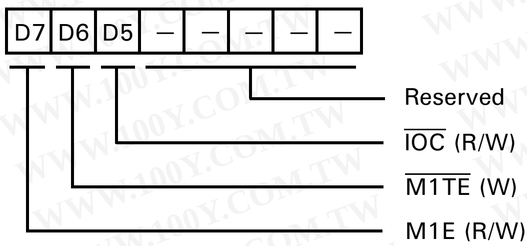


Figure 76. Operating Control Register(OMCR: I/O Address = 3Eh

M1E ($\overline{\textbf{M1}}$ Enable). This bit controls the M1 output and is set to a 1 during reset.

When M1E = 1, the $\overline{\text{M1}}$ output is asserted Low during the op code fetch cycle, the $\overline{\text{INT0}}$ acknowledge cycle, and the first machine cycle of the $\overline{\text{NMI}}$ acknowledge.

On the Z80180, this choice makes the processor fetch a RETI instruction one time only, and when fetching a RETI from zero-wait-state memory, uses three clock machine cycles which are not fully Z80-timing compatible, but are compatible with the on-chip CTCs.

When MIE = 0, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching a RETI instruction one time only with normal timing, the processor refetches the instruction using fully Z80-compatible cycles that include driving $\overline{M1}$ Low. As a result, some external Z80 peripherals may require properly decoded RETI instruction.

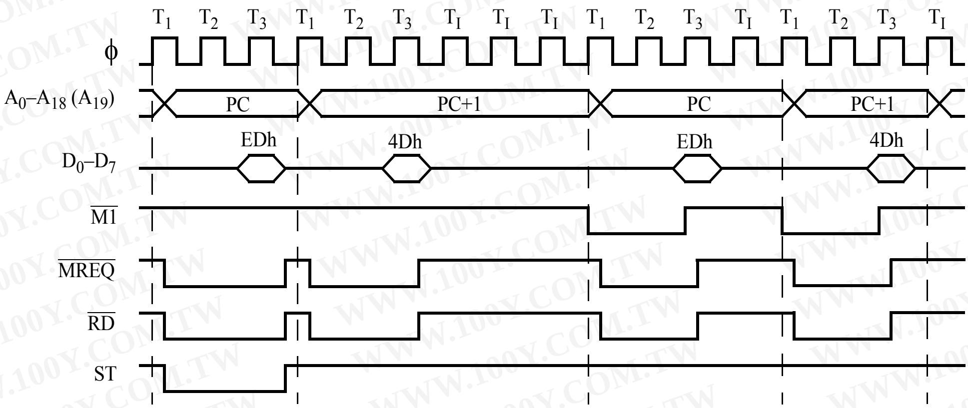


Figure 77. RETI Instruction Sequence with MIE=0

I/O Control Register (ICR)

ICR allows relocating of the internal I/O addresses. ICR also controls enabling/disabling of the IOSTOP mode (Figure).

Bit	7	6	5	4	3	2	1	0
	IOA7	IOA6	IOSTP	—	—	—	—	—
	R/W	R/W	R/W					

Figure 78. I/O Control Register (ICR: I/O Address = 3Fh)

IOA7, 6: I/O Address Relocation (bits 7,6)

IOA7 and IOA6 relocate internal I/O as illustrated in Figure 74.

Note: The high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.

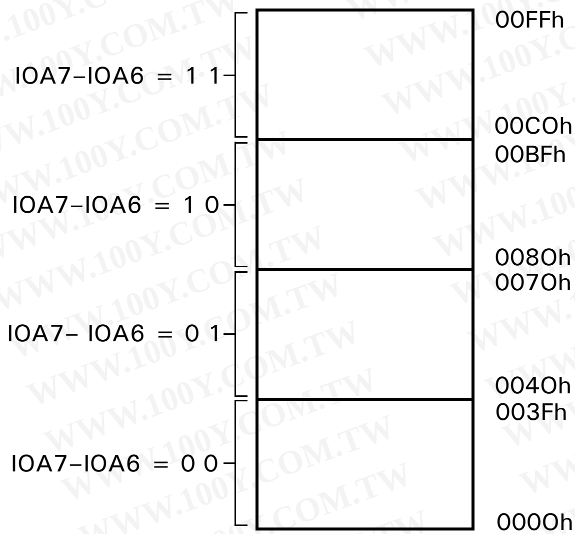
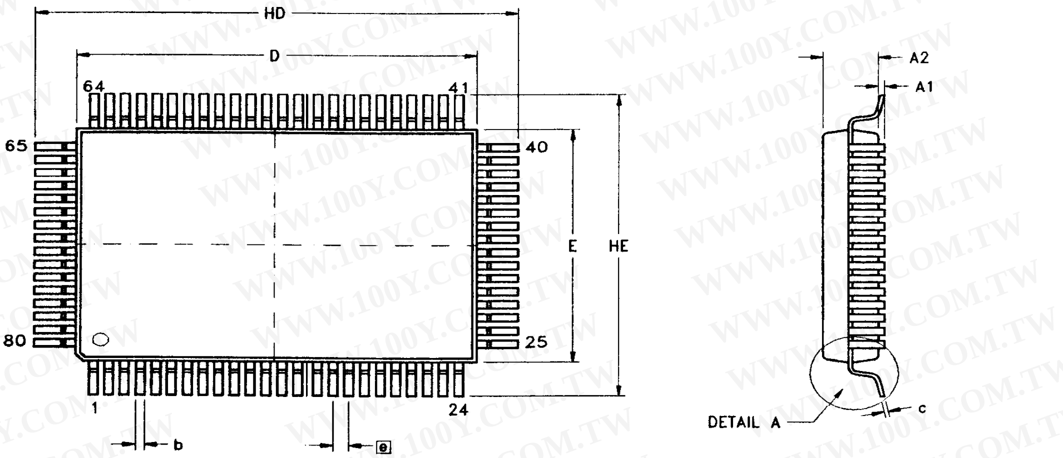


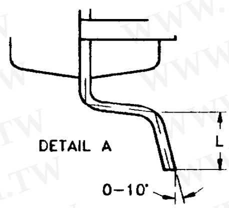
Figure 79. I/O Address Relocation

IOSTP: IOSTOP Mode (bit 5) IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTOP is reprogrammed or RESET to 0.

Package Information

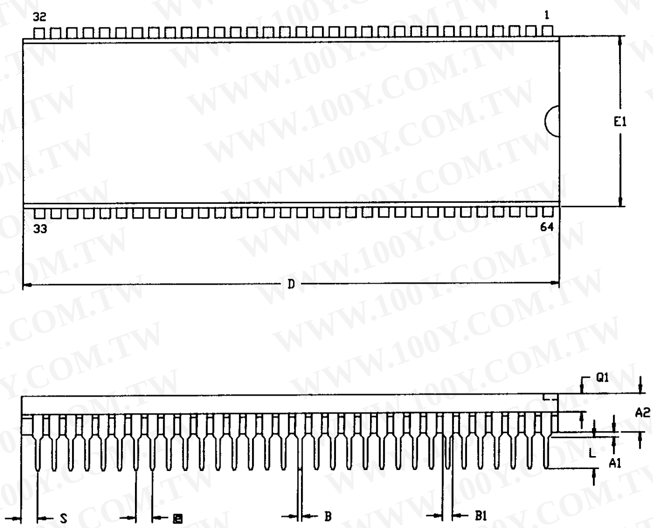


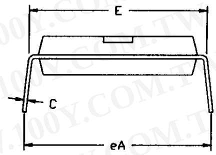
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.30	0.45	.012	.018
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.80 TYP		.0315 TYP	
L	0.70	1.10	.028	.043



NOTES:
1. CONTROLLING DIMENSIONS: MILLIMETER
2. MAX. COPLANARITY: $\frac{.10}{.004}$

Figure 80. 80-Pin QFP Package Diagram

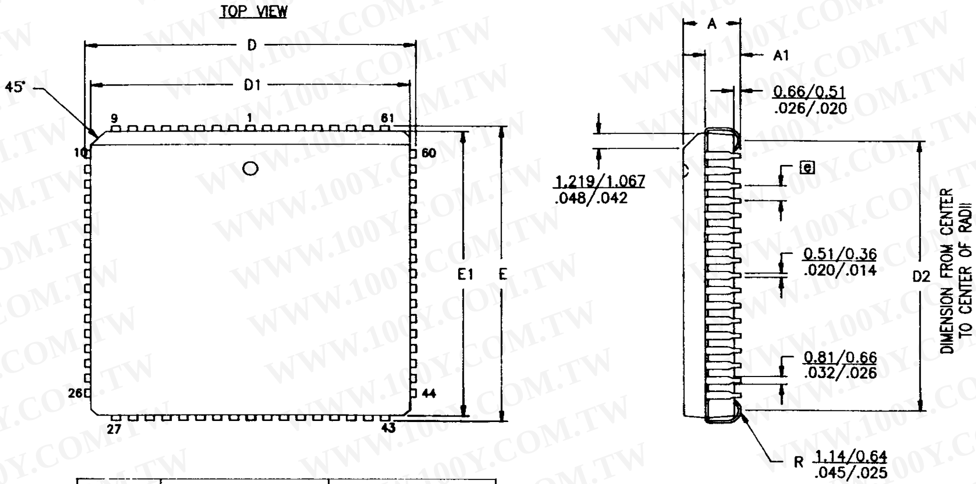




SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	1.07	.015	.042
A2	3.68	3.94	.145	.155
B	0.38	0.53	.015	.021
B1	0.94	1.09	.037	.043
C	0.23	0.38	.009	.015
D	57.40	58.17	2.260	2.290
E	18.80	19.30	.740	.760
E1	16.76	17.27	.660	.680
e	1.78 TYP		.070 TYP	
eA	19.30	20.32	.760	.800
L	3.18	3.81	.125	.150
Q1	1.65	1.91	.065	.075
S	1.02	1.78	.040	.070

CONTROLLING DIMENSIONS : INCH

Figure 81. 64-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	25.02	25.40	.985	1.000
D1/E1	24.13	24.33	.950	.958
D2	22.86	23.62	.900	.930
e	1.27 TYP		.050 TYP	

NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : $\frac{\text{MM}}{\text{INCH}}$

Figure 82. 68-Pin PLCC Package Diagram

Ordering Information

Table 20. Ordering Information

Z80180
6, 8, 10, 20, 33 MHz
Z8018010FSC
Z8018010PSC
Z8018010VSC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

Codes

Package	F = Plastic Quad Flatpack
	P = Plastic Dual In Line
	V = Plastic Leaded Chip Carrier
Temperature	S = 0°C to +70°C
Speed	6 = 6 MHz
	8 = 8 MHz
	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

The Z80180 is a 10-MHz DIP, 0ºC to 70ºC, with Plastic Standard Flow.

Z	ZiLOG Prefix
80180	Product Number
10	Speed
P	Package
S	Temperature
C	Environmental Flow