512K × 8 CMOS FLASH MEMORY

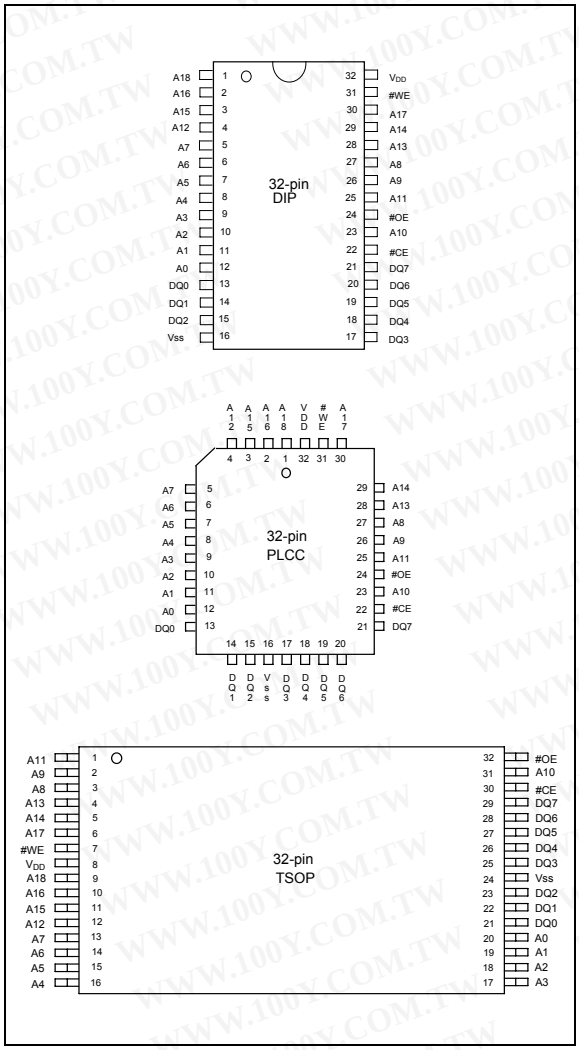
GENERAL DESCRIPTION

The W29C040 is a 4-megabit, 5-volt only CMOS page mode Flash Memory organized as 512K × 8 bits. The device can be written (erased and programmed) in-system with a standard 5V power supply. A 12-volt VPP is not required. The unique cell architecture of the W29C040 results in fast write (erase/program) operations with extremely low current consumption (compared to other comparable 5-volt flash memory products.) The device can also be erased and programmed by using standard EPROM programmers.

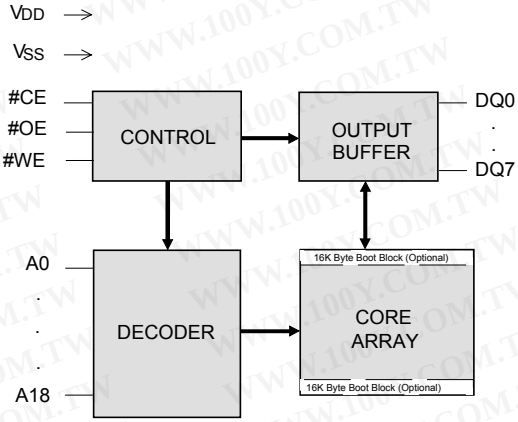
FEATURES

- Single 5-volt write (erase and program) operations
- Fast page-write operations
  - 256 bytes per page
  - Page write (erase/program) cycle: 5 mS (typ.)
  - Effective byte-write (erase/program) cycle time: 19.5 μS
  - Optional software-protected data write
- Fast chip-erase operation: 50 mS
- Two 16 KB boot blocks with lockout
- Page write (erase/program) cycles: 50K (typ.)
- Read access time: 70/90/120 nS
- Ten-year data retention
- Software and hardware data protection
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 μA (typ.)
- Automatic write (erase/program) timing with internal VPP generation
- End of write (erase/program) detection
  - Toggle bit
  - Data polling
- Latched address and data
- All inputs and outputs directly TTL compatible
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin 600 mil DIP, TSOP and PLCC

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0 – A18	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#WE	Write Enable
VDD	Power Supply
VSS	Ground

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W29C040 is controlled by #CE and #OE, both Chip of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either #CE or #OE is high.

Refer to the read cycle timing waveforms for further details.

Page Write Mode

The W29C040 is written (erased/programmed) on a page basis. Every page contains 256 bytes of data. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded will be erased to "FF hex" during the write operation of the page.

The write operation is initiated by forcing #CE and #WE low and #OE high. The write procedure consists of two steps. Step 1 is the byte-load cycle, in which the host writes to the page buffer of the device.

Step 2 is an internal write (erase/program) cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the byte-load cycle, the addresses are latched by the falling edge of either #CE or #WE, whichever occurs last. The data are latched by the rising edge of either #CE or #WE, whichever occurs first. If the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 200 μS after the initial byte-load cycle, the W29C040 will stay in the page load cycle. Additional bytes can then be loaded consecutively. The page load cycle will be terminated and the internal write (erase/program) cycle will start if no additional byte is loaded into the page buffer. A8 to A18 specify the page address. All bytes that are loaded into the page buffer must have the same page address. A0 to A7 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

In the internal write cycle, all data in the page buffers, i.e., 256 bytes of data, are written simultaneously into the memory array. The typical write (erase/program) time is 5 mS. The entire memory array can be written in 10.4 seconds. Before the completion of the internal write cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

Software-protected Data Write

The device provides a JEDEC-approved optional software-protected data write. Once this scheme is enabled, any write operation requires a three-byte command sequence (with specific data to a specific address) to be performed before the data load operation. The three-byte load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29C040 is shipped with the software data protection enabled. To enable the software data protection scheme, perform the three-byte command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-byte command sequence cycle. Once enabled, the software data protection will remain enabled unless the disable commands are issued. A power transition will not reset the

software data protection feature. To reset the device to unprotected mode, a six-byte command sequence is required. For information about specific codes, see the Command Codes for Software Data Protection in the Table of Operating Modes. For information about timing waveforms, see the timing diagrams below.

Hardware Data Protection

The integrity of the data stored in the W29C040 is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A #WE pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The write and read operation are inhibited when V_{DD} is less than 2.5V.

(3) Write Inhibit Mode: Forcing #OE low, #CE high, or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reach its sense level, the device will automatically time-out 10 mS before any write (erase/program) operation.

Chip Erase Modes

The entire device can be erased by using a six-byte software command code. See the Software Chip Erase Timing Diagram.

Boot Block Operation

There are two boot blocks (16K bytes each) in this device, which can be used to store boot code. One of them is located in the first 16K bytes and the other is located in the last 16K bytes of the memory. The first 16K or last 16K of the memory can be set as a boot block by using a seven-byte command sequence.

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout); a regular programming method can change other memory locations. Once the boot block programming lockout feature is activated, the chip erase function will be disabled. In order to detect whether the boot block feature is set on the two 16K blocks, users can perform a six-byte command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "00002 hex" (for the first 16K bytes) or "7FFF2 hex" (for the last 16K bytes). If the output data is "FF hex," the boot block programming lockout feature is activated; if the output data is "FE hex," the lockout feature is inactivated and the block can be programmed.

To return to normal operation, perform a three-byte command sequence to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Data Polling (DQ7)- Write Status Detection

The W29C040 includes a data polling feature to indicate the end of a write cycle. When the W29C040 is in the internal write cycle, any attempt to read DQ7 of the last byte loaded during the page/byte-load cycle will receive the complement of the true data. Once the write cycle is completed. DQ7 will show the true data. See the #DATA Polling Timing Diagram.

Toggle Bit (DQ6)- Write Status Detection

In addition to data polling, the W29C040 provides another method for determining the end of a write cycle. During the internal write cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the write cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation. See Toggle Bit Timing Diagram.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-byte command sequence can be used to access the product ID. A read from address "00000 hex" outputs the manufacturer code "DA hex." A read from address "00001 hex" outputs the device code "46 hex." The product ID operation can be terminated by a three-byte command sequence.

In the hardware access mode, access to the product ID is activated by forcing #CE and #OE low, #WE high, and raising A9 to 12 volts.

Note: The hardware SID read function is not included in all parts; please refer to Ordering Information for details.

TABLE OF OPERATING MODES

Operating Mode Selection

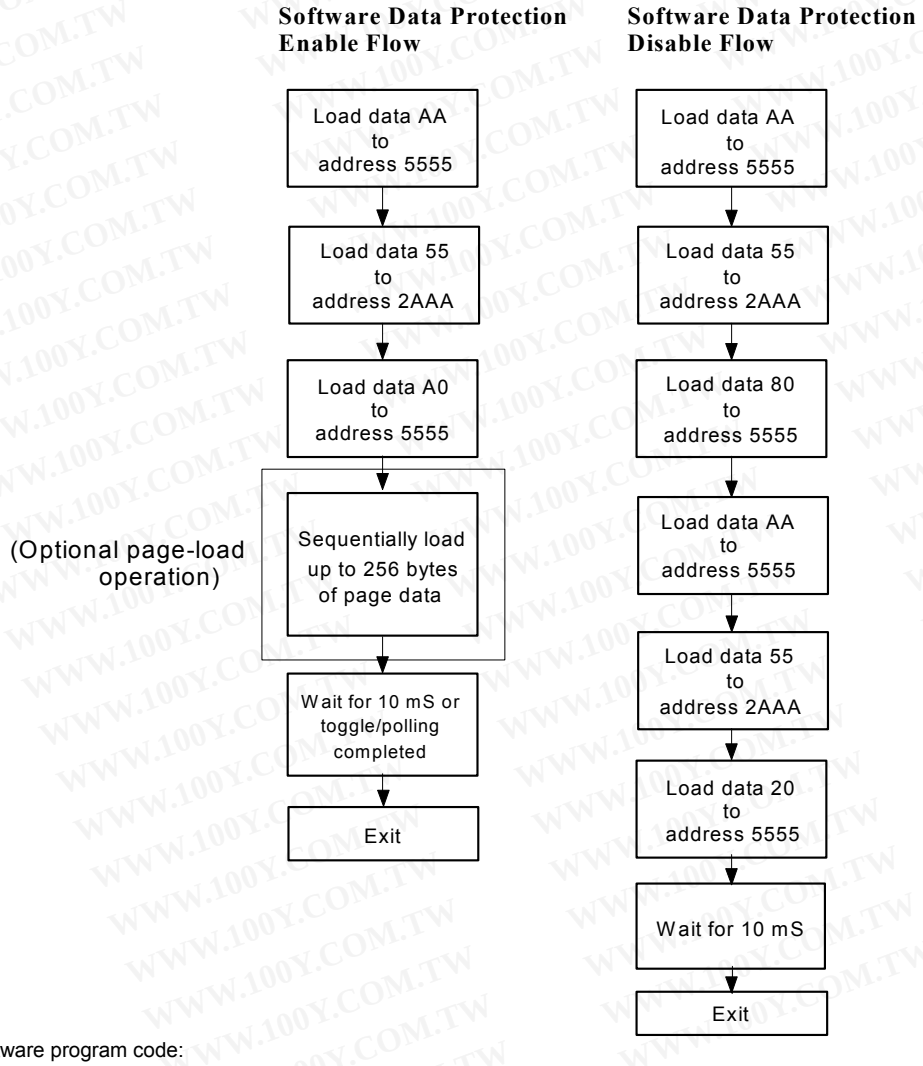
Operating Range: 0 to 70° C for normal products, -40 to 85° C for W29C040xxxxK, V_{DD} = 5V ±10 %, V_{SS} = 0V, V_{HH} = 12V

MODE	PINS				
	#CE	#OE	#WE	ADDRESS	DQ.
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	Dout
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	Din
Standby	V_{IH}	X	X	X	High Z
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}
	X	X	V_{IH}	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Product ID	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}; A1 – A18 = V_{IL}; A9 = V_{HH}	Manufacturer Code DA (Hex)
	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}; A1 – A18 = V_{IL}; A9 = V_{HH}	Device Code 46 (Hex)

Command Codes for Software Data Protection

BYTE SEQUENCE	TO ENABLE PROTECTION		TO DISABLE PROTECTION	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	A0H	5555H	80H
3 Write	-	-	5555H	AAH
4 Write	-	-	2AAAH	55H
5 Write	-	-	5555H	20H

Software Data Protection Acquisition Flow

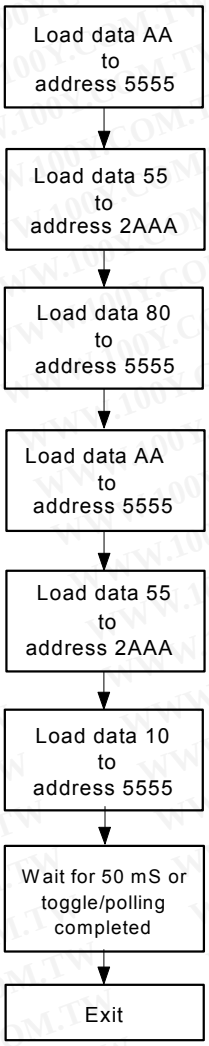


Notes for software program code:
Data Format: DQ7 – DQ0 (Hex)
Address Format: A14 – A0 (Hex)

Command Codes for Software Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	80H
3 Write	5555H	AAH
4 Write	2AAAH	55H
5 Write	5555H	10H

Software Chip Erase Acquisition Flow

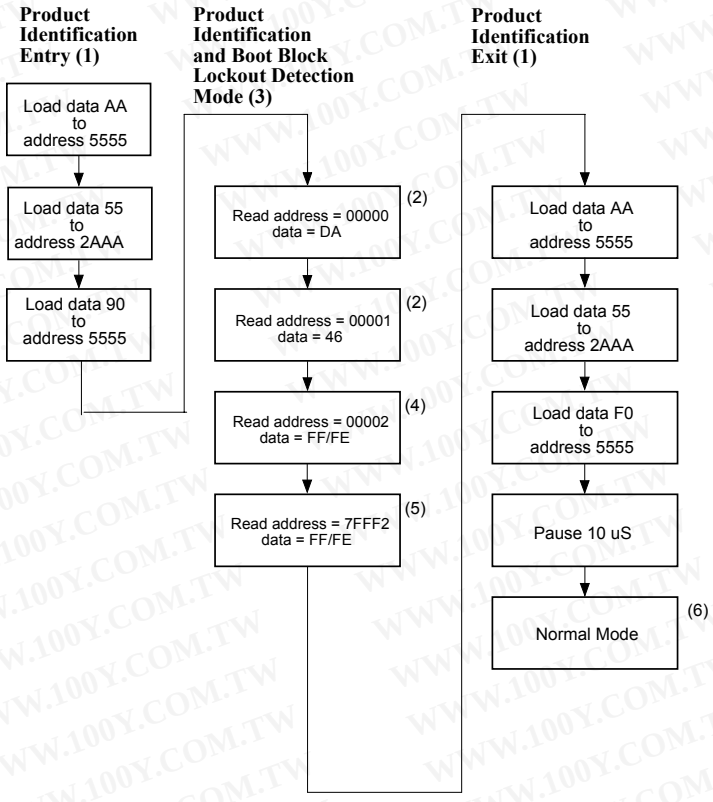


Notes for software chip erase:
Data Format: DQ7 – DQ0 (Hex)
Address Format: A14 – A0 (Hex)

Command Codes for Product Identification and Boot Block Lockout Detection

BYTE SEQUENCE	ALTERNATE PRODUCT (7) IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY		SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION EXIT	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555	AA	5555H	AAH
1 Write	2AAA	55	2AAAH	55H
2 Write	5555	90	5555H	F0H
3 Write	-	-	-	-
4 Write	-	-	-	-
5 Write	-	-	-	-
	Pause 10 μS		Pause 10 μS	

Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ7 – DQ0 (Hex); Address Format: A14 – A0 (Hex)

(2) A1 – A18 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block (address 0002 Hex/7FFF2 Hex respond to first 16K/last 16K) lockout detection mode if power down.

(4), (5) If the output data is "FF Hex," the boot block programming lockout feature is activated; if the output data "FE Hex," the lockout feature is inactivated and the block can be programmed.

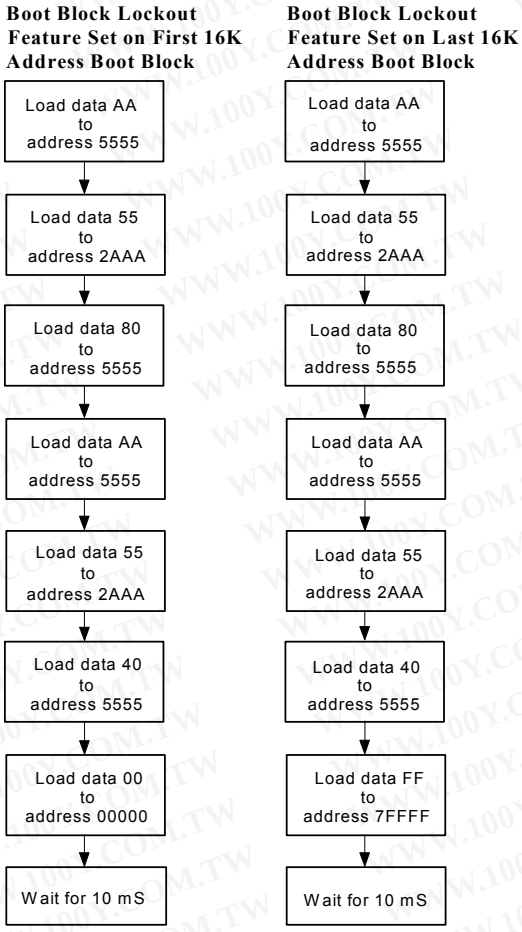
(6) The device returns to standard operation mode.

(7) This product supports both the JEDEC standard 3 bytes command code sequence and original 6 byte command code sequence. For new designs, Winbond recommends that the 3 bytes command code sequence be used.

Command Codes for Boot Block Lockout Enable

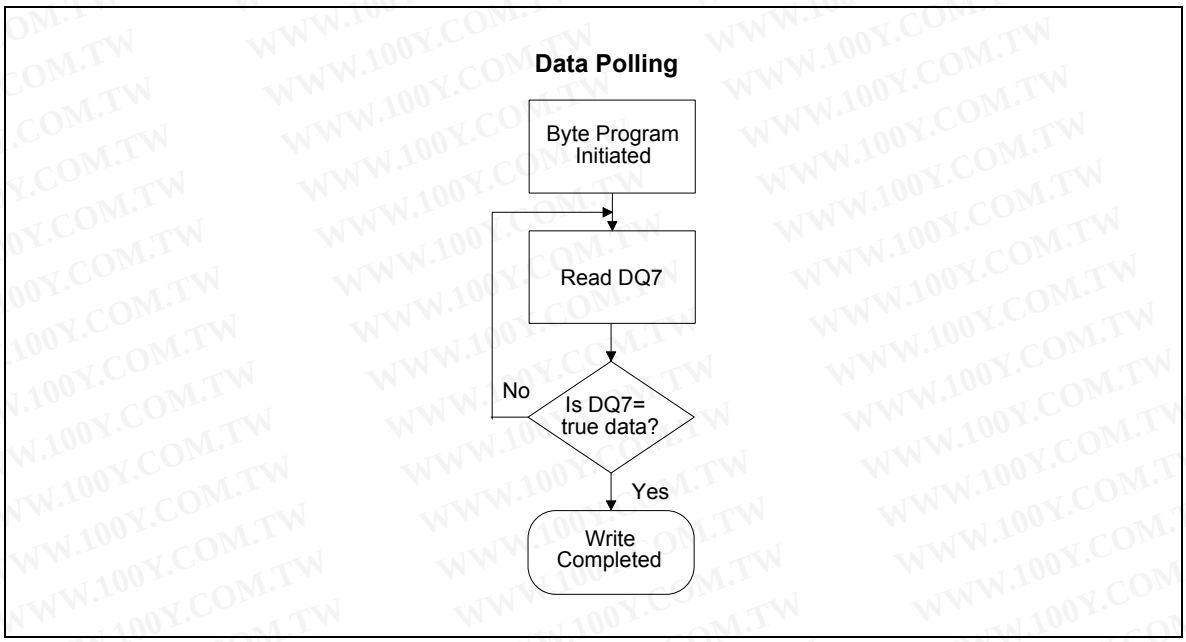
BYTE SEQUENCE	BOOT BLOCK LOCKOUT FEATURE SET ON FIRST 16K ADDRESS BOOT BLOCK		BOOT BLOCK LOCKOUT FEATURE SET ON LAST 16K ADDRESS BOOT BLOCK	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	80H	5555H	80H
3 Write	5555H	AAH	5555H	AAH
4 Write	2AAAH	55H	2AAAH	55H
5 Write	5555H	40H	5555H	40H
6 Write	00000H	00H	7FFFFH	FFH
	Pause 10 mS		Pause 10 mS	

Boot Block Lockout Enable Acquisition Flow

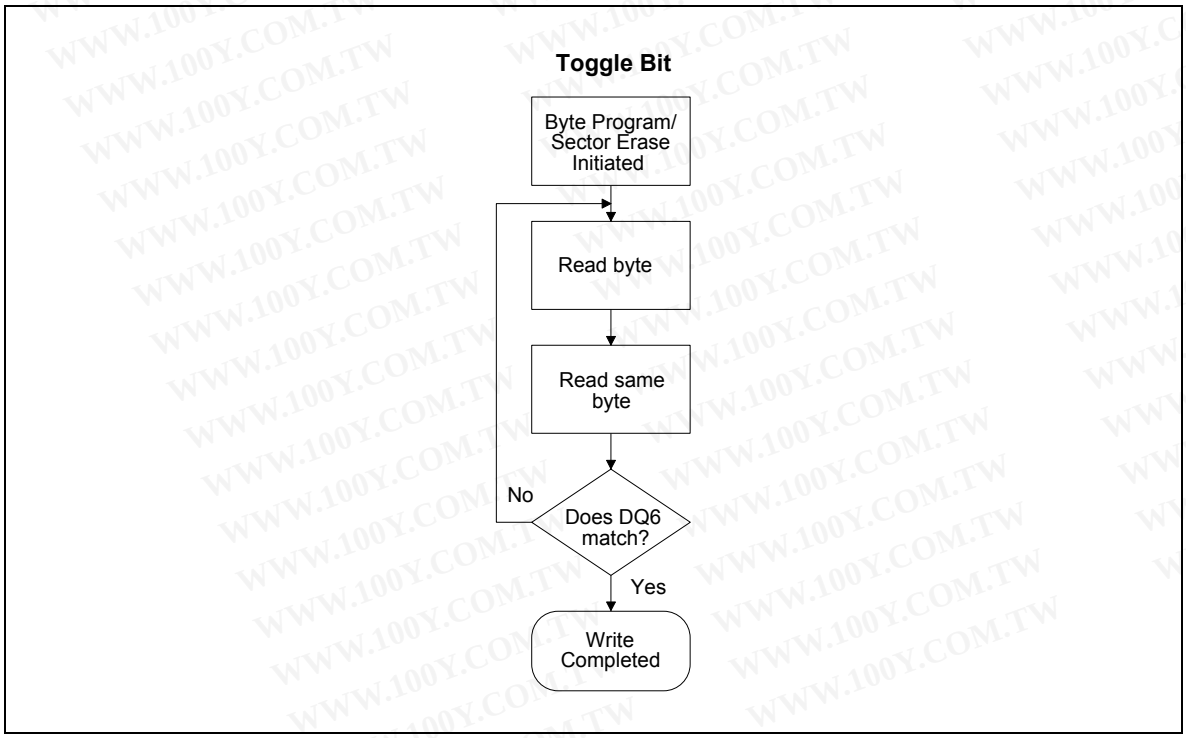


Notes for boot block lockout enable:
1. Data Format: DQ 7 – DQ0 (Hex)
2. Address Format: A14 – A0 (Hex)
3. If you have any questions about this command sequence, please contact the local distributor or Winbond Electronics Corp.

Data Polling Acquisition Flow



Data Toggle Acquisition Flow



DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential Except A9	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on A9 and #OE Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5.0V ±10 %, V_{SS} = 0V, T_A = 0 to 70° C for normal products, -40 to 85° C for W29C040xxxxK)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	#CE = #OE = V_{IL}, #WE = V_{IH}, all DQs open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	-	50	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	#CE = V_{IH}, all DQs open Other inputs = V_{IL}/V_{IH}	-	2	3	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	#CE = V_{DD} -0.3V, all DQs open	-	20	100	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{IN} = V_{SS} to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-	-	0.8	V
Input High Voltage	V_{IH}	For PLCC and TSOP pkg	2.0	-	-	V
		For DIP pkg	2.2	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA	-	-	0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -400 µA	2.4	-	-	V
Output High Voltage CMOS	V_{OH2}	I_{OH} = -100 µA; V_{DD} = 4.5V	4.2	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	100	µS
Power-up to Write Operation	$T_{PU. WRITE}$	10	mS

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
DQ Pin Capacitance	C_{DQ}	V_{DQ} = 0V	12	pF
Input Pin Capacitance	C_{IN}	V_{IN} = 0V	6	pF

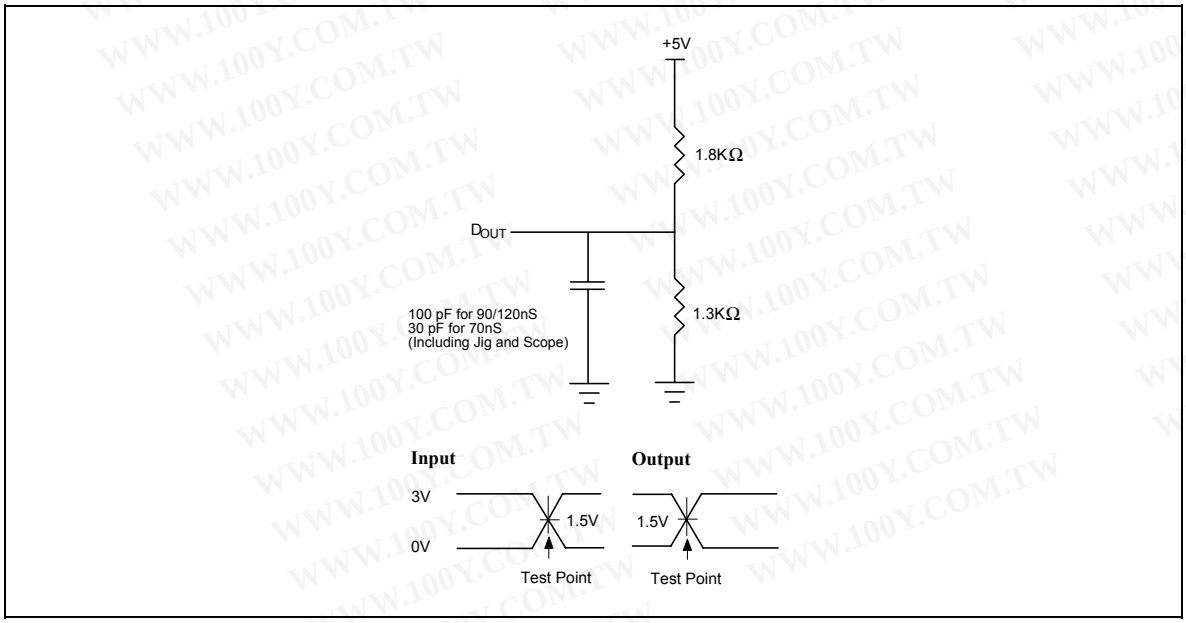
AC CHARACTERISTICS

AC Test Conditions

(V_{DD} = 5.0V ±10 % for 70, 90,120 nS)

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise/Fall Time	<5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 100 pF for 90/120 nS C_L = 30 pF for 70 nS

AC Test Load and Waveform



AC Characteristics, continued

Read Cycle Timing Parameters

(V_{DD} = 5.0V ±10 % V_{SS} = 0V, T_A = 0 to 70° C for normal products, -40 to 85° C for W29C040xxxxK)

PARAMETER	SYM.	W29C040-70		W29C040-90		W29C040-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	90	-	120	-	nS
Chip Enable Access Time	T_{CE}	-	70	-	90	-	120	nS
Address Access Time	T_{AA}	-	70	-	90	-	120	nS
Output Enable Access Time	T_{OE}	-	35	-	40	-	50	nS
#CE High to High-Z Output	T_{CHZ}	-	20	-	25	-	30	nS
#OE High to High-Z Output	T_{OHZ}	-	20	-	25	-	30	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	0	-	nS

Byte/Page-write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Write Cycle (erase and program)	T_{WC}	-	-	10	mS
Address Setup Time	T_{AS}	0	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
#WE and #CE Setup Time	T_{CS}	0	-	-	nS
#WE and #CE Hold Time	T_{CH}	0	-	-	nS
#OE High Setup Time	T_{OES}	0	-	-	nS
#OE High Hold Time	T_{OEH}	0	-	-	nS
#CE Pulse Width	T_{CP}	70	-	-	nS
#WE Pulse Width	T_{WP}	70	-	-	nS
#WE High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	0	-	-	nS
Byte Load Cycle Time	T_{BLC}	-	-	200	µS

Notes:
All AC timing signals observe the following guideline for determining setup and hold times:
(1) High level signal's reference level is V_{IH}
(2) Low level signal's reference level is V_{IL}

AC Characteristics, continued

#DATA Polling Characteristics (1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data Hold Time	T_{DH}	10	-	-	nS
#OE Hold Time	T_{OEH}	10	-	-	nS
#OE to Output Delay (2)	T_{OE}	-	-	-	nS
Write Recovery Time	T_{WR}	0	-	-	nS

Notes:
(1) These parameters are characterized and not 100% tested.
(2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

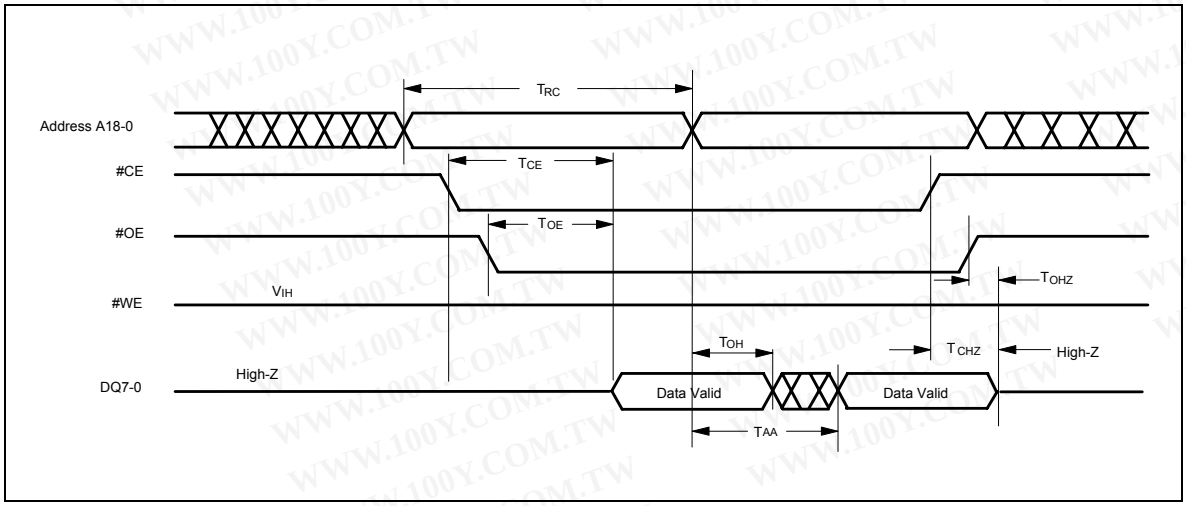
Toggle Bit Characteristics (1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data Hold Time	T_{DH}	10	-	-	nS
#OE Hold Time	T_{OEH}	10	-	-	nS
#OE to Output Delay (2)	T_{OE}	-	-	-	nS
#OE High Pulse	T_{OEHP}	150	-	-	nS
Write Recovery Time	T_{WR}	0	-	-	nS

Notes:
(1) These parameters are characterized and not 100% tested.
(2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

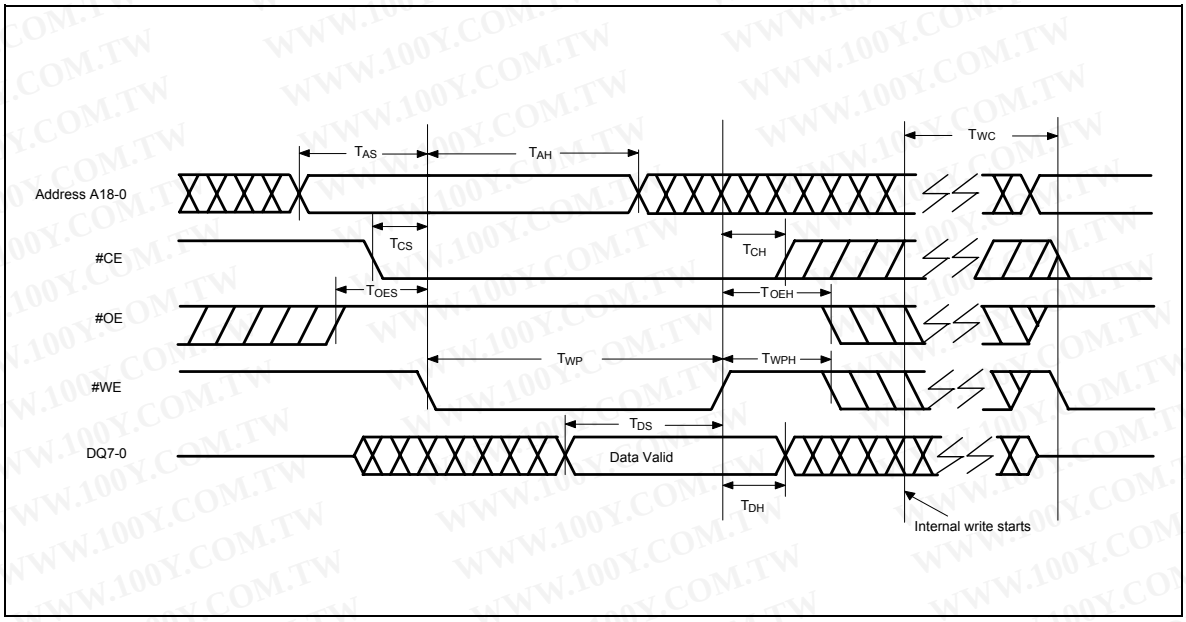
TIMING WAVEFORMS

Read Cycle Timing Diagram

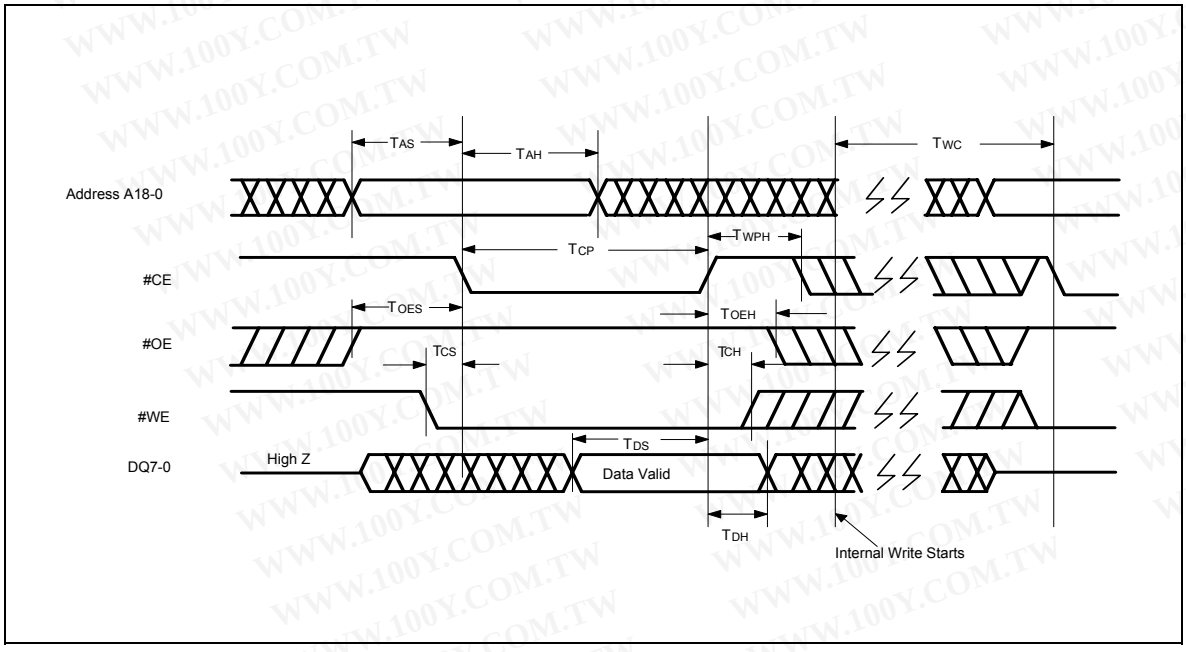


Timing Waveforms, continued

#WE Controlled Write Cycle Timing Diagram

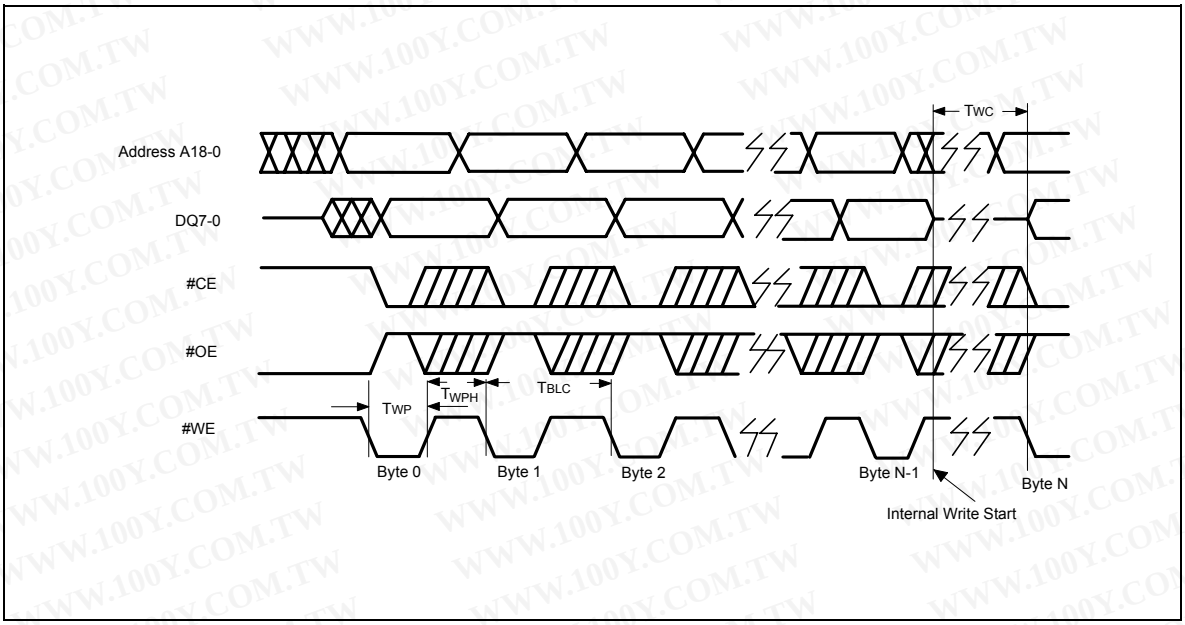


#CE Controlled Write Cycle Timing Diagram

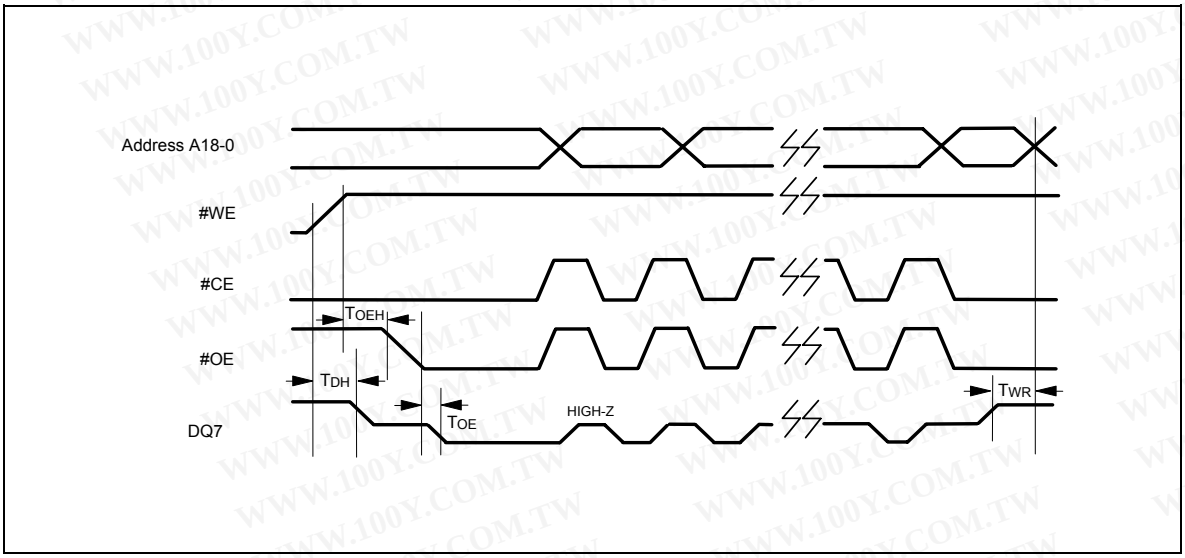


Timing Waveforms, continued

Page Write Cycle Timing Diagram

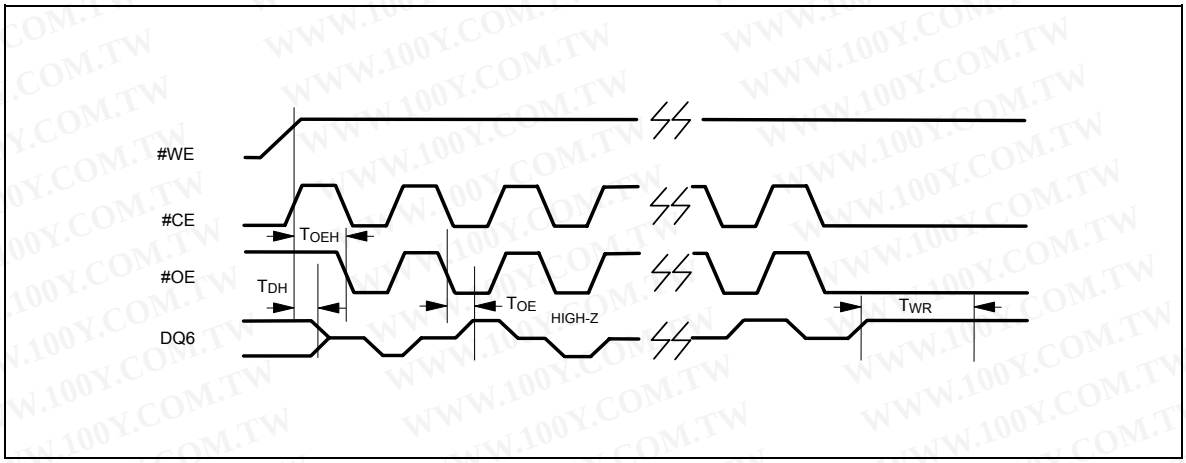


#DATA Polling Timing Diagram

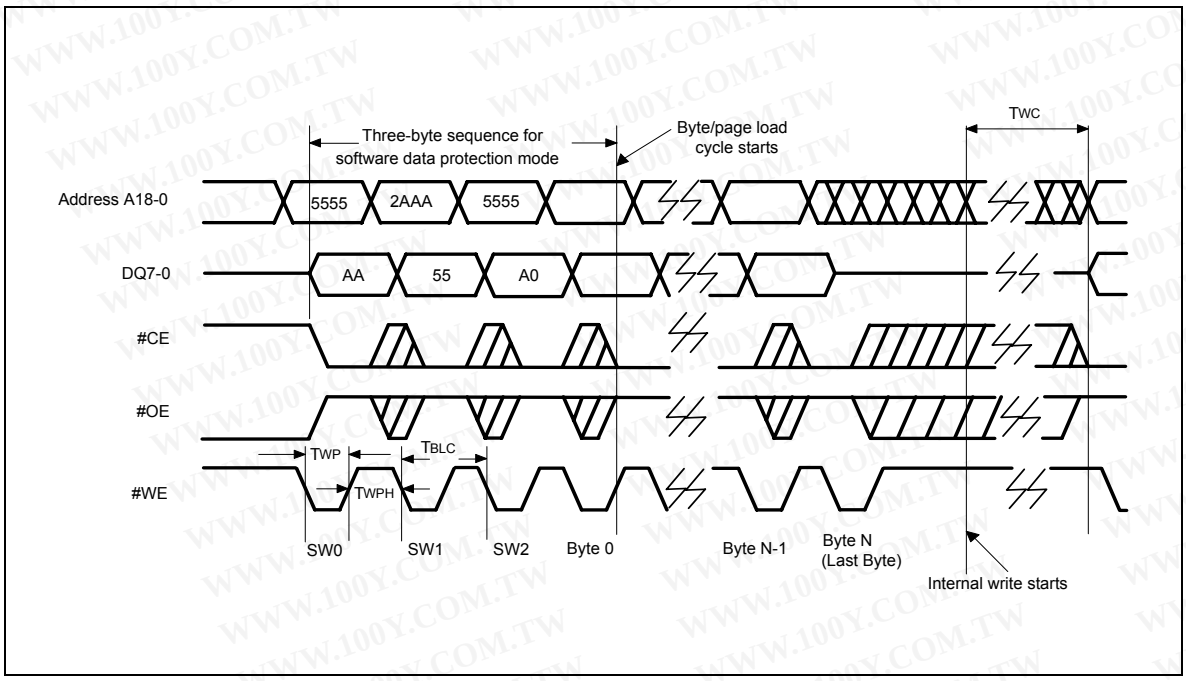


Timing Waveforms, continued

Toggle Bit Timing Diagram

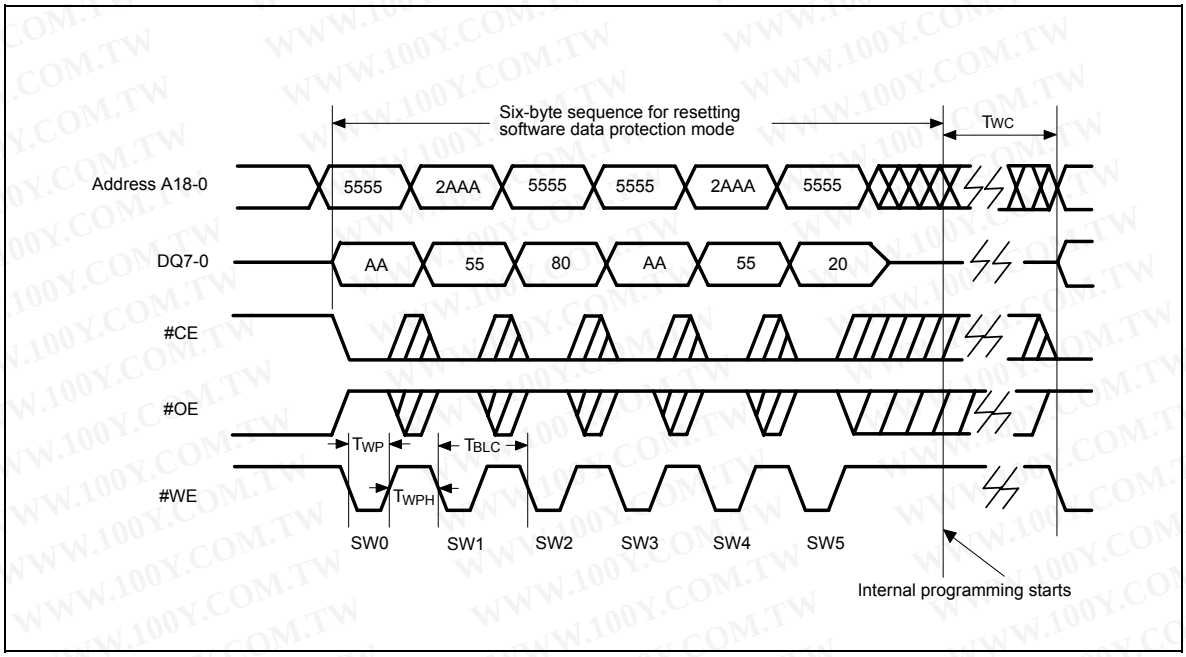


Page Write Timing Diagram Software Data Protection Mode

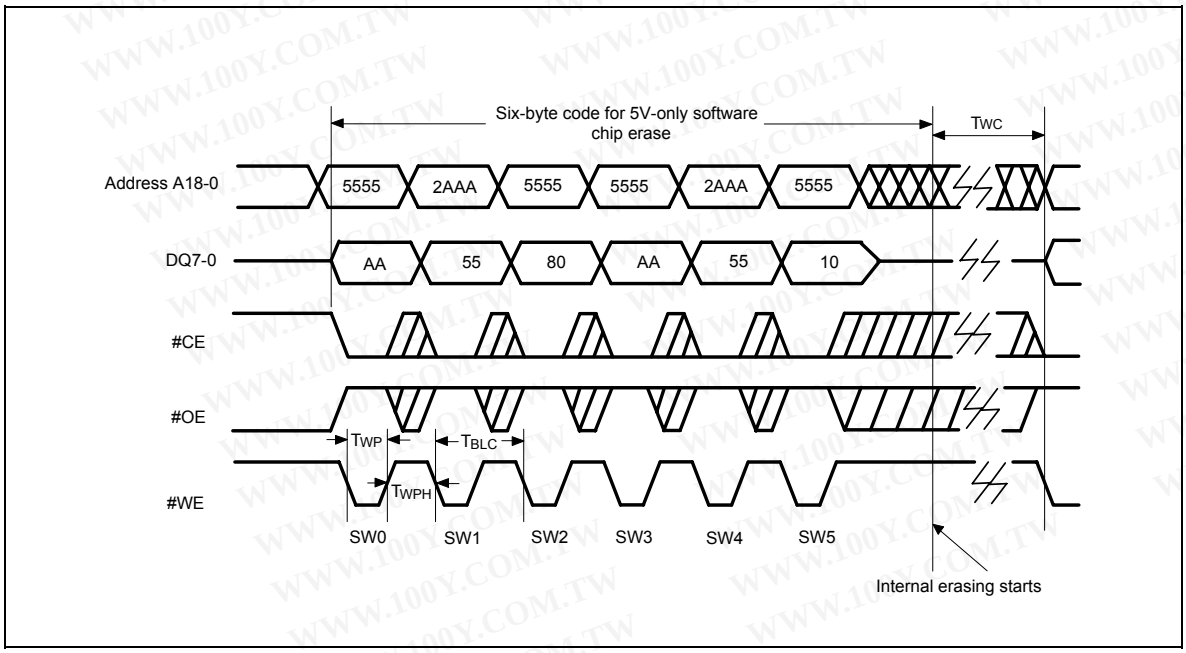


Timing Waveforms, continued

Reset Software Data Protection Timing Diagram



5 Volt-only Software Chip Erase Timing Diagram



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	OPERATING TEMP. (°C)	PACKAGE	CYCLING (K) (MIN.)	HARDWARE SID READ FUNCTION
W29C040-90	90	50	0 to 70	600 mil DIP	1	Y
W29C040-12	120	50	0 to 70	600 mil DIP	1	Y
W29C040T-90	90	50	0 to 70	Type one TSOP	1	Y
W29C040T-12	120	50	0 to 70	Type one TSOP	1	Y
W29C040P-90	90	50	0 to 70	32-pin PLCC	1	Y
W29C040P-12	120	50	0 to 70	32-pin PLCC	1	Y
W29C040-90N	90	50	0 to 70	600 mil DIP	1	N
W29C040-12N	120	50	0 to 70	600 mil DIP	1	N
W29C040T-90N	90	50	0 to 70	Type one TSOP	1	N
W29C040T-12N	120	50	0 to 70	Type one TSOP	1	N
W29C040P-90N	90	50	0 to 70	32-pin PLCC	1	N
W29C040P-12N	120	50	0 to 70	32-pin PLCC	1	N
W29C040-90B	90	50	0 to 70	600 mil DIP	10	Y
W29C040T-70B	70	50	0 to 70	Type one TSOP	10	Y
W29C040T-90B	90	50	0 to 70	Type one TSOP	10	Y
W29C040P-70B	70	50	0 to 70	32-pin PLCC	10	Y
W29C040P-90B	90	50	0 to 70	32-pin PLCC	10	Y
W29C040-90BN	90	50	0 to 70	600 mil DIP	10	N
W29C040T70BN	70	50	0 to 70	Type one TSOP	10	N
W29C040T90BN	90	50	0 to 70	Type one TSOP	10	N
W29C040P70BN	70	50	0 to 70	32-pin PLCC	10	N
W29C040P90BN	90	50	0 to 70	32-pin PLCC	10	N
W29C040P-70K	70	50	-40 to 85	32-pin PLCC	10	Y
W29C040P-90K	90	50	-40 to 85	32-pin PLCC	10	Y
W29C040T-70K	70	50	-40 to 85	Type one TSOP	10	Y
W29C040T-90K	90	50	-40 to 85	Type one TSOP	10	Y

Notes:
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.
3. In Hardware SID Read column: Y = with SID read function; N = without SID read function.

HOW TO READ THE TOP MARKING

Example: The top marking of 32-pin TSOP W29C040T-90

1st line: winbond logo

2nd line: the part number: W29C040T-90

3rd line: the lot number

4th line: the tracking code: 149 O B SA

149: Packages made in '01, week 49

O: Assembly house ID: A means ASE, O means OSE, ...etc.

B: IC revision; A means version A, B means version B, ...etc.

SA: Process code

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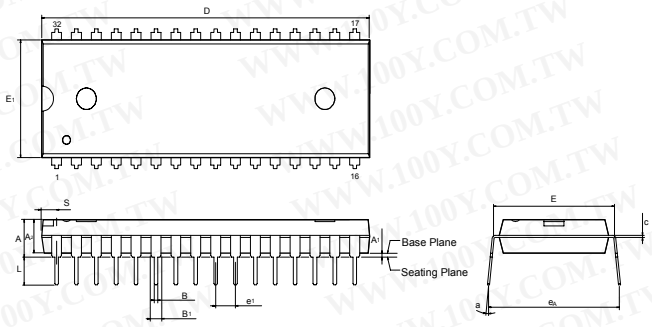
PACKAGE DIMENSIONS

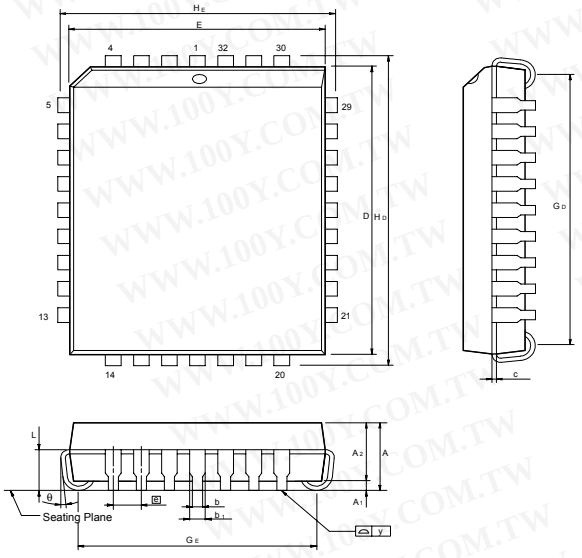
32-pin P-DIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:
1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches
6. General appearance spec. should be based on final visual inspection spec.

32-pin PLCC



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based on final visual inspection sepc.

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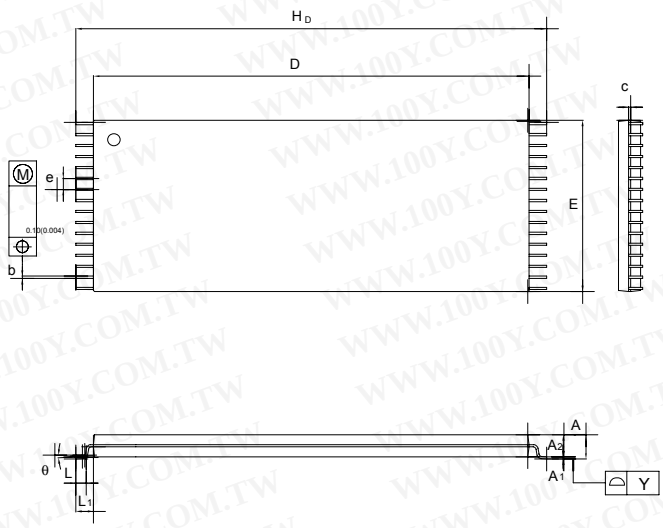
Package Dimensions, continued

32-pin TSOP



Symbol	Dimension In Inches			Dimension In mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A 1	0.002	—	0.006	0.05	—	0.15
A 2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L 1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Note:
Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A3	June 1998	4	Correct Power-on Delay from 5 mS to 10 mS
		11	Correct $T_{PU.WRITE}$ (Typ.) from 5 mS to 10 mS
A4	Oct. 1998	20	Correct 40-pin TSOP Package Drawing by 32-pin TSOP
		9	Correct the Address from 3FFFF to 7FFFF
A5	May 1999	1, 12, 18	Modify TACC: 90/120/150 nS → 90/120 nS binning
		1, 2, 18, 19	Modify Packages: PDIP/SOP/PLCC/TSOP → PLCC/TSOP
A6	Nov. 2000	12	Change Byte Load Cycle Time from 150 µS to 200 µS
		1, 12, 18	Modify TACC: 90/120 nS → 70/90/120 nS binning
		1	Typo Correction
		11	Modify Output Load Parameter
		1, 2, 23, 24	Add DIP Package
		10	Add toggle and polling Acquisition Flow
		6, 7	Correct the Acquisition Flow Wait Time
		5, 23	Add in Hardware SID Read Function Note
A7	April 2001	11	Modify V_{IH} from 2.0V to 2.2V for DIP only (2.0V for PLCC & TSOP; 2.2V for DIP)
A8	9/12/2001	1,19	Range page write (erase/program) cycles between 1K/10K (min.) and 5K/50K (typ.)
A9	May 6, 2002	5, 11, 13	Add operating range -40 to 85° C
		19	Add Part No of W29C040xxxxK for ordering information
		4	Correct V_{DD} Power Up/Down Detection Description
		8	Correct Command Codes and Acquisition Flow for Software Product Identification and Boot Block Lockout Detection
		20	ADD HOW TO READ THE TOP MARKING
A10	April 15, 2005	24	Add Important Notice

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu Chiu, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064