

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
 Http://www.100y.com.tw

W24258



32K × 8 CMOS STATIC RAM

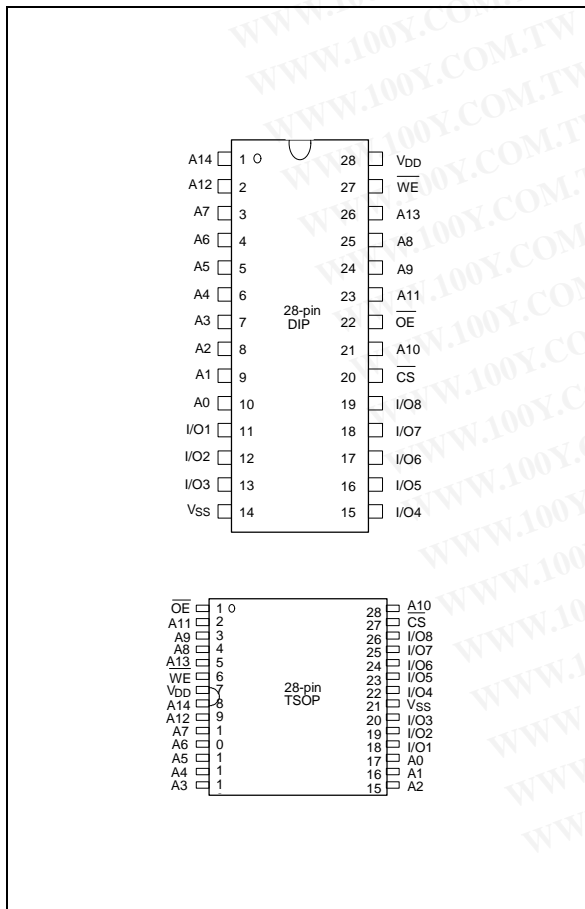
GENERAL DESCRIPTION

The W24258 is a normal speed, very low power CMOS static RAM organized as 32768 × 8 bits that operates on a wide voltage range from 2.7V to 5.5V power supply. The W24258 family, W24258-70LE and W24258-70LI, can meet requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

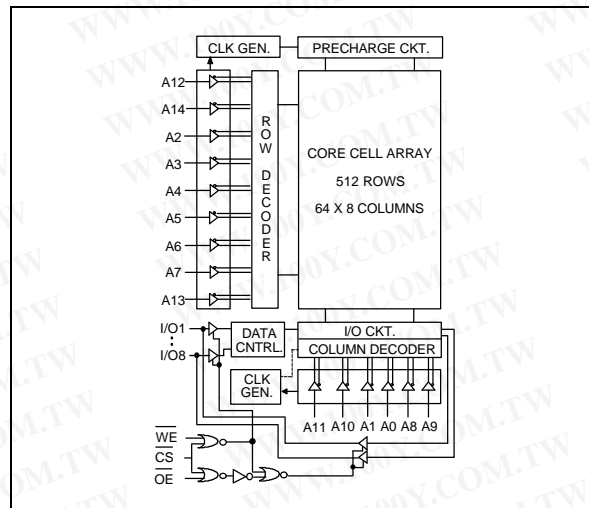
FEATURES

- Low power consumption:
 - Active: 350 mW (max.)
 - Standby: 6 μW (max.)/3V
25 μW (max.)/5V
- Access time: 70 nS (max.)/5V
100 nS (max.)/3V
- Single 3V/5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 28-pin 600 mil DIP, 330 mil SOP and standard type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS	Chip Select Input
WE	Write Enable Input
OE	Output Enable Input
V _{DD}	Power Supply
V _{SS}	Ground

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TRUTH TABLE

CS	OE	WE	MODE	I/O1- I/O8	VDD CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	IDD
L	L	H	Read	Data Out	IDD
L	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT	
Supply Voltage to Vss Potential	-0.5 to +7.0	V	
Input/Output to Vss Potential	-0.5 to VDD +0.5	V	
Allowable Power Dissipation	1.0	W	
Storage Temperature	-65 to +150	°C	
Operating Temperature	LE	-20 to 85	°C
	LI	-40 to 85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VDD = 5V ±10%; VDD = 3V ±10%; VSS = 0V; TA (°C) = -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	5V - 10%		3V - 10%		UNIT
			MIN.	MAX.	MIN.	MAX.	
Input Low Voltage	VIL	-	-0.5	+0.8	-0.5	+0.6	V
Input High Voltage	VIH	-	+2.2	VDD +0.5	+2.0	VDD +0.5	V
Input Leakage Current	ILI	VIN = VSS to VDD	-1	+1	-1	+1	μA
Output Leakage Current	ILO	VIO = VSS to VDD, CS = VIH (min.) or OE = VIH (min.) or WE = VIL (max.)	-1	+1	-1	+1	μA
Output Low Voltage	VOL	IOL = +2.1 mA	-	0.4	-	0.4	V
Output High Voltage	VOH	IOH = -1.0 mA	2.4	-	2.2	-	V

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Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	5V - 10%			3V - 10%			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Operating Power Supply Current	I _{DD}	$\overline{CS} = V_{IL} (\text{max.}), I/O = 0 \text{ mA},$ Cycle = min., Duty = 100%	-	-	70	-	-	30	mA
Standby Power Supply Current	I _{SB}	$\overline{CS} = V_{IH} (\text{min.}),$ Cycle = min., Duty = 100%	-	-	3	-	-	1	mA
	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	0.7	5	-	0.5	2	μA

Note: Typical parameter is measured under ambient temperature $T_A = 25^\circ \text{C}$ and $V_{DD} = 5V / 3V$.

CAPACITANCE

($V_{DD} = 5V, T_A = 25^\circ \text{C}, f = 1 \text{ MHz}$)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	$V_{IN} = 0V$	6	pF
Input/Output Capacitance	C _{I/O}	$V_{OUT} = 0V$	8	pF

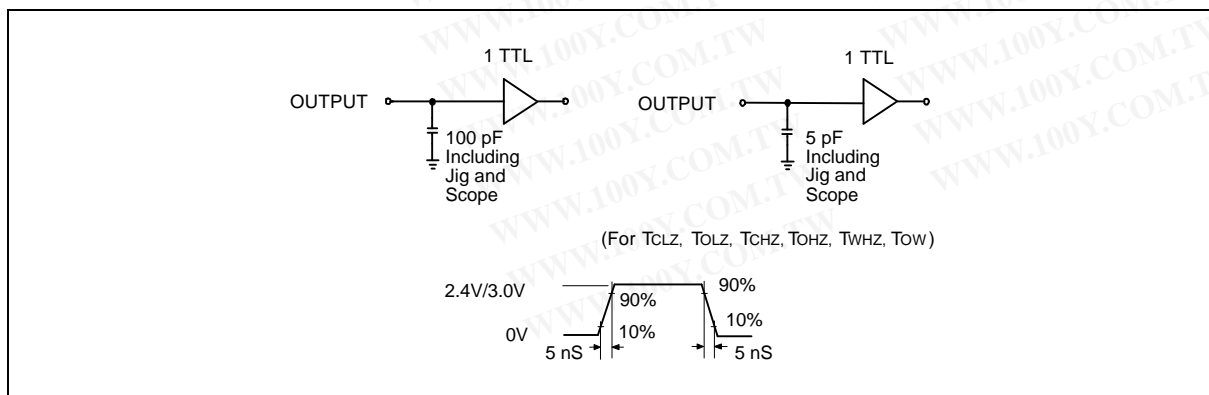
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	$3V \pm 10\%, 0V \text{ to } 2.4V$
	$5V \pm 10\%, 0V \text{ to } 3.0V$
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform



AC Characteristics, continued

(V_{DD} = 5V ±10%; V_{DD} = 3V ±10%; V_{SS} = 0V; T_A (°C) = -20 to 85 for LE; -40 to 85 for LI)

Read Cycle

PARAMETER	SYM.	5V		3V		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	70	-	100	-	nS
Address Access Time	TAA	-	70	-	100	nS
Chip Select Access Time	TACS	-	70	-	100	nS
Output Enable to Output Valid	TAOE	-	35	-	50	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	15	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	30	-	35	nS
Output Disable to Output in High Z	TOHZ*	-	30	-	35	nS
Output Hold from Address Change	TOH	10	-	15	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

PARAMETER	SYM.	5V		3V		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	TWC	70	-	100	-	nS
Chip Selection to End of Write	TCW	50	-	70	-	nS
Address Valid to End of Write	TAW	50	-	70	-	nS
Address Setup Time	TAS	0	-	0	-	nS
Write Pulse Width	TWP	50	-	70	-	nS
Write Recovery Time	\overline{CS} , \overline{WE} TWR	0	-	0	-	nS
Data Valid to End of Write	TDW	30	-	50	-	nS
Data Hold from End of Write	TDH	0	-	0	-	nS
Write to Output in High Z	TWHZ*	-	25	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	25	-	30	nS
Output Active from End of Write	TOW	5	-	10	-	nS

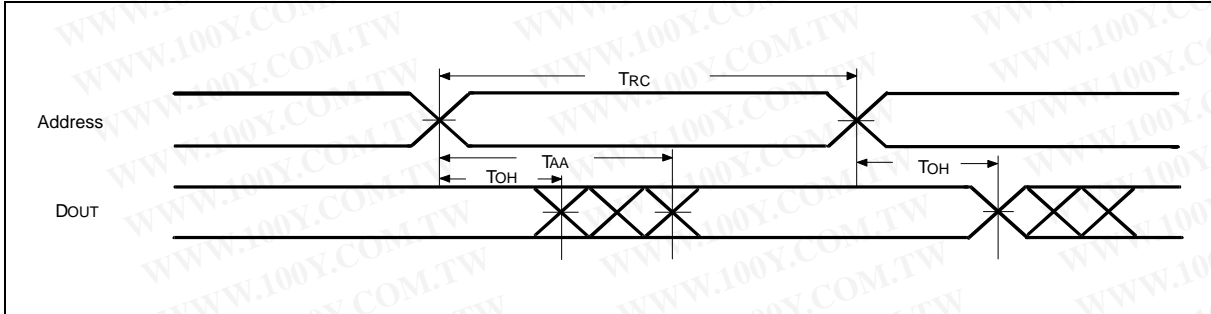
* These parameters are sampled but not 100% tested



TIMING WAVEFORMS

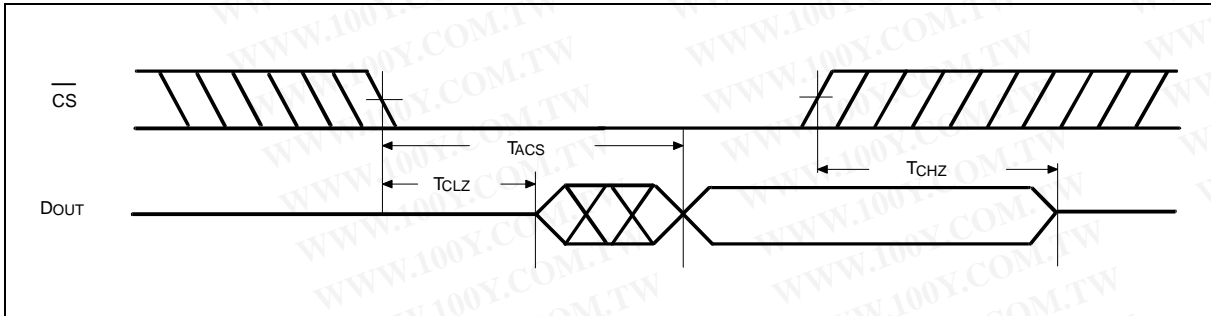
Read Cycle 1

(Address Controlled)



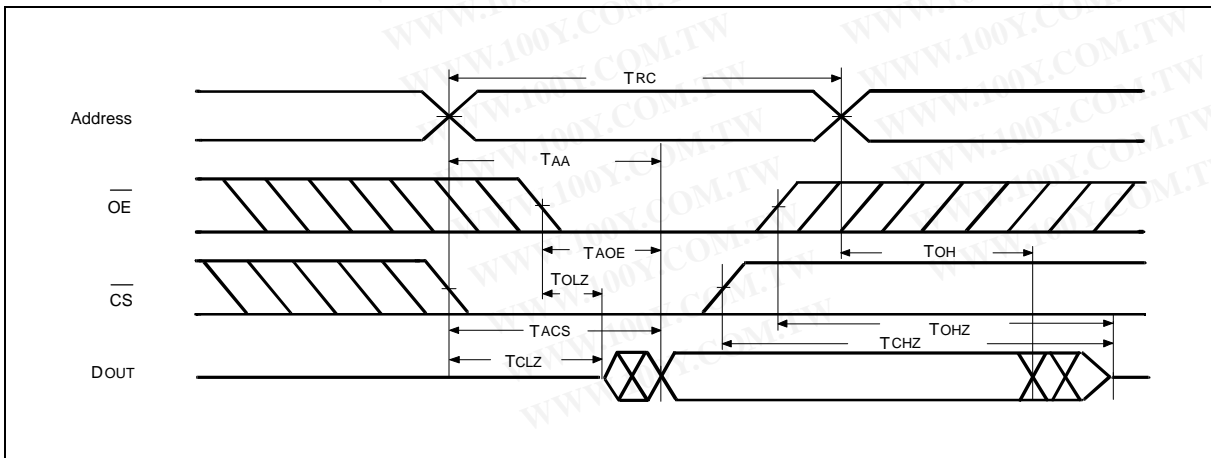
Read Cycle 2

(Chip Select Controlled)



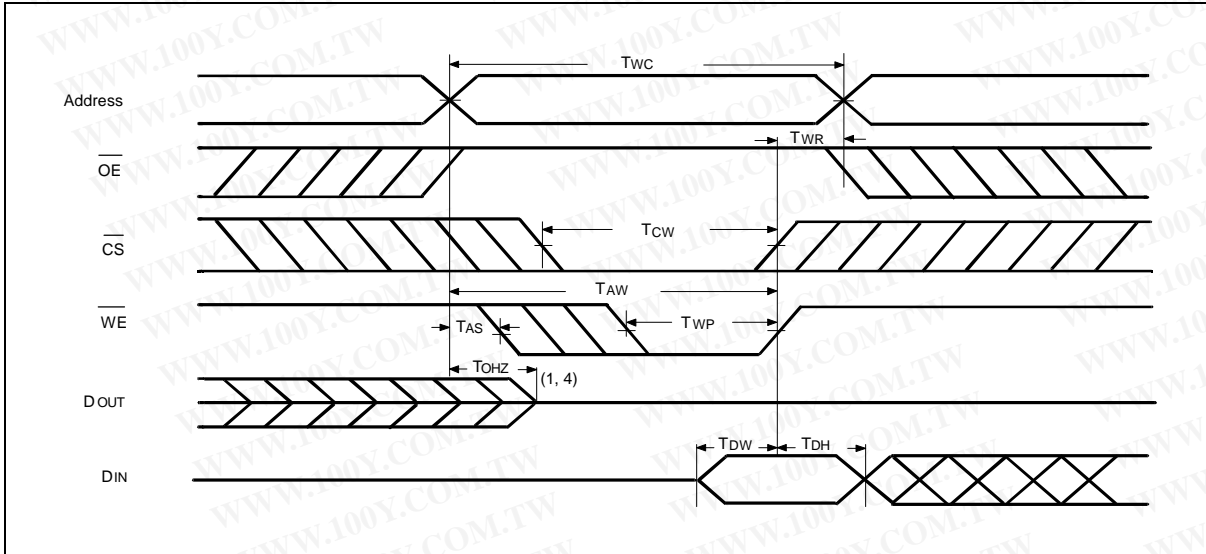
Read Cycle 3

(Output Enable Controlled)



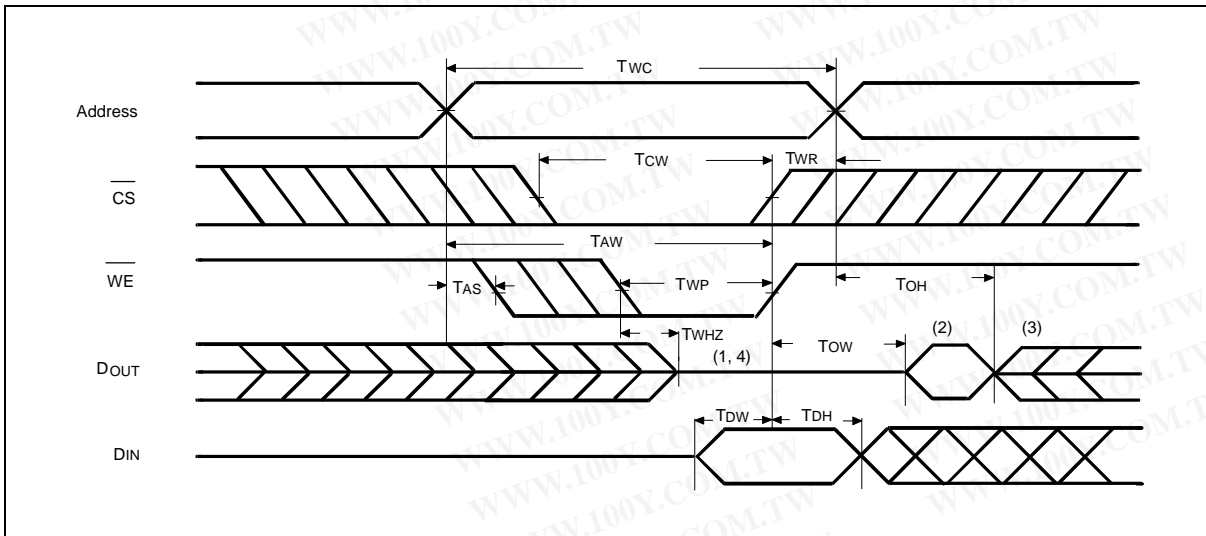
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{\text{OE}} = \text{VIL Fixed}$)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with C_L = 5 pF. This parameter is guaranteed but not 100% tested.

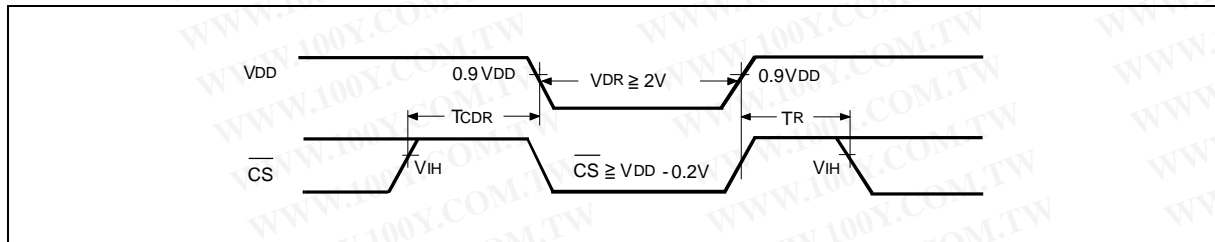
DATA RETENTION CHARACTERISTICS

(TA (°C) = -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{CS} \geq V_{DD} - 0.2V$	2.0	-	-	V
Data Retention Current	I _{DDDR}	$\overline{CS} \geq V_{DD} - 0.2V, V_{DD} = 3V$	-	-	2	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T _R		TRC*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V)	OPERATING TEMPERATURE (°C)	PACKAGE
W24258H	100	3V	0 to 70	Die form
W24258-70LE	70/100	5V/3V	-20 to 85	600 mil DIP
W24258S-70LE	70/100	5V/3V	-20 to 85	330 mil SOP
W24258Q-70LE	70/100	5V/3V	-20 to 85	Standard type one TSOP
W24258-70LI	70/100	5V/3V	-40 to 85	600 mil DIP
W24258S-70LI	70/100	5V/3V	-40 to 85	330 mil SOP
W24258Q-70LI	70/100	5V/3V	-40 to 85	Standard type one TSOP

Notes:

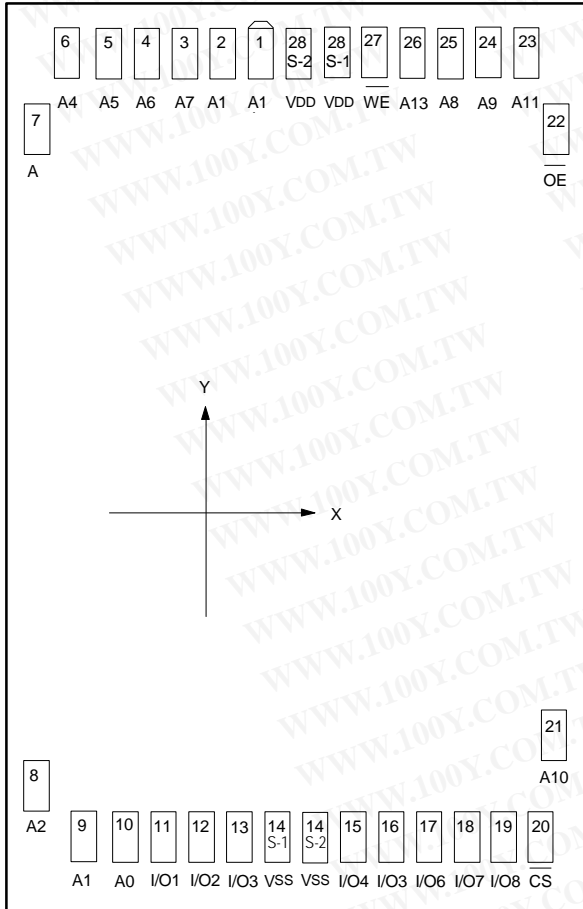
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

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BONDING PAD DIAGRAM

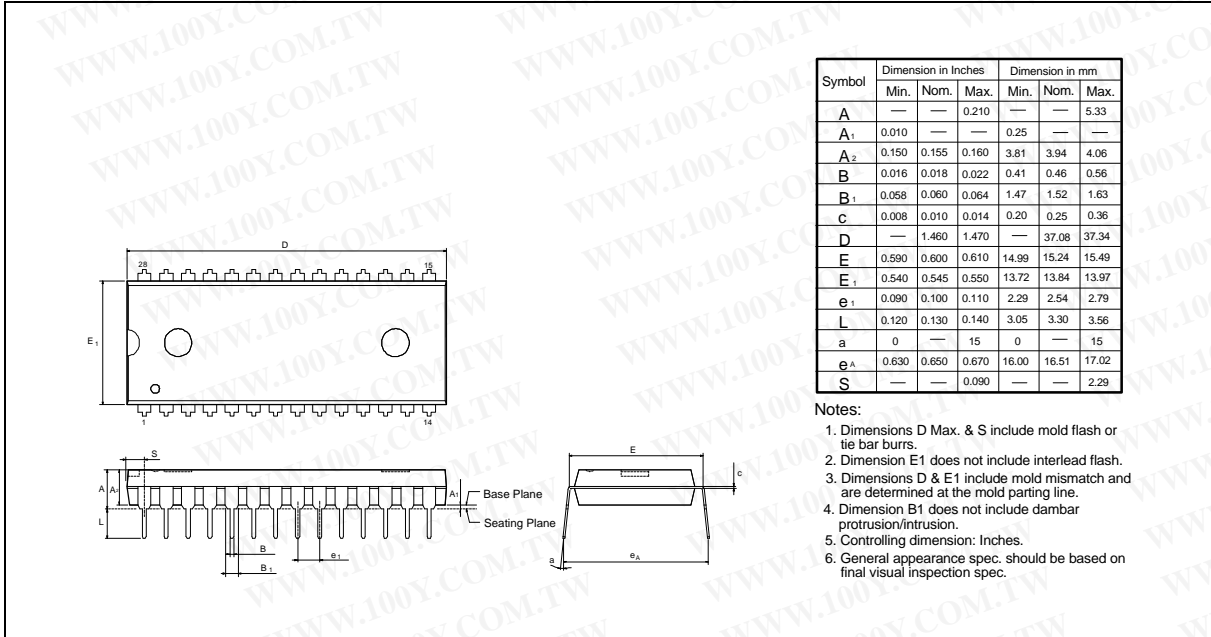


PAD NO.	X	Y
1	-276.73	2047.90
2	-421.97	2047.90
3	-568.93	2047.90
4	-714.17	2047.90
5	-861.13	2047.90
6	-1006.37	2047.90
7	-1190.70	1796.55
8	-1190.70	-1797.65
9	-1023.69	-2049.00
10	-878.45	-2049.00
11	-730.05	-2049.00
12	-584.79	-2049.00
13	-438.69	-2049.00
14S-1	-293.69	-2049.00
14S-2	-152.23	-2049.00
15	-9.22	-2049.00
16	437.42	-2049.00
17	582.68	-2049.00
18	730.42	-2049.00
19	875.68	-2049.00
20	1025.65	-2049.00
21	1189.20	-1797.65
22	1188.70	1796.55
23	1025.68	2047.90
24	878.72	2047.90
25	733.48	2047.90
26	586.52	2047.90
27	441.28	2047.90
28S-1	18.40	2047.90
28S-2	-131.73	2047.90

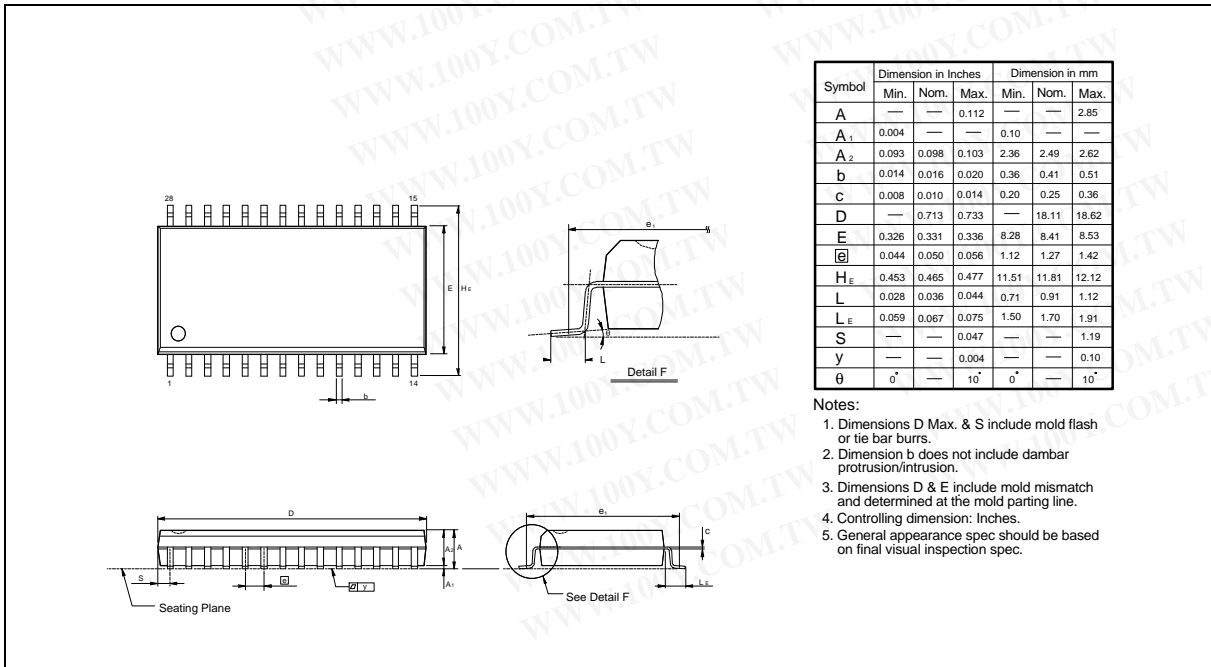
Note: For bare chip form (C.O.B.) applications, the substrate must be connected to VDD or left floating in the PCB layout.

PACKAGE DIMENSIONS

28-pin P-DIP

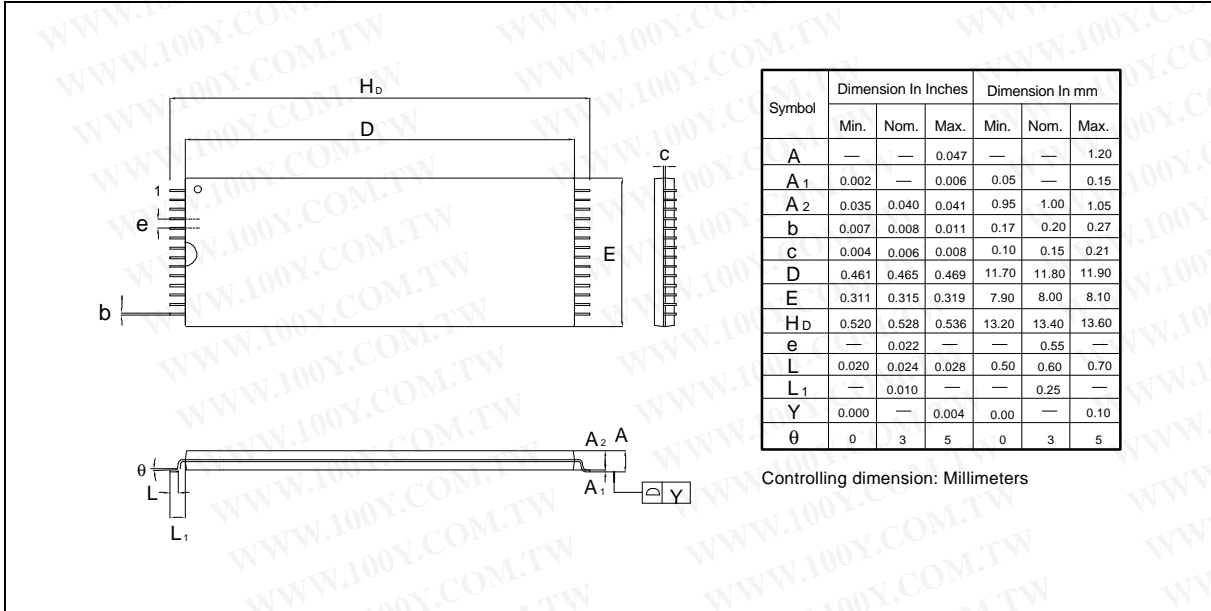


28-pin SOP Wide Body



Package Dimensions, continued

28-pin Standard Type One TSOP



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VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A4	Mar. 1997	8	Add bonding PAD diagram
A5	Jan. 1998	8	Modify bonding PAD diagram
A6	Feb. 1998	1, 2, 4, 7	Delete operating temperature (SL = 0 to 70 °C)
A7	Apr. 1998	3	Add standby power supply current (ISB1) typical parameter when operation temperature TA = 25° C
A8	Nov. 1998	1, 3, 7, 10	Deduct reverse type one TSOP package

