N-Channel 80-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
80	0.0165 at V_{GS} = 10 V	12.5
	0.022 at V_{GS} = 6 V	10.9

FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- PWM Optimized for Fast Switching
- 100 % R_g Tested

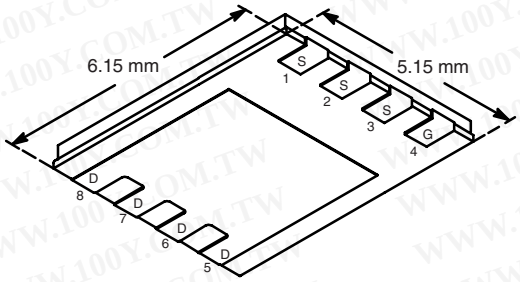
Pb-free Available

RoHS* COMPLIANT

APPLICATIONS

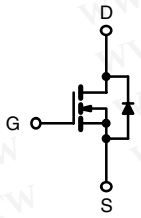
- Primary Side Switch for DC/DC Applications

PowerPAK SO-8



Bottom View

Ordering Information: Si7852DP-T1
Si7852DP-T1-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	80		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	12.5	7.6	A
	T_A = 70 °C		10.0	6.1	
Pulsed Drain Current		I_{DM}	50		
Avalanche Current	L = 0.1 mH	I_{AS}	40		
Continuous Source Current (Diode Conduction)[a]		I_S	4.7	1.7	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	5.2	1.9	W
	T_A = 70 °C		3.3	1.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[b,c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	19	24	°C/W
	Steady State		52	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.5	1.8	

Notes:
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (*http://www.vishay.com/ppg?73257*). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

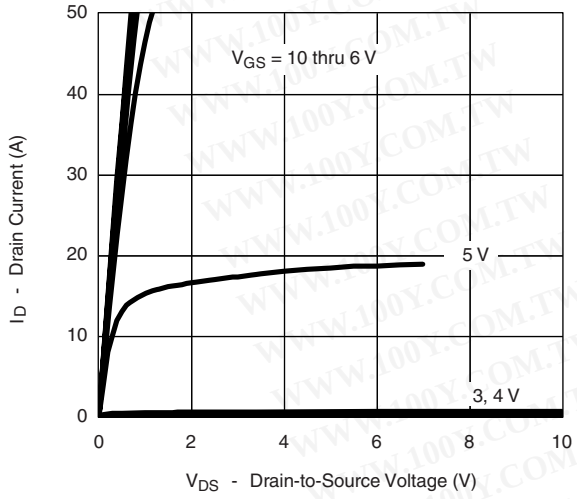
* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55 °C			5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A		0.0135	0.0165	Ω
		V_{GS} = 6.0 V, I_D = 8.0 A		0.0175	0.022	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 10 A		25		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.8 A, V_{GS} = 0 V		0.75	1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 40 V, V_{GS} = 10 V, I_D = 10 A		34	41	nC
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			11.0		
Gate Resistance	R_g		0.1	0.6	1	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 40 Ω $I_D \cong$ 1.0 A, V_{GEN} = 10 V, R_G = 6 Ω		17	25	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	t_f			31	45	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.8 A, di/dt = 100 A/µs		45	75	

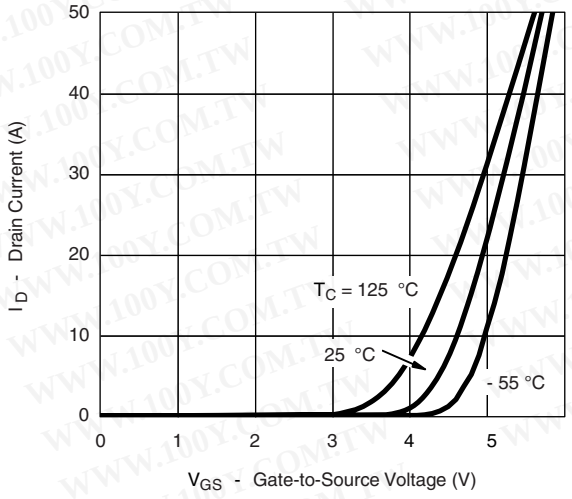
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

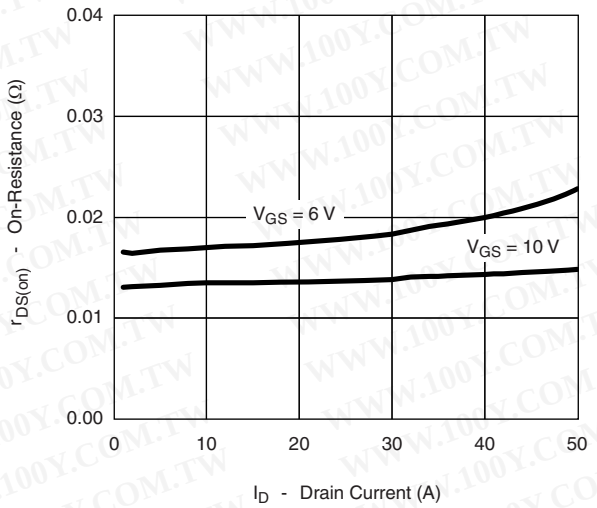


Output Characteristics

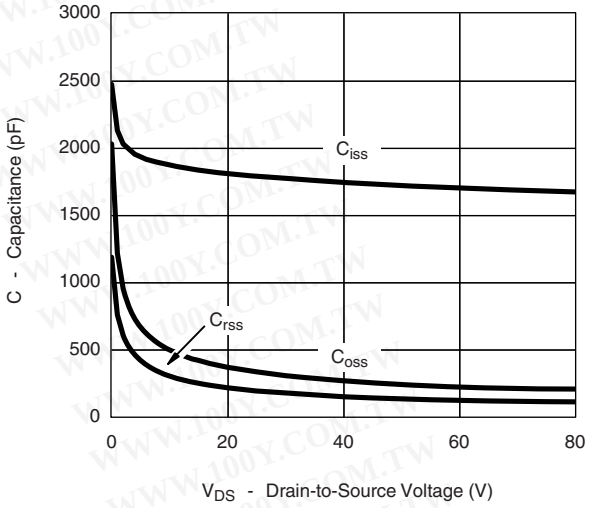


Transfer Characteristics

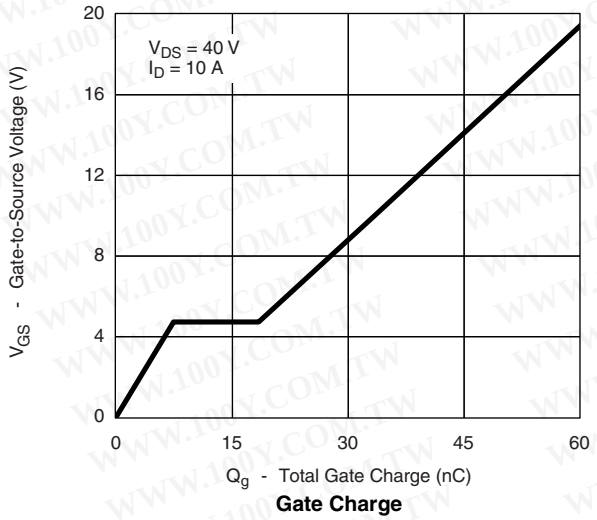
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



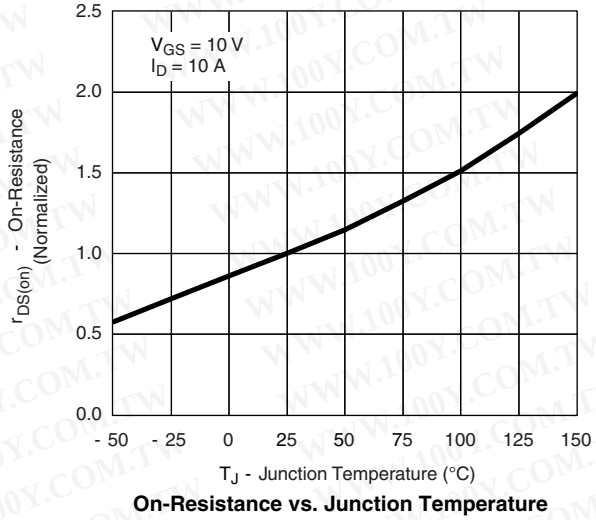
On-Resistance vs. Drain Current



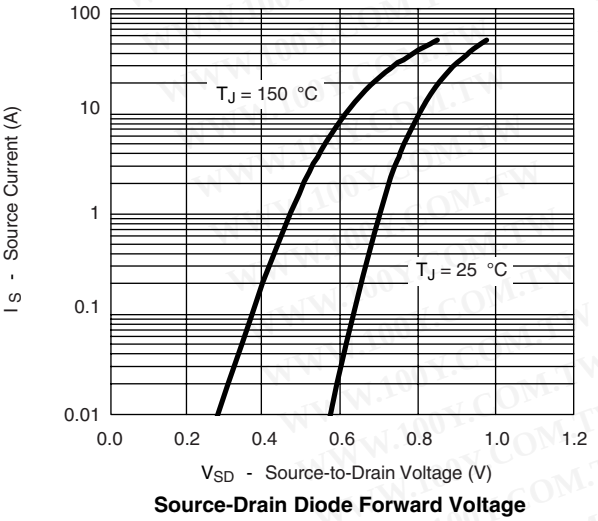
Capacitance



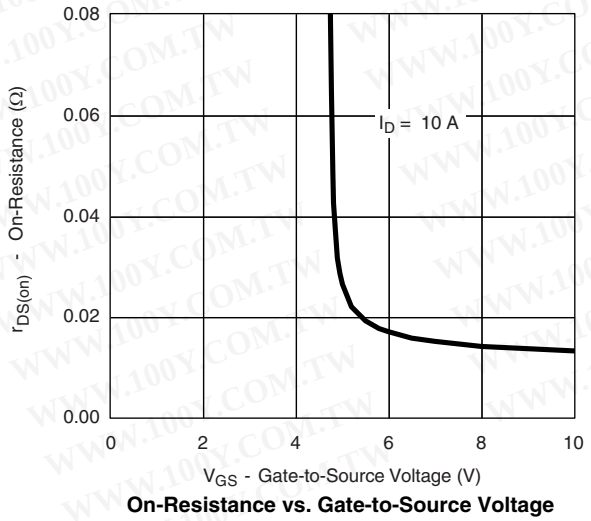
Gate Charge



On-Resistance vs. Junction Temperature

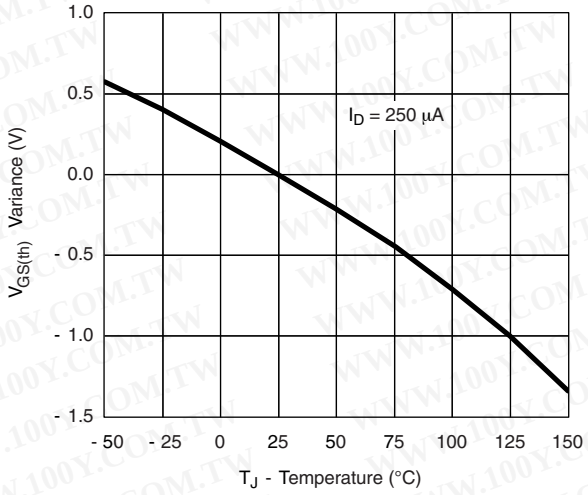


Source-Drain Diode Forward Voltage

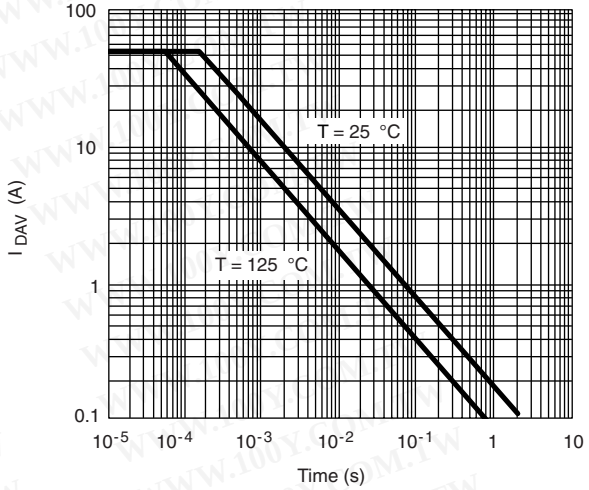


On-Resistance vs. Gate-to-Source Voltage

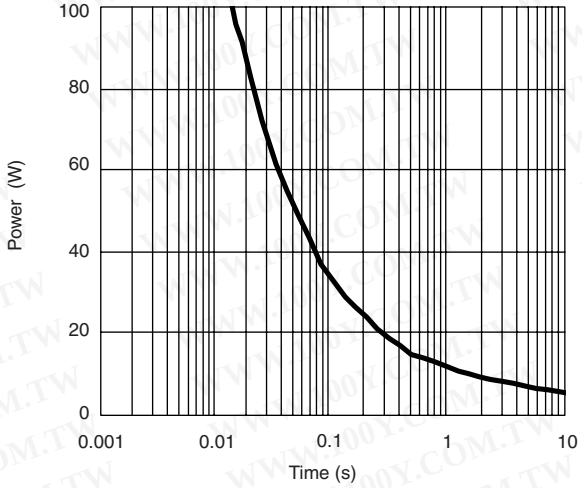
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



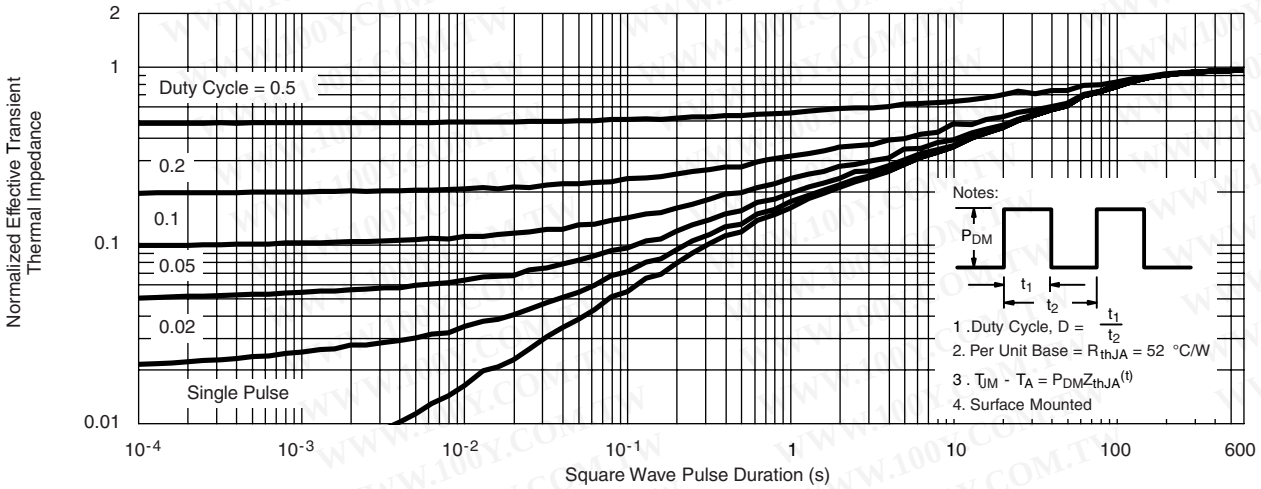
Threshold Voltage



Avalanche Current vs. Time

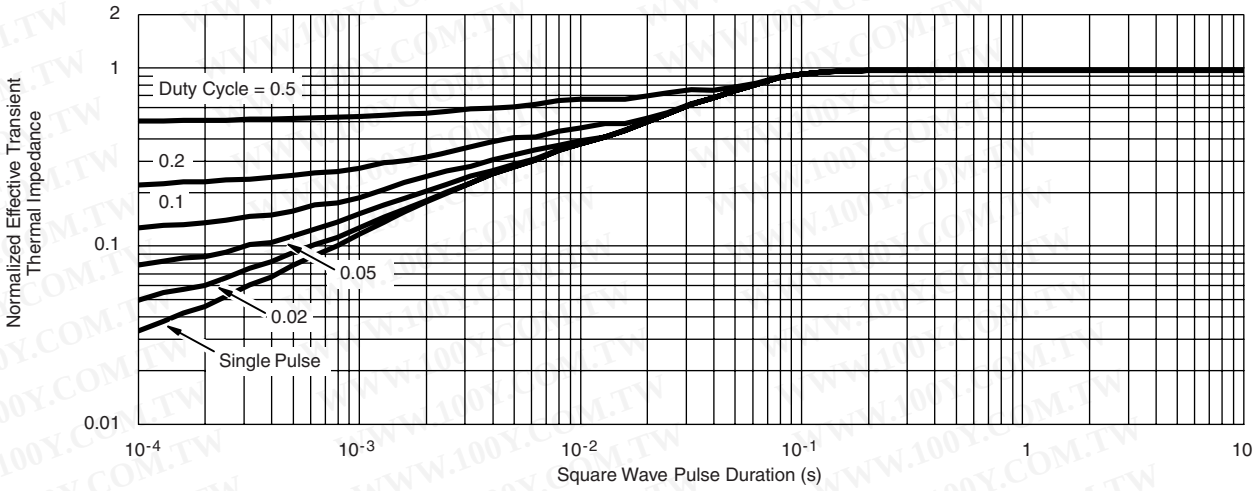


Single Pulse Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

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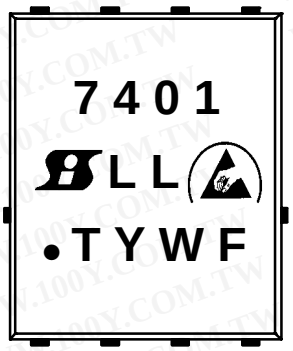
DEVICES: **PowerPAK® SO-8**
PowerPAK® 1212-8

PowerPAK SO-8/1212-8
(Single and Dual)



7401	=	Example Base Part Number
	=	Siliconix Logo
LL	=	Lot Code
	=	ESD Symbol
●	=	Pin 1 Indicator
T	=	Assembly Factory Code
Y	=	Year Code
W	=	Week Code
F	=	Wafer Fab Code

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.