

## Dual Non-Inverting Power Driver

### FEATURES

- 3.0A Peak Current Totem Pole Output
- 5 to 35V Operation
- 25ns Rise and Fall Times
- 25ns Propagation Delays
- Thermal Shutdown and Under-Voltage Protection
- High-Speed, Power MOSFET Compatible
- Efficient High Frequency Operation
- Low Cross-Conduction Current Spike
- Enable and Shutdown Functions
- Wide Input Voltage Range
- ESD Protection to 2kV

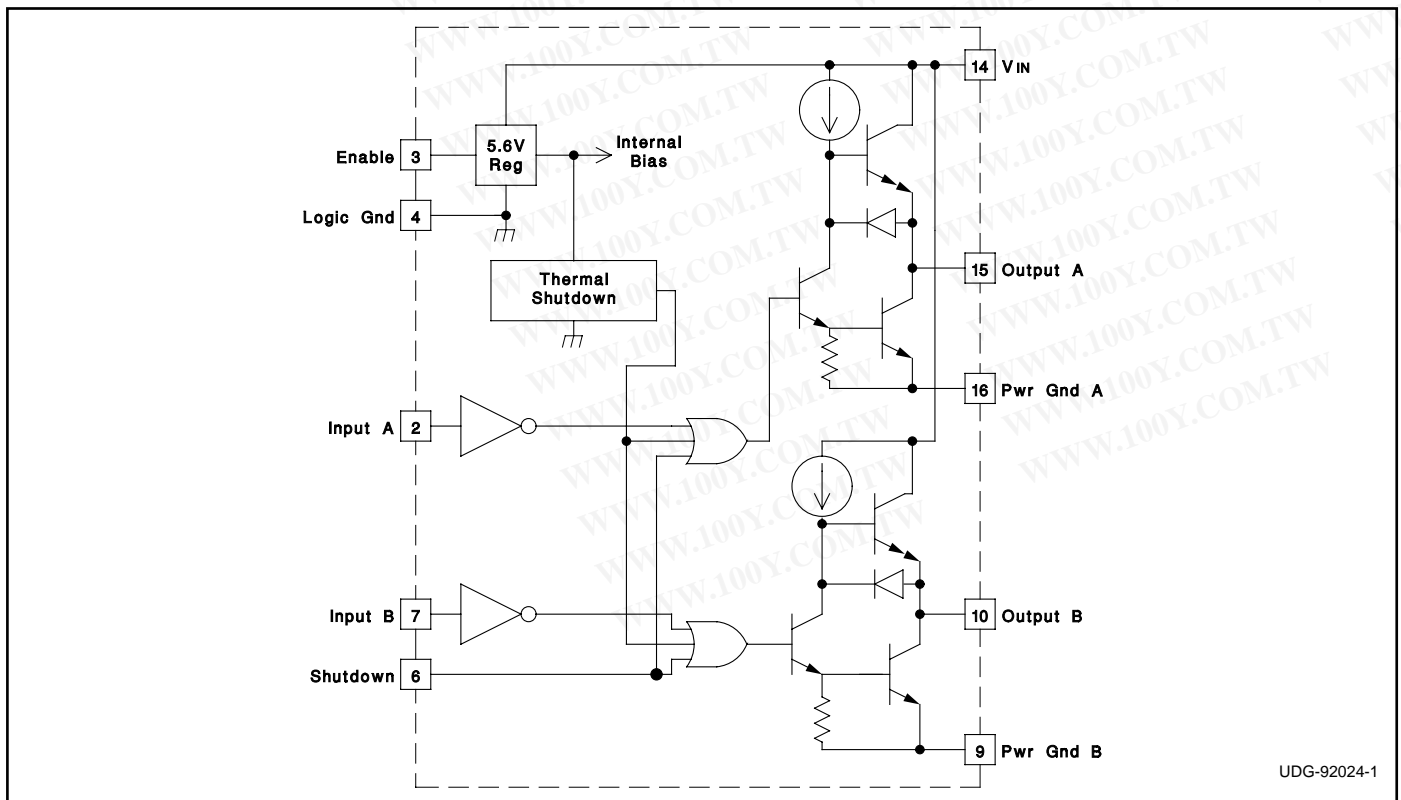
### DESCRIPTION

The UC1708 family of power drivers is made with a high-speed, high-voltage, Schottky process to interface control functions and high-power switching devices – particularly power MOSFETs. Operating over a 5 to 35 volt supply range, these devices contain two independent channels. The A and B inputs are compatible with TTL and CMOS logic families, but can withstand input voltages as high as  $V_{IN}$ . Each output can source or sink up to 3A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, they can be forced low in common through the action of either a digital high signal at the Shutdown terminal or by forcing the Enable terminal low. The Shutdown terminal will only force the outputs low, it will not effect the behavior of the rest of the device. The Enable terminal effectively places the device in under-voltage lockout, reducing power consumption by as much as 90%. During under-voltage and disable (Enable terminal forced low) conditions, the outputs are held in a self-biasing, low-voltage, state.

The UC3708 and UC2708 are available in plastic 8-pin MINI DIP and 16-pin “bat-wing” DIP packages for commercial operation over a  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  temperature range and industrial temperature range of  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  respectively. For operation over a  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range, the UC1708 is available in hermetically sealed 8-pin MINI CDIP, 16 pin CDIP and 20 pin CLCC packages. Surface mount devices are also available.

### BLOCK DIAGRAM



Note: Shutdown feature is not available in J or N packages only.

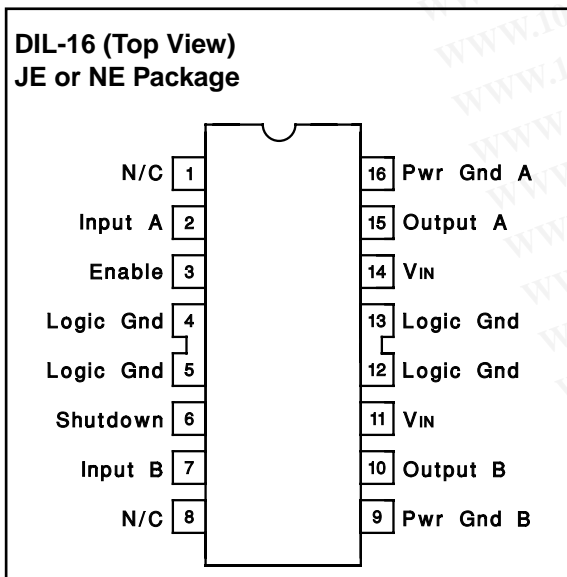
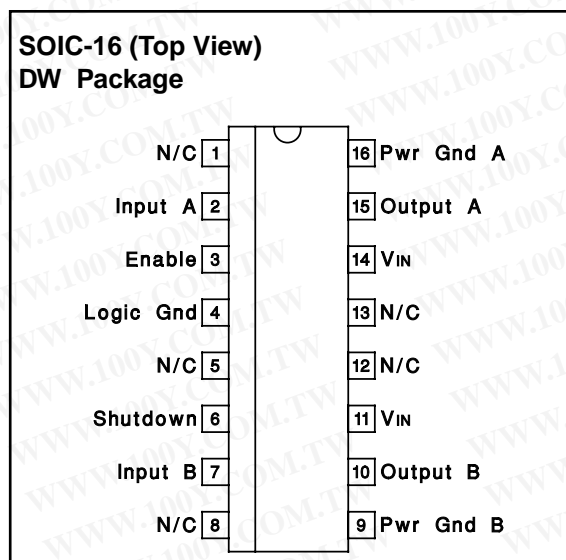
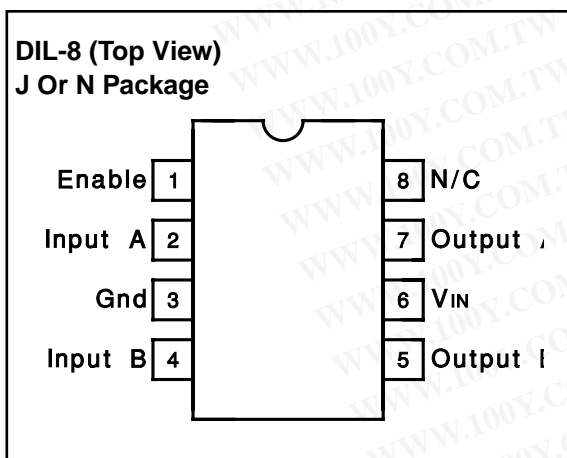
### ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage $V_{IN}$ .....	35V
Output Current (Each Output, Source or Sink)	
Steady-State .....	0.5A
Peak Transient .....	3A
Output Voltage .....	-0.3 to $(V_{IN} + 0.3)V$
Enable and Shutdown Inputs .....	-0.3 to 6.2V
A and B Inputs .....	-0.3 to $(V_{IN} + 0.3)V$
Operating Junction Temperature (Note 2) .....	150°C
Storage Temperature Range .....	-65° to 150°C
Lead Temperature (Soldering, 10 Seconds) .....	300°C

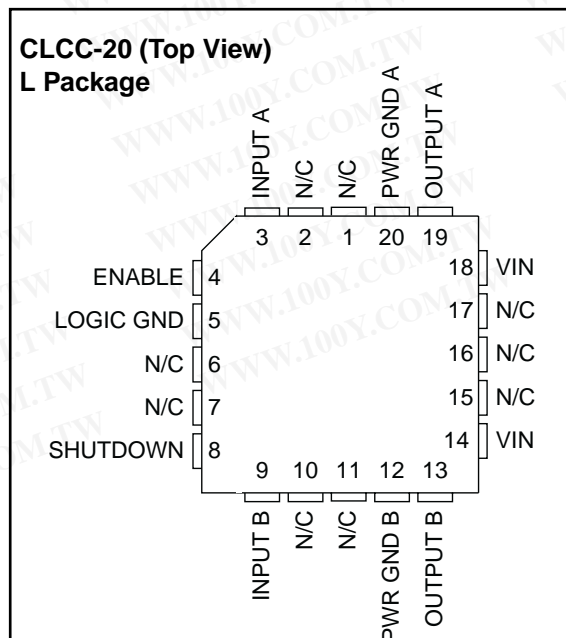
NOTE 1: All voltages are with respect to Logic Gnd pin. All currents are positive into, negative out of, device terminals.

NOTE 2: Consult Unitorde Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

### CONNECTION DIAGRAMS



Note: In JE package Pin 4 is logic ground. Pins 5, 12, and 13 are N/C.



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated,  $V_{IN}=10V$  to  $35V$ , and these specifications apply for:  $-55^{\circ}C < T_A < 125^{\circ}C$  for the UC1708,  $-25^{\circ}C < T_A < +85^{\circ}C$  for the UC2708, and  $0^{\circ}C < T_A < 70^{\circ}C$  for the UC3708.  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN Supply Current	Outputs Low		18	26	mA
	Outputs High		14	18	mA
	Enable = 0V		1	4	mA
A, B and Shutdown Inputs Low Level				0.8	V
A, B and Shutdown Inputs High Level		2.0			V
A, B Input Current Low	$V_{A,B} = 0.4V$	-1	-0.6		mA
A, B Input Current High	$V_{A,B} = 2.4V$	-200		50	$\mu A$
A, B Input Leakage Current High	$V_{A,B} = 35.3V$			200	$\mu A$
Shutdown Input Current Low	$V_{SHUTDOWN} = 0.4V$		20	100	$\mu A$
Shutdown Input Current High	$V_{SHUTDOWN} = 2.4V$		170	500	$\mu A$
	$V_{SHUTDOWN} = 6.2V$		0.6	1.5	mA
Enable Input Current Low	$V_{ENABLE} = 0V$	-600	-460	200	$\mu A$
Enable Input Current High	$V_{ENABLE} = 6.2V$			200	$\mu A$
Enable Threshold Rising			2.8	3.6	V
Enable Threshold Falling		1.0	2.4	3.4	V
Output High Sat., $V_{IN} - V_{OUT}$	$I_{OUT} = -50mA$			2.0	V
	$I_{OUT} = -500mA$			2.5	V
Output Low Sat., $V_{OUT}$	$I_{OUT} = 50mA$			0.5	V
	$I_{OUT} = 500mA$			2.5	V
Thermal Shutdown			155		$^{\circ}C$

**SWITCHING CHARACTERISTICS (Figure 1),** ( $V_{IN} = 20V$ , delays measured to 10% output change.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>From A,B Input to Output:</b>					
Rise Time Delay (TPLH)	$CL = 0pF$		25	40	ns
	$CL = 1000pF$ (Note 3)		25	40	ns
	$CL = 2200pF$		30	45	ns
10% to 90% Rise (TTLH)	$CL = 0pF$		55	75	ns
	$CL = 1000pF$ (Note 3)		25	50	ns
	$CL = 2200pF$		40	55	ns
Fall Time Delay (TPHL)	$CL = 0pF$		25	40	ns
	$CL = 1000pF$ (Note 3)		25	45	ns
	$CL = 2200pF$		35	50	ns
90% to 10% Fall (TTHL)	$CL = 0pF$		15	20	ns
	$CL = 1000pF$ (Note 3)		25	45	ns
	$CL = 2200pF$		40	55	ns

NOTE 3: These parameters, specified at 1000pF, although ensured over recommended operating conditions, are not tested in production.

**SWITCHING CHARACTERISTICS (Figure 1),** ( $V_{IN} = 20V$ , delays measured to 10% output change.)

From Shutdown Input to Output					
Rise Time Delay (T <sub>PLH</sub> )	CL = 0pF		25	75	ns
	CL = 1000pF (Note 3)		30	75	ns
	CL = 2200pF		35	75	ns
10% to 90% Rise (T <sub>T LH</sub> )	CL = 0pF		50	75	ns
	CL = 1000pF (Note 3)		25	50	ns
	CL = 2200pF		40	55	ns
Fall Time Delay (T <sub>PHL</sub> )	CL = 0pF		25	45	ns
	CL = 1000pF (Note 3)		30	50	ns
	CL = 2200pF		35	55	ns
90% to 10% Fall (T <sub>T HL</sub> )	CL = 0pF		25	20	ns
	CL = 1000pF (Note 3)		25	45	ns
	CL = 2200pF		40	55	ns
Total Supply Current	F = 200kHz, 50% duty cycle, both channels; CL = 0pF		23	25	mA
	F = 200kHz, 50% duty cycle, both channels; CL = 2200pF		38	45	mA

NOTE 3: These parameters, specified at 1000pF, although ensured over recommended operating conditions, are not tested in production.

Figure 1: AC Test Circuit and Switching Time Waveforms

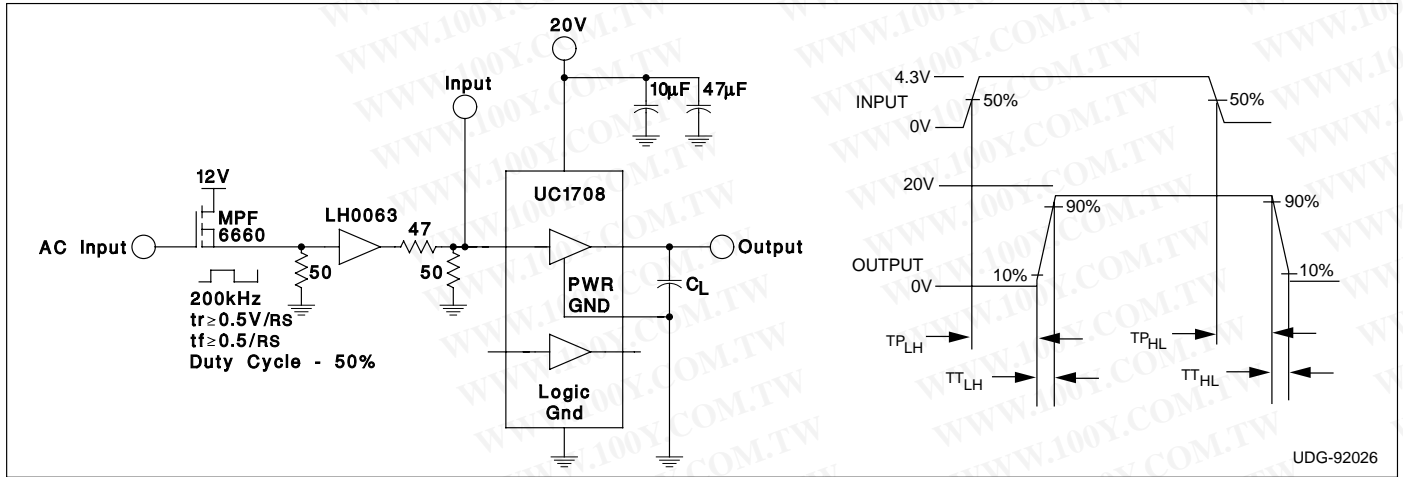
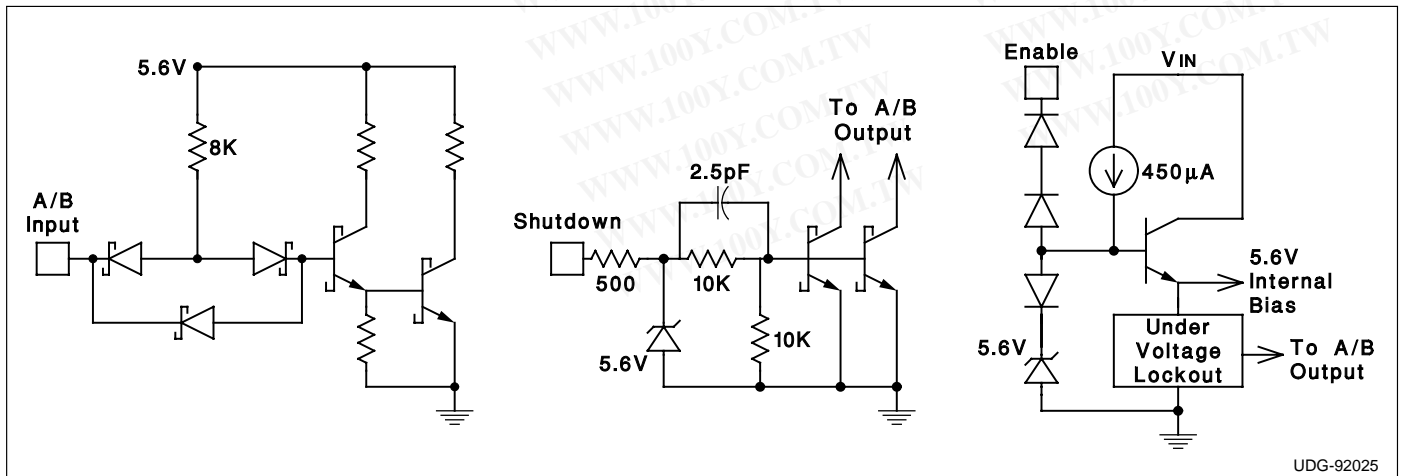


Figure 2: Equivalent Input Circuits



Note: Shutdown feature available only in JE, NE or DW Packages.

PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-0051401Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-0051401QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-0051401QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
5962-0051401V2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
5962-0051401VEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type
5962-0051401VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1708J	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
UC1708J883B	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
UC1708JE	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1708JE883B	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1708L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC2708D	OBSOLETE		UTR			TBD	Call TI	Call TI
UC2708DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2708DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2708DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2708DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2708J	OBSOLETE		UTR			TBD	Call TI	Call TI
UC2708JE	OBSOLETE		UTR			TBD	Call TI	Call TI
UC2708N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2708NE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2708NEG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2708NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2708Q	OBSOLETE		UTR			TBD	Call TI	Call TI
UC3708DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3708DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3708DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3708DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3708J	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
UC3708JE	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC3708N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3708NE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3708NEG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
						no Sb/Br)		
UC3708NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3708Q	OBSOLETE		UTR			TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

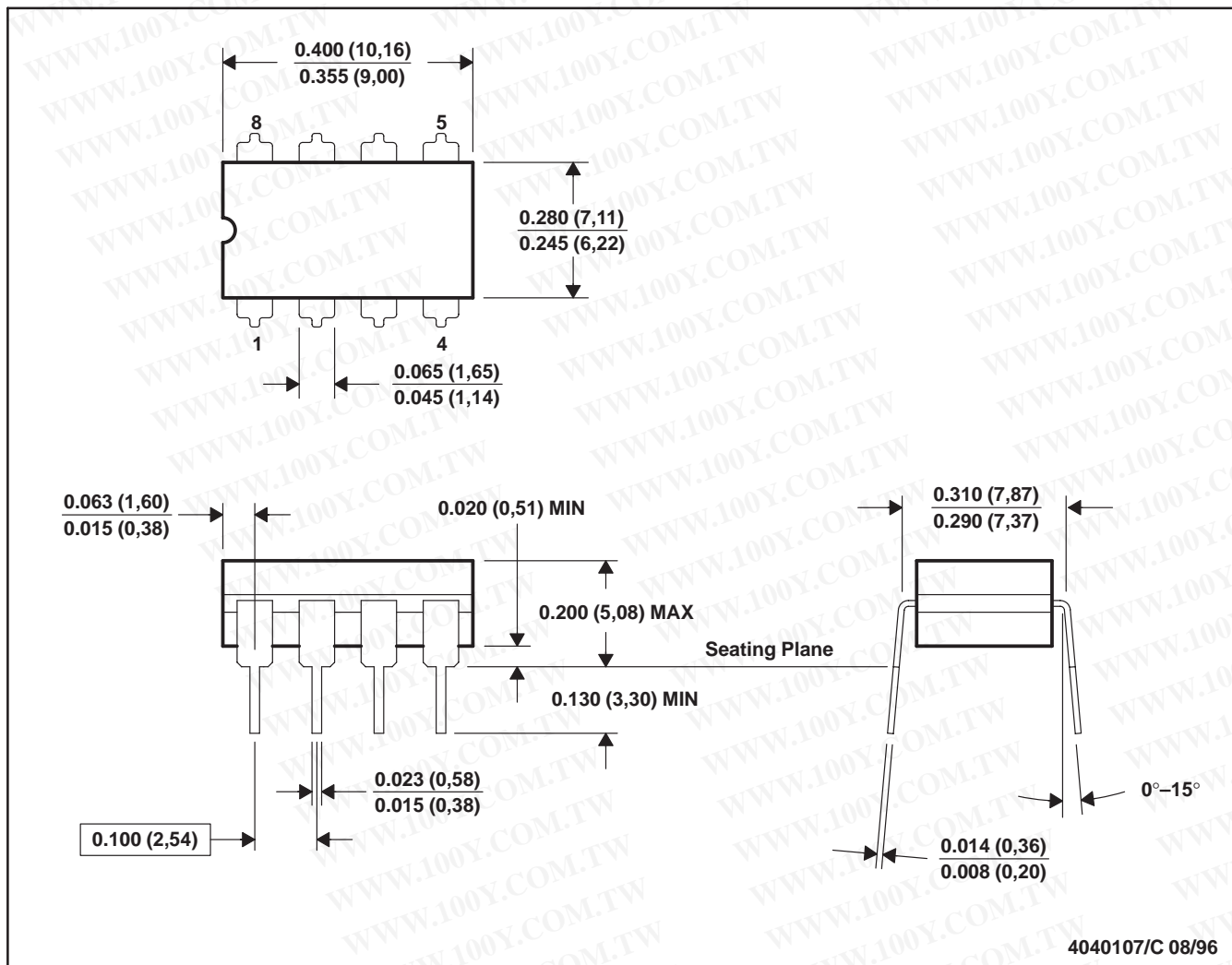
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## JG (R-GDIP-T8)

## CERAMIC DUAL-IN-LINE



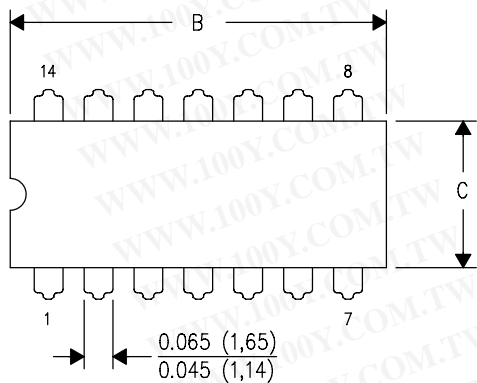
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

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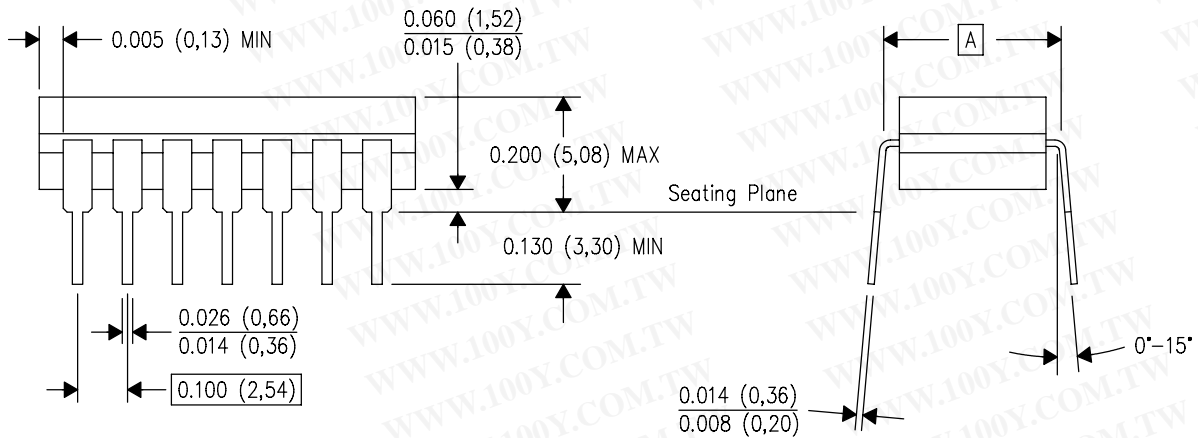
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J (R-GDIP-T\*\*)  
 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
	A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



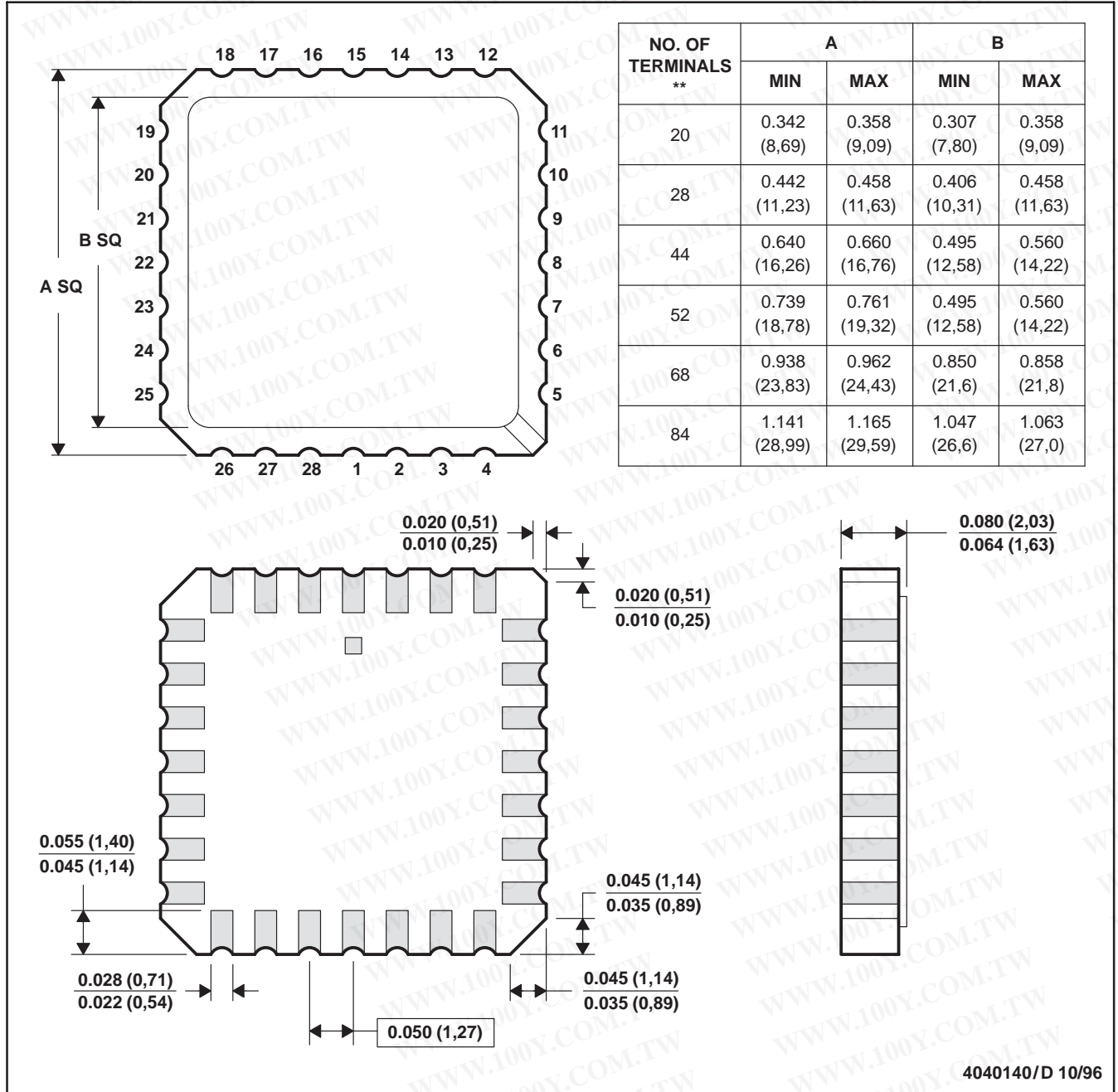
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

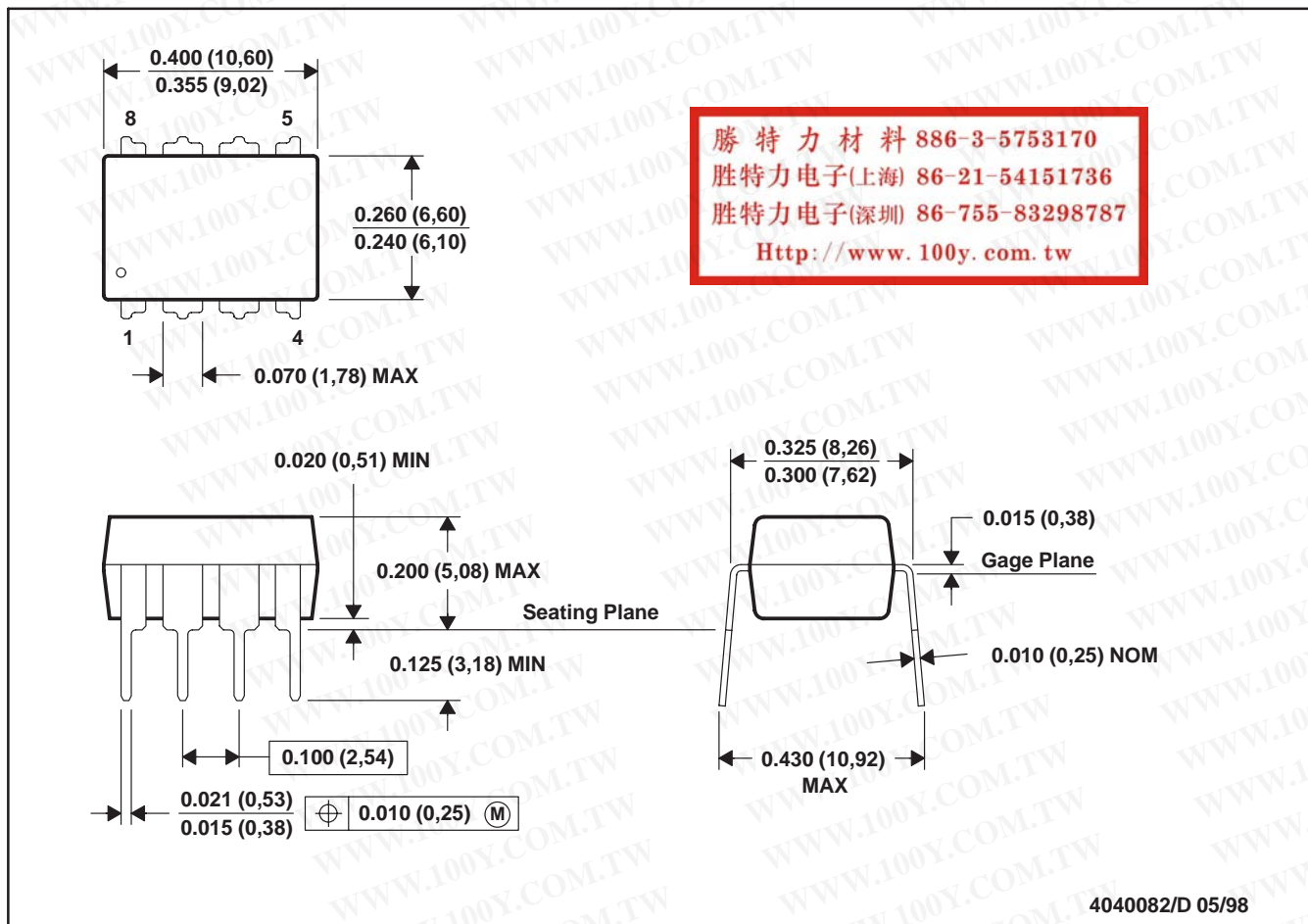
28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



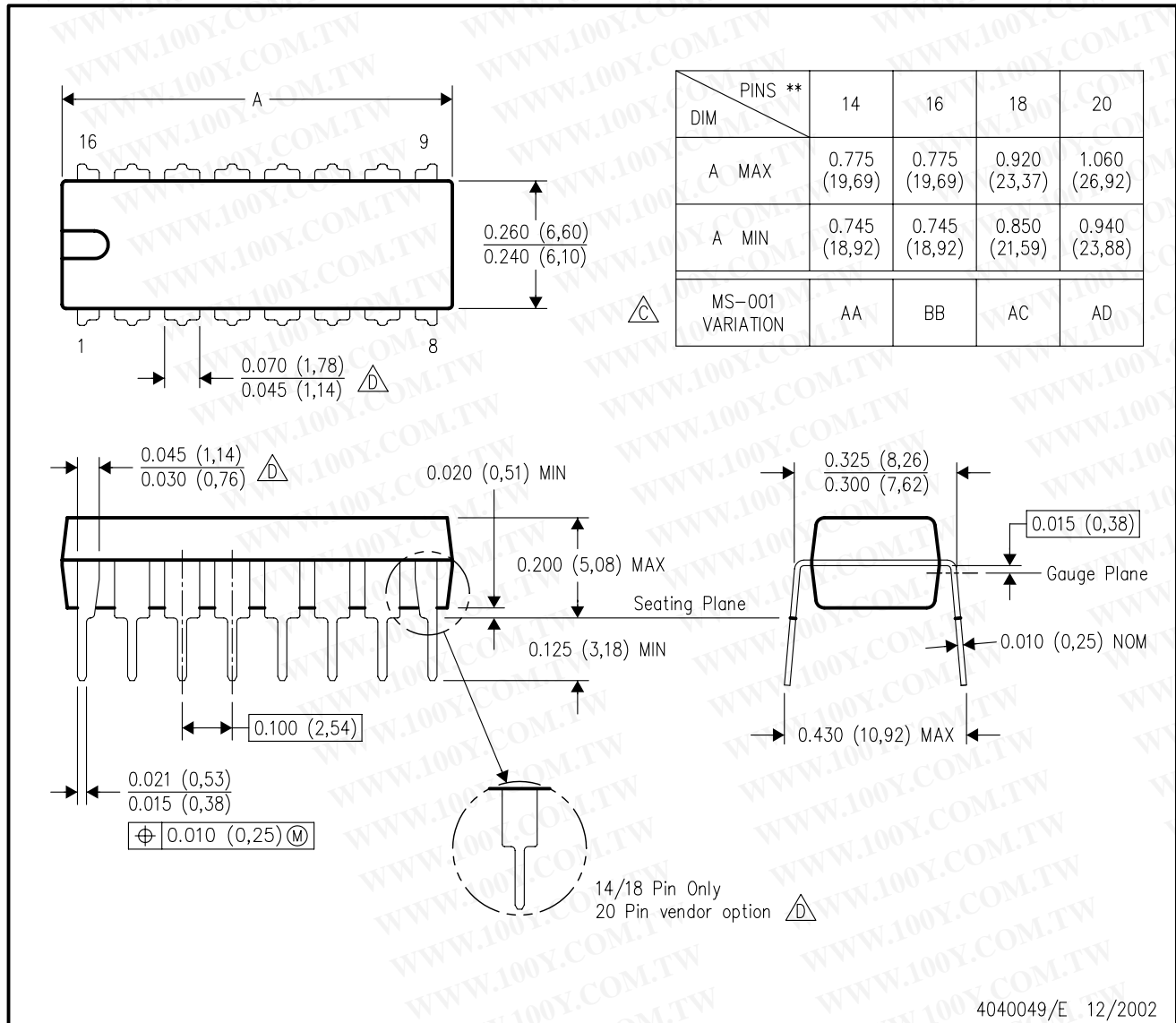
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

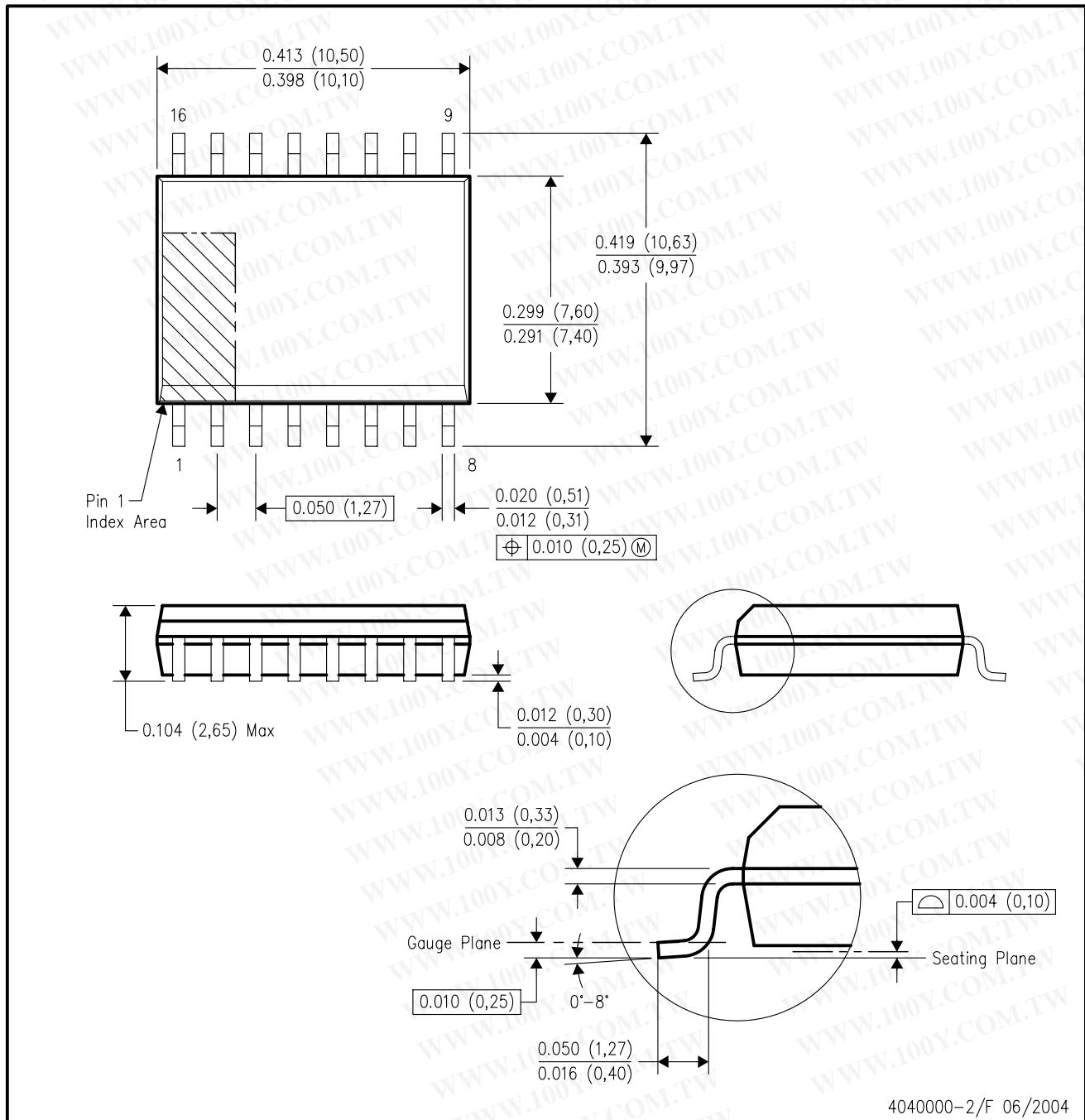
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.