- **Programmable Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$**
- **In Auto-$\overline{\text{CTS}}$ Mode, $\overline{\text{CTS}}$ Controls Transmitter**
- **In Auto-$\overline{\text{RTS}}$ Mode, RCV FIFO Contents and Threshold Control $\overline{\text{RTS}}$**
- **Serial and Modem Control Outputs Drive a RJ11 Cable Directly When Equipment Is on the Same Power Drop**
- **Capable of Running With All Existing TL16C450 Software**
- **After Reset, All Registers Are Identical to the TL16C450 Register Set**
- **Up to 16-MHz Clock Rate for Up to 1-Mbaud Operation**
- **In the TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data**
- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to (2^{16} – 1) and Generates an Internal 16× Clock**
- **Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream**
- **Independent Receiver Clock Input**
- **Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (dc to 1 Mbit/s)**
- **False-Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **3-State Output TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, and Framing Error Simulation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$)**

description

The TL16C550C is a functional upgrade of the TL16C550B asynchronous communications element (ACE), which in turn is a functional upgrade of the TL16C450. Functionally equivalent to the TL16C450 on power up (character or TL16C450 mode), the TL16C550C, like the TL16C550B, can be placed in an alternate mode (FIFO mode). This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO. In the FIFO mode, there is a selectable autoflow control feature that can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow using $\overline{\text{RTS}}$ output and $\overline{\text{CTS}}$ input signals.

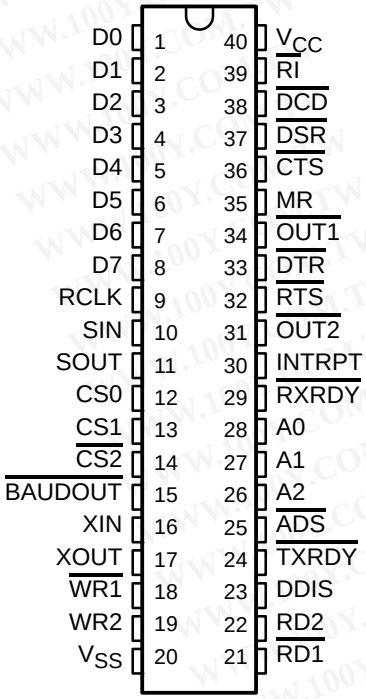
The TL16C550C performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read the ACE status at any time. The ACE includes complete modem control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The TL16C550C ACE includes a programmable baud rate generator capable of dividing a reference clock by divisors from 1 to 65535 and producing a 16× reference clock for the internal transmitter logic. Provisions are included to use this 16× clock for the receiver logic. The ACE accommodates a 1-Mbaud serial rate (16-MHz input clock) so that a bit time is 1 µs and a typical character time is 10 µs (start bit, 8 data bits, stop bit).

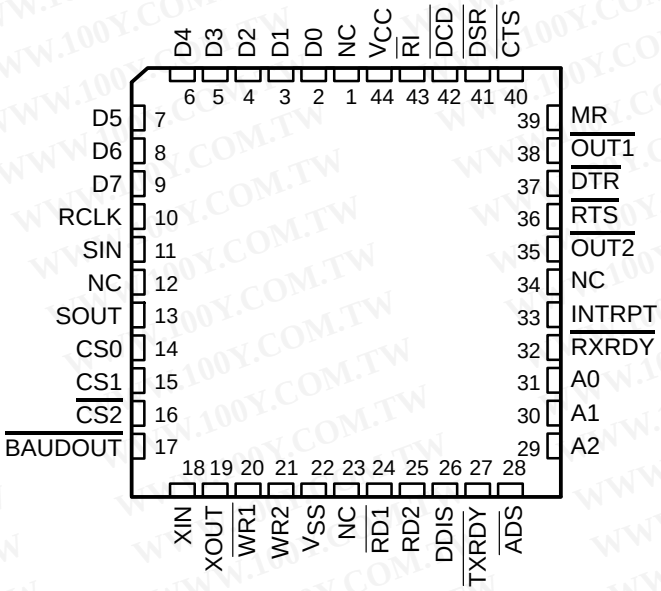
Two of the TL16C450 terminal functions on the TL16C550C have been changed to $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$, which provide signaling to a DMA controller.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

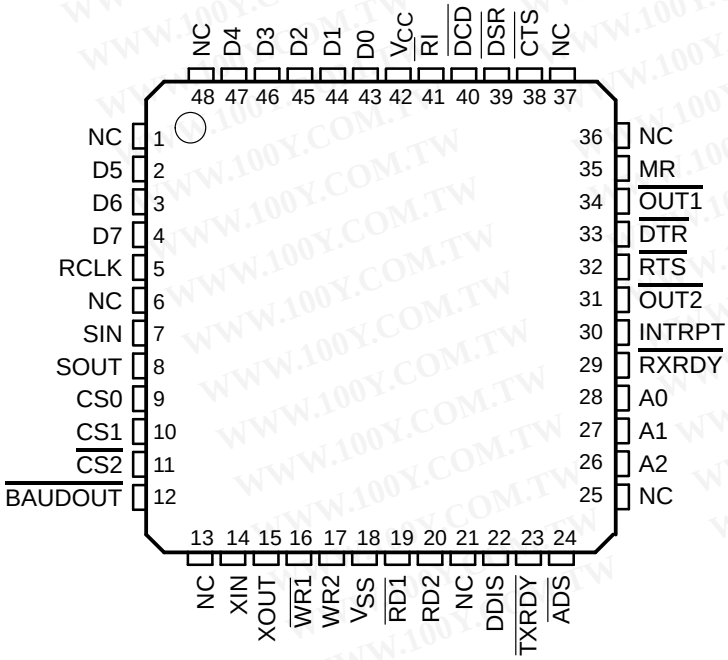
N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

detailed description

autoflow control

Auto-flow control is comprised of auto-$\overline{CTS}$ and auto-$\overline{RTS}$. With auto-$\overline{CTS}$, the $\overline{CTS}$ input must be active before the transmitter FIFO can emit data (see Figure 1). With auto-$\overline{RTS}$, $\overline{RTS}$ becomes active when the receiver needs more data and notifies the sending serial device (see Figure 1). When $\overline{RTS}$ is connected to $\overline{CTS}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using ACE1 and ACE2 from a TLC16C550C with the autoflow control enabled. If not, overrun errors occur when the transmit data rate exceeds the receiver FIFO read latency.

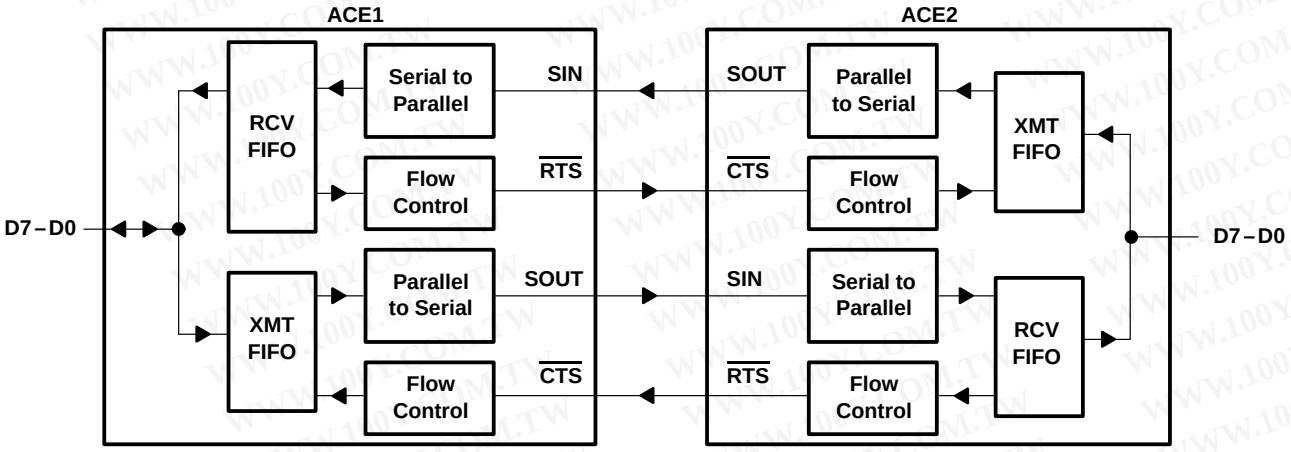


Figure 1. Autoflow Control (Auto-$\overline{RTS}$ and Auto-$\overline{CTS}$) Example

auto-$\overline{RTS}$ (see Figure 1)

Auto-$\overline{RTS}$ data flow control originates in the receiver timing and control block (see functional block diagram) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches a trigger level of 1, 4, or 8 (see Figure 3), $\overline{RTS}$ is deasserted. With trigger levels of 1, 4, and 8, the sending ACE may send an additional byte after the trigger level is reached (assuming the sending ACE has another byte to send) because it may not recognize the deassertion of $\overline{RTS}$ until after it has begun sending the additional byte. $\overline{RTS}$ is automatically reasserted once the RCV FIFO is emptied by reading the receiver buffer register.

When the trigger level is 14 (see Figure 6), $\overline{RTS}$ is deasserted after the first data bit of the 16th character is present on the SIN line. $\overline{RTS}$ is reasserted when the RCV FIFO has at least one available byte space.

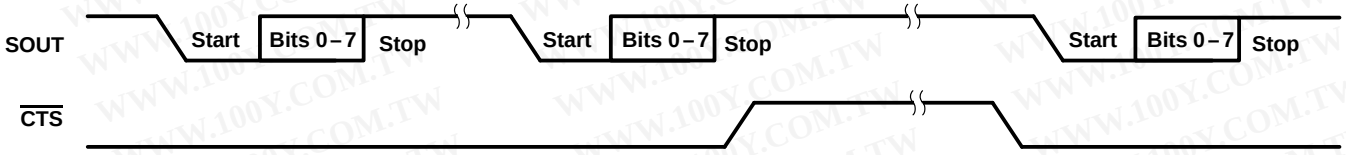
auto-$\overline{CTS}$ (see Figure 1)

The transmitter circuitry checks $\overline{CTS}$ before sending the next data byte. When $\overline{CTS}$ is active, it sends the next byte. To stop the transmitter from sending the following byte, $\overline{CTS}$ must be released before the middle of the last stop bit that is currently being sent (see Figure 2). The auto-$\overline{CTS}$ function reduces interrupts to the host system. When flow control is enabled, $\overline{CTS}$ level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{CTS}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.

enabling autoflow control and auto-$\overline{CTS}$

Auto-flow control is enabled by setting modem control register bits 5 (autoflow enable or AFE) and 1 (RTS) to 1. Auto-flow incorporates both auto-$\overline{RTS}$ and auto-$\overline{CTS}$. When only auto-$\overline{CTS}$ is desired, bit 1 in the modem control register should be cleared (this assumes that a control signal is driving $\overline{CTS}$).

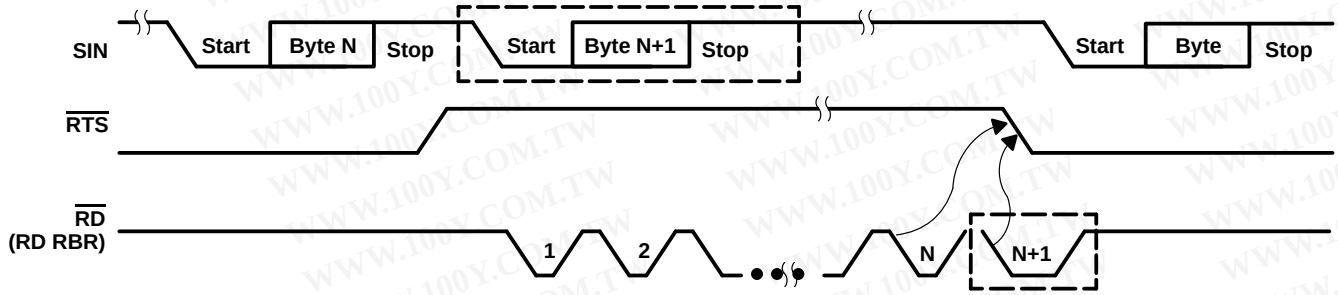
auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$ functional timing



NOTES: A. When $\overline{\text{CTS}}$ is low, the transmitter keeps sending serial data out.
B. If $\overline{\text{CTS}}$ goes high before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte but it does not send the next byte.
C. When $\overline{\text{CTS}}$ goes from high to low, the transmitter begins sending data again.

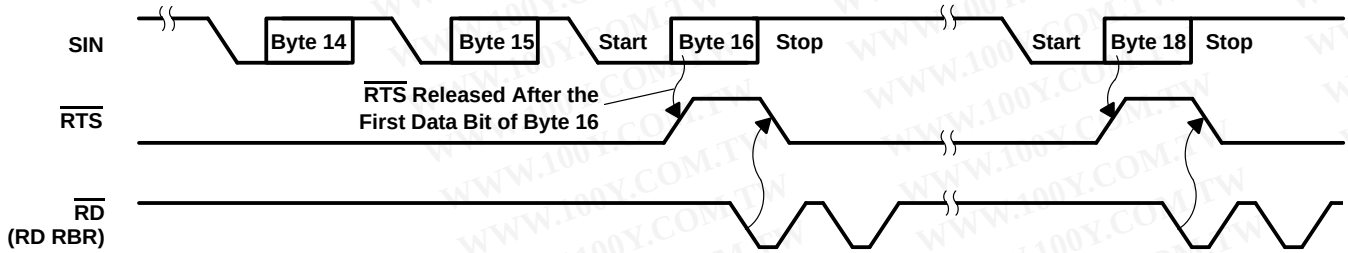
Figure 2. $\overline{\text{CTS}}$ Functional Timing Waveforms

The receiver FIFO trigger level can be set to 1, 4, 8, or 14 bytes. These are described in Figures 3 and 4.



NOTES: A. N = RCV FIFO trigger level (1, 4, or 8 bytes)
B. The two blocks in dashed lines cover the case where an additional byte is sent as described in the preceding auto-$\overline{\text{RTS}}$ section.

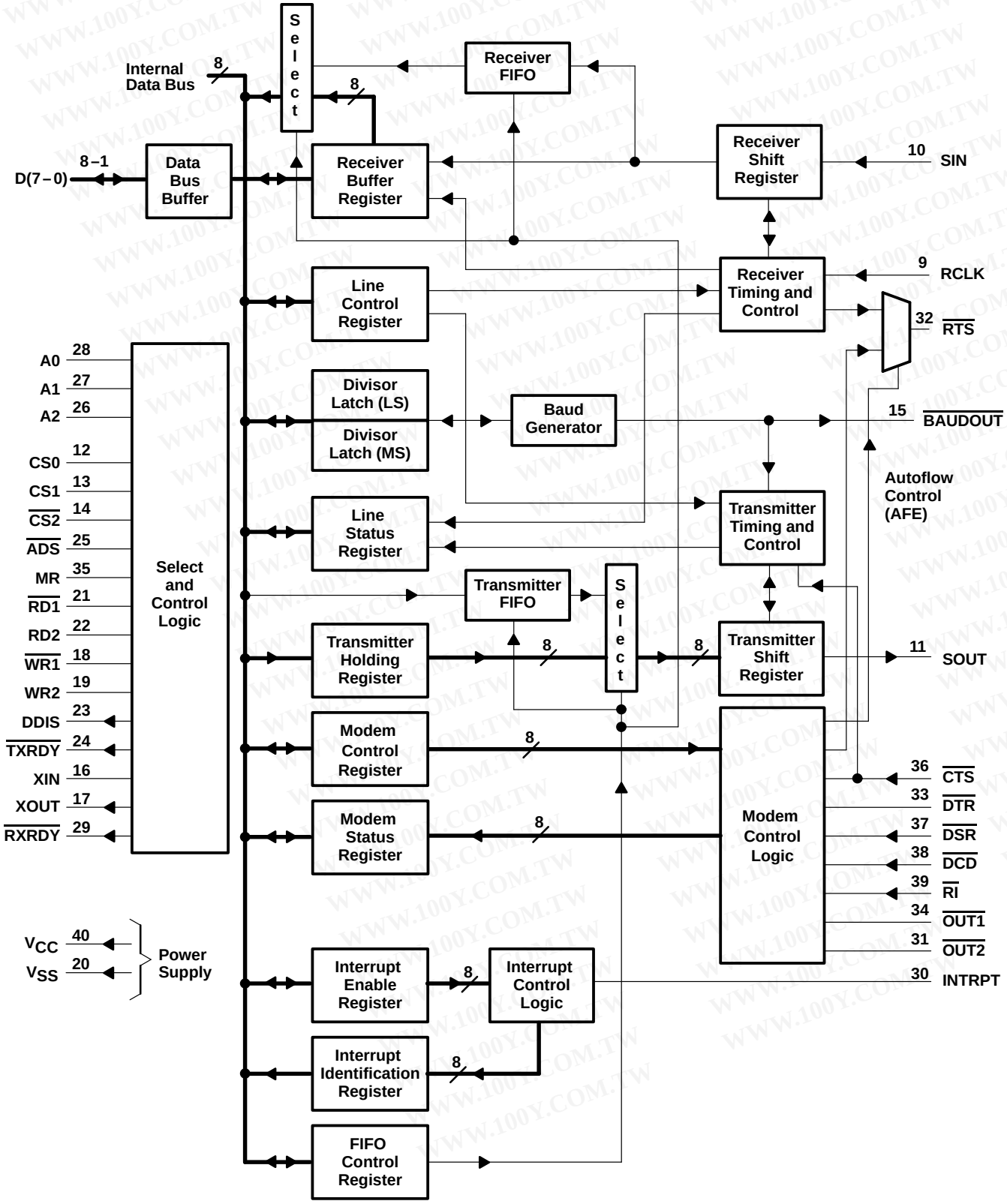
Figure 3. $\overline{\text{RTS}}$ Functional Timing Waveforms, RCV FIFO Trigger Level = 1,4, or 8 Bytes



NOTES: A. $\overline{\text{RTS}}$ is deasserted when the receiver receives the first data bit of the sixteenth byte. The receive FIFO is full after finishing the sixteenth byte.
B. $\overline{\text{RTS}}$ is asserted again when there is at least one byte of space available and no incoming byte is in processing or there is more than one byte of space available.
C. When the receive FIFO is full, the first receive buffer register read reasserts $\overline{\text{RTS}}$.

Figure 4. $\overline{\text{RTS}}$ Functional Timing Waveforms, RCV FIFO Trigger Level = 14 Bytes

functional block diagram



NOTE A: Terminal numbers shown are for the N package.

Terminal Functions

TERMINAL NAME	NO. N	NO. FN	NO. PT	I/O	DESCRIPTION
A0 A1 A2	28 27 26	31 30 29	28 27 26	I	Register select. A0–A2 are used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses and refer to $\overline{ADS}$ description.
$\overline{ADS}$	25	28	24	I	Address strobe. When $\overline{ADS}$ is active (low), A0, A1, and A2 and CS0, CS1, and $\overline{CS2}$ drive the internal select logic directly; when $\overline{ADS}$ is high, the register select and chip select signals are held at the logic levels they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15	17	12	O	Baud out. $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to RCLK.
CS0 $\overline{CS1}$ $\overline{CS2}$	12 13 14	14 15 16	9 10 11	I	Chip select. When CS0 and CS1 are high and $\overline{CS2}$ is low, these three inputs select the ACE. When any of these inputs are inactive, the ACE remains inactive (refer to $\overline{ADS}$ description).
$\overline{CTS}$	36	40	38	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (ΔCTS) of the modem status register indicates that $\overline{CTS}$ has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes levels and the auto-$\overline{CTS}$ mode is not enabled, an interrupt is generated. $\overline{CTS}$ is also used in the auto-$\overline{CTS}$ mode to control the transmitter.
D0 D1 D2 D3 D4 D5 D6 D7	1 2 3 4 5 6 7 8	2 3 4 5 6 7 8 9	43 44 45 46 47 2 3 4	I/O	Data bus. Eight data lines with 3-state outputs provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38	42	40	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 ($\overline{DCD}$) of the modem status register. Bit 3 (ΔDCD) of the modem status register indicates that $\overline{DCD}$ has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{DCD}$ changes levels, an interrupt is generated.
DDIS	23	26	22	O	Driver disable. $\overline{DDIS}$ is active (high) when the CPU is not reading data. When active, $\overline{DDIS}$ can disable an external transceiver.
$\overline{DSR}$	37	41	39	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (ΔDSR) of the modem status register indicates $\overline{DSR}$ has changed levels since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{DSR}$ changes levels, an interrupt is generated.
$\overline{DTR}$	33	37	33	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active level by setting the DTR bit of the modem control register. $\overline{DTR}$ is placed in the inactive level either as a result of a master reset, during loop mode operation, or clearing the DTR bit.
INTRPT	30	33	30	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data that is available or timed out (FIFO mode only), an empty transmitter holding register, or an enabled modem status interrupt. INTRPT is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35	39	35	I	Master reset. When active (high), MR clears most ACE registers and sets the levels of various output signals (refer to Table 2).

Terminal Functions (Continued)

TERMINAL NAME	NO. N	NO. FN	NO. PT	I/O	DESCRIPTION
$\overline{OUT1}$ $\overline{OUT2}$	34 31	38 35	34 31	O	Outputs 1 and 2. These are user-designated output terminals that are set to the active (low) level by setting respective modem control register bits (OUT1 and OUT2). $\overline{OUT1}$ and $\overline{OUT2}$ are set to inactive the (high) level as a result of master reset, during loop mode operations, or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the MCR.
RCLK	9	10	5	I	Receiver clock. RCLK is the 16× baud rate clock for the receiver section of the ACE.
$\overline{RD1}$ RD2	21 22	24 25	19 20	I	Read inputs. When either $\overline{RD1}$ or RD2 is active (low or high respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied to its inactive level (i.e., RD2 tied low or $\overline{RD1}$ tied high).
$\overline{RI}$	39	43	41	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that $\overline{RI}$ has transitioned from a low to a high level since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32	36	32	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to receive data. $\overline{RTS}$ is set to the active level by setting the RTS modem control register bit and is set to the inactive (high) level either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the MCR. In the auto-$\overline{RTS}$ mode, $\overline{RTS}$ is set to the inactive level by the receiver threshold control logic.
$\overline{RXRDY}$	29	32	29	O	Receiver ready. Receiver direct memory access (DMA) signalling is available with $\overline{RXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected using the FIFO control register bit 3 (FCR3). When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR0 = 0 or FCR0 = 1, FCR3 = 0), when there is at least one character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ is active (low). When $\overline{RXRDY}$ has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). In DMA mode 1 (FCR0 = 1, FCR3 = 1), when the trigger level or the time-out has been reached, $\overline{RXRDY}$ goes active (low); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (high).
SIN	10	11	7	I	Serial data input. SIN is serial data input from a connected communications device
SOUT	11	13	8	O	Serial data output. SOUT is composite serial data output to a connected communication device. SOUT is set to the marking (high) level as a result of master reset.
$\overline{TXRDY}$	24	27	23	O	Transmitter ready. Transmitter DMA signalling is available with $\overline{TXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected using FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	40	44	42		5-V supply voltage
V_{SS}	20	22	18		Supply common
$\overline{WR1}$ WR2	18 19	20 21	16 17	I	Write inputs. When either $\overline{WR1}$ or WR2 is active (low or high respectively) and while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied to its inactive level (i.e., WR2 tied low or $\overline{WR1}$ tied high).
XIN XOUT	16 17	18 19	14 15	I/O	External clock. XIN and XOUT connect the ACE to the main timing reference (clock or crystal).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range at any input, V_I . . . . . –0.5 V to 7 V
Output voltage range, V_O . . . . . –0.5 V to 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N or PT package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	–0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}§	High-level output voltage	I_{OH} = –1 mA		2.4			V
V_{OL}§	Low-level output voltage	I_{OL} = 1.6 mA				0.4	V
I_I	Input current	V_{CC} = 5.25 V, V_I = 0 to 5.25 V,	V_{SS} = 0, All other terminals floating			10	µA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselect	V_{SS} = 0,			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, No load on outputs,	T_A = 25°C, XTAL1 at 4 MHz, Baud rate = 50 kbit/s			10	mA
$C_{i(CLK)}$	Clock input capacitance	V_{CC} = 0, f = 1 MHz, All other terminals grounded	V_{SS} = 0, T_A = 25°C,		15	20	pF
$C_{o(CLK)}$	Clock output capacitance				20	30	pF
C_i	Input capacitance				6	10	pF
C_o	Output capacitance				10	20	pF

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ These parameters apply for all outputs except XOUT.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC			87		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC			87		ns
t_{w1}	Pulse duration, clock high	t_{XH}	5	f = 16 MHz Max	25		ns
t_{w2}	Pulse duration, clock low	t_{XL}	5	f = 16 MHz Max	25		ns
t_{w5}	Pulse duration, $\overline{ADS}$ low	t_{ADS}	6, 7		9		ns
t_{w6}	Pulse duration, $\overline{WR}$	t_{WR}	6		40		ns
t_{w7}	Pulse duration, $\overline{RD}$	t_{RD}	7		40		ns
t_{w8}	Pulse duration, MR	t_{MR}			1		µs
t_{su1}	Setup time, address valid before $\overline{ADS}\uparrow$	t_{AS}	6, 7		8		ns
t_{su2}	Setup time, CS valid before $\overline{ADS}\uparrow$	t_{CS}	6, 7		8		ns
t_{su3}	Setup time, data valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{DS}	6		15		ns
t_{su4}	Setup time, $\overline{CTS}\uparrow$ before midpoint of stop bit		17			10	ns
t_{h1}	Hold time, address low after $\overline{ADS}\uparrow$	t_{AH}	6, 7		0		ns
t_{h2}	Hold time, CS valid after $\overline{ADS}\uparrow$	t_{CH}	6, 7		0		ns
t_{h3}	Hold time, CS valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WCS}	6		10		ns
t_{h4}	Hold time, address valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WA}	6		10		ns
t_{h5}	Hold time, data valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{DH}	6		5		ns
t_{h6}	Hold time, chip select valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RCS}	7		10		ns
t_{h7}	Hold time, address valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RA}	7		20		ns
t_{d4}†	Delay time, CS valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{CSW}	6		7		ns
t_{d5}†	Delay time, address valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{AW}	6		7		ns
t_{d6}†	Delay time, write cycle, $\overline{WR1}\uparrow$ or WR2$\downarrow$ to $\overline{ADS}\downarrow$	t_{WC}	6		40		ns
t_{d7}†	Delay time, CS valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{CSR}	7		7		ns
t_{d8}†	Delay time, address valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{AR}	7		7		ns
t_{d9}	Delay time, read cycle, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to $\overline{ADS}\downarrow$	tRC	7		40		ns
t_{d10}	Delay time, $\overline{RD1}\downarrow$ or RD2$\uparrow$ to data valid	t_{RVD}	7	C_L = 75 pF	45		ns
t_{d11}	Delay time, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to floating data	t_{HZ}	7	C_L = 75 pF	20		ns

† Only applies when $\overline{ADS}$ is low

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{dis(R)}$	Disable time, $\overline{RD1}\downarrow\uparrow$ or RD2$\uparrow\downarrow$ to DDIS$\uparrow\downarrow$	t_{RDD}	7	C_L = 75 pF	20		ns

NOTE 2: Charge and discharge times are determined by V_{OL}, V_{OH}, and external loading.

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	t_{LW}	5	f = 16 MHz, CLK ÷ 2	50		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	t_{HW}	5	f = 16 MHz, CLK ÷ 2	50		ns
t_{d1}	Delay time, XIN$\uparrow$ to $\overline{BAUDOUT}\uparrow$	t_{BLD}	5			45	ns
t_{d2}	Delay time, XIN$\uparrow\downarrow$ to $\overline{BAUDOUT}\downarrow$	t_{BHD}	5			45	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample	t_{SCD}	8			10	ns
t_{d13}	Delay time, stop to set INTRPT or read RBR to LSI interrupt or stop to $\overline{RXRDY}\downarrow$	t_{SINT}	8, 9, 10, 11, 12			1	RCLK cycle
t_{d14}	Delay time, read RBR/LSR to reset INTRPT	t_{RINT}	8, 9, 10, 11, 12	C_L = 75 pF		70	ns

NOTE 3: In the FIFO mode, the read cycle (RC) = 425 ns (min) between reads of the receive FIFO and the status registers (interrupt identification register or line status register).

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, initial write to transmit start	t_{IRS}	13		8	24	baudout cycles
t_{d16}	Delay time, start to INTRPT	t_{STI}	13		8	10	baudout cycles
t_{d17}	Delay time, $\overline{WR}$ (WR THR) to reset INTRPT	t_{HR}	13	C_L = 75 pF		50	ns
t_{d18}	Delay time, initial write to INTRPT (THRE†)	t_{SI}	13		16	34	baudout cycles
t_{d19}	Delay time, read IIR† to reset INTRPT (THRE†)	t_{IR}	13	C_L = 75 pF		35	ns
t_{d20}	Delay time, write to $\overline{TXRDY}$ inactive	t_{WXI}	14,15	C_L = 75 pF		35	ns
t_{d21}	Delay time, start to $\overline{TXRDY}$ active	t_{SXA}	14,15	C_L = 75 pF		9	baudout cycles

† THRE = transmitter holding register empty; IIR = interrupt identification register.

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

PARAMETER		ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{d22}	Delay time, WR MCR to output	t_{MDO}	16		50	ns
t_{d23}	Delay time, modem interrupt to set INTRPT	t_{SIM}	16		35	ns
t_{d24}	Delay time, RD MSR to reset INTRPT	t_{RIM}	16		40	ns
t_{d25}	Delay time, $\overline{CTS}$ low to SOUT$\downarrow$		17		24	baudout cycles
t_{d26}	Delay time, RCV threshold byte to $\overline{RTS}\uparrow$		18		2	baudout cycles
t_{d27}	Delay time, read of last byte in receive FIFO to $\overline{RTS}\downarrow$		18		2	baudout cycles
t_{d28}	Delay time, first data bit of 16th character to $\overline{RTS}\uparrow$		19		2	baudout cycles
t_{d29}	Delay time, $\overline{RBRRD}$ low to $\overline{RTS}\downarrow$		19		2	baudout cycles

PARAMETER MEASUREMENT INFORMATION

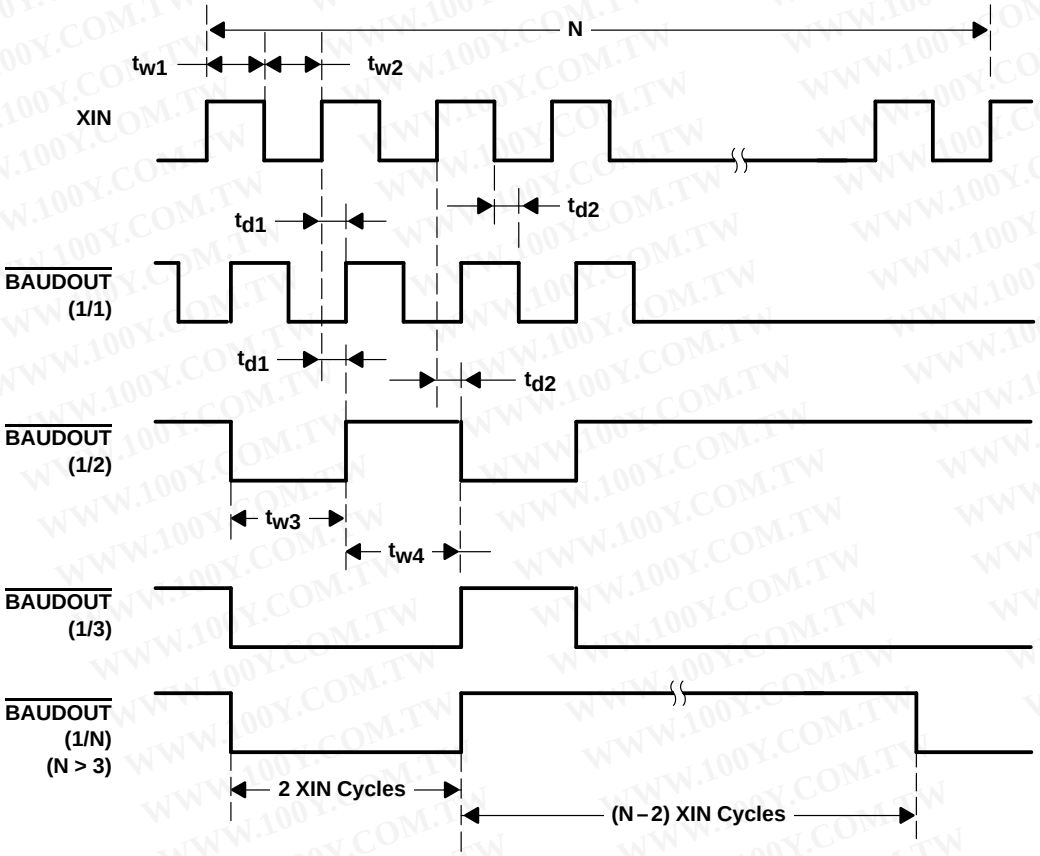
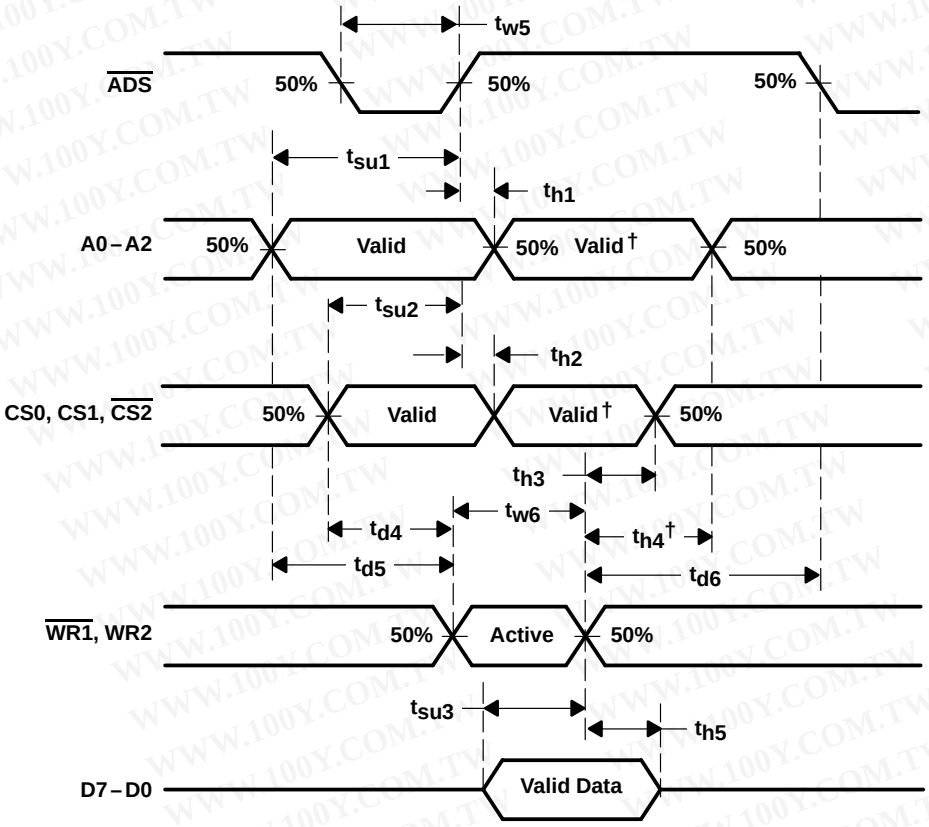


Figure 5. Baud Generator Timing Waveforms

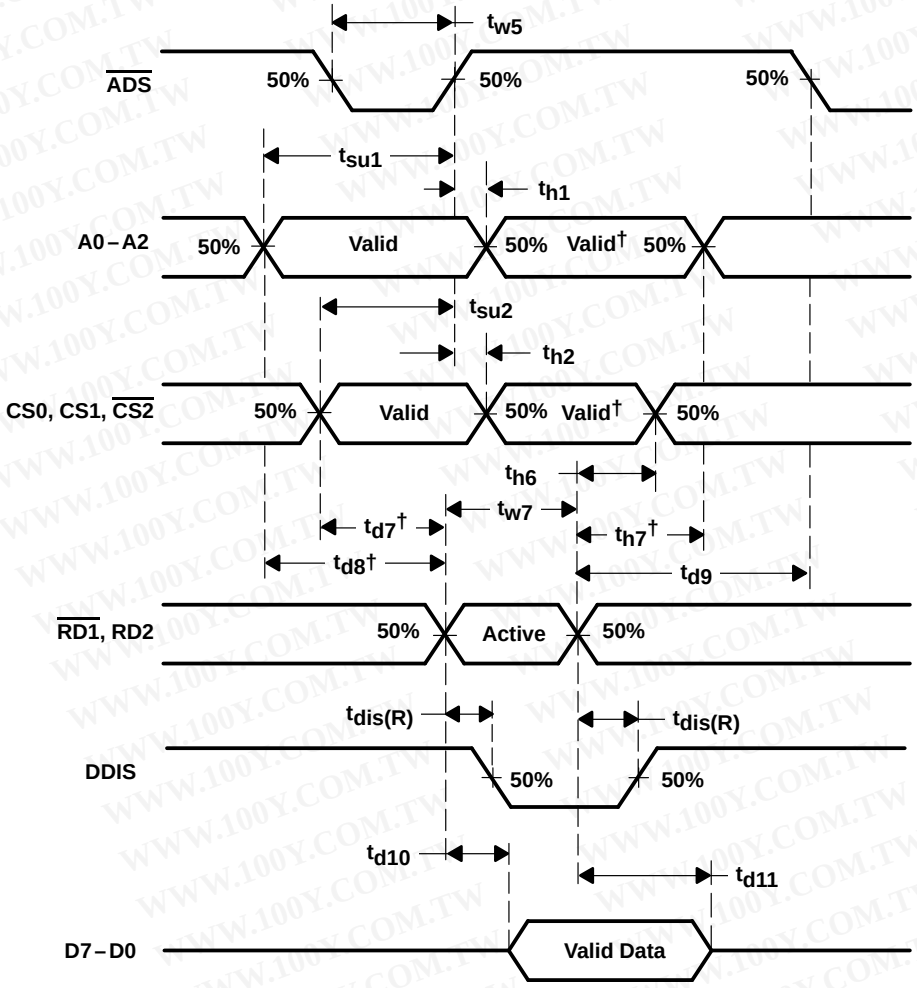
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is low

Figure 6. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is low

Figure 7. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

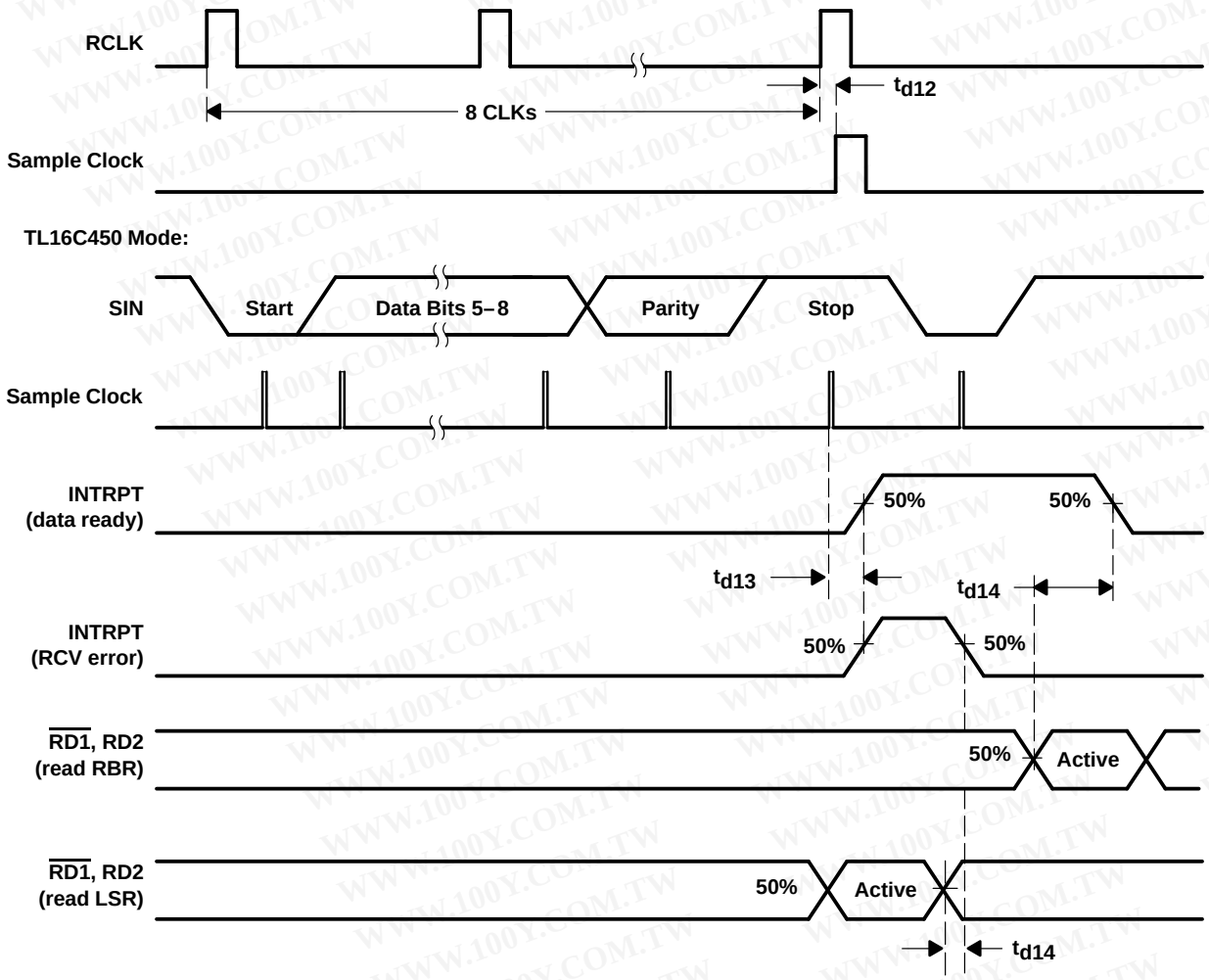
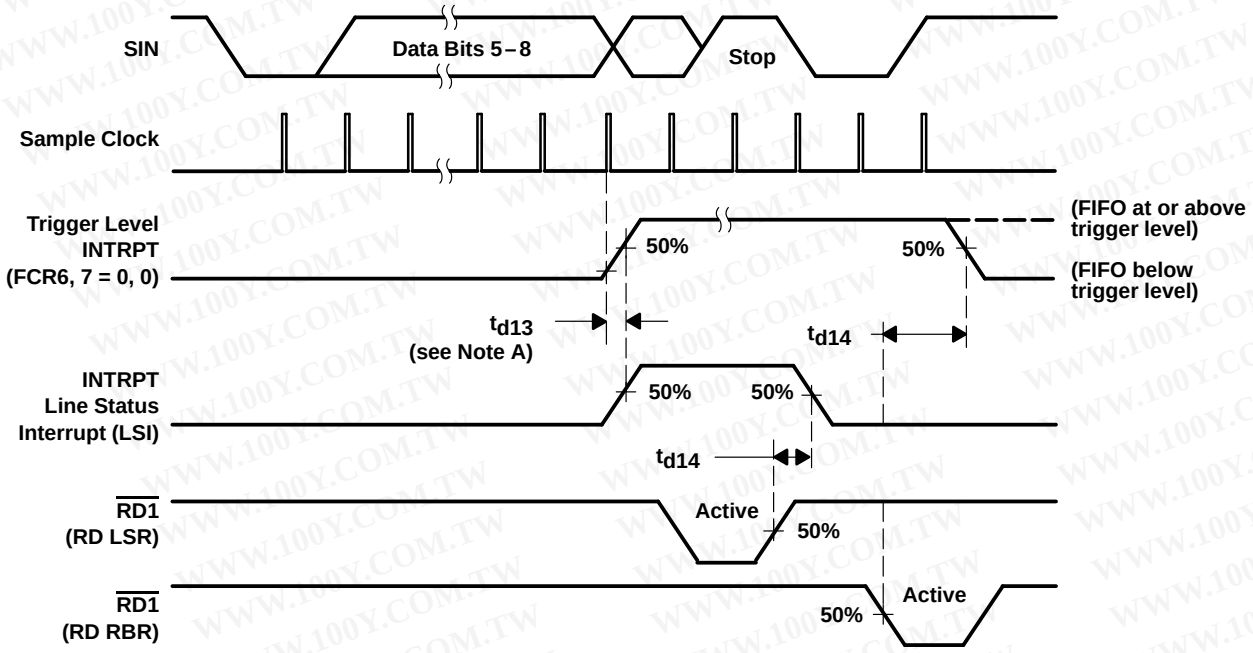


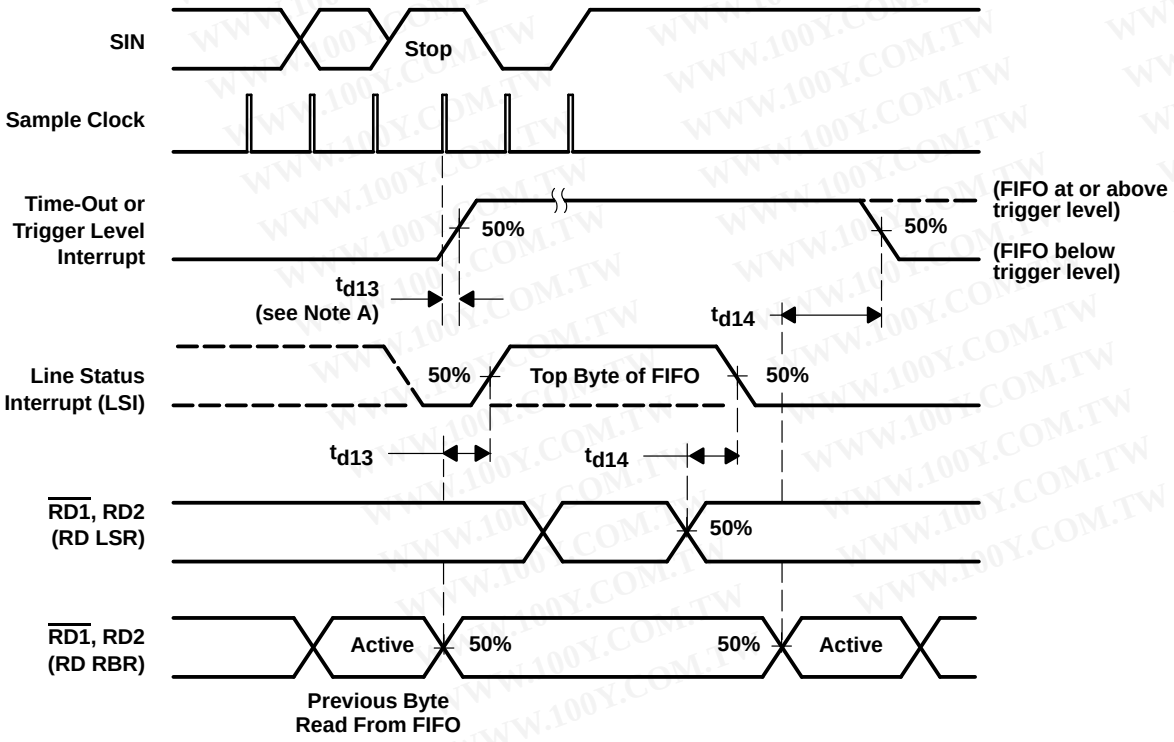
Figure 8. Receiver Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: For a time-out interrupt, t_{d13} = 9 RCLKs.

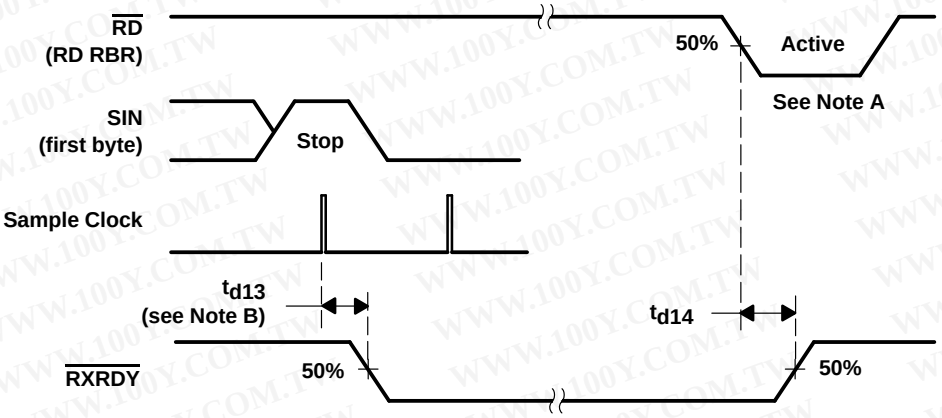
Figure 9. Receive FIFO First Byte (Sets DR Bit) Waveforms



NOTE A: For a time-out interrupt, t_{d13} = 9 RCLKs.

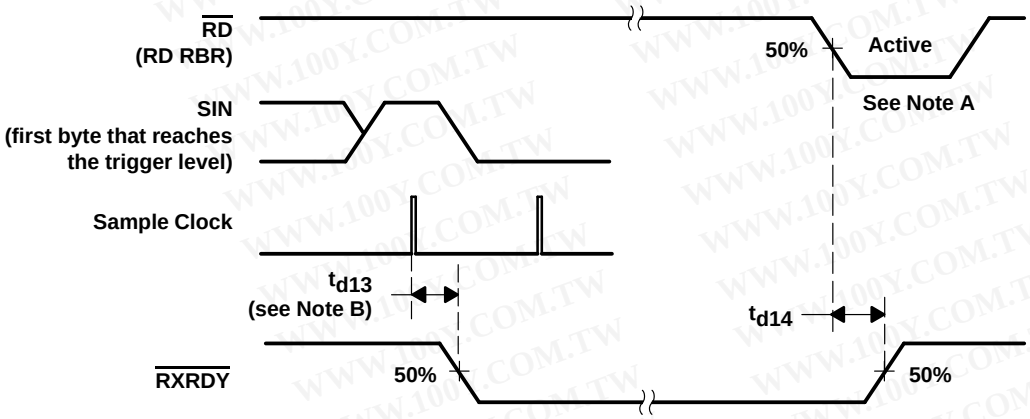
Figure 10. Receive FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This is the reading of the last byte in the FIFO.

Figure 11. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a time-out interrupt, t_{d13} = 9 RCLKs.

Figure 12. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR0 = 1 or FCR3 = 1 (Mode 1)

PARAMETER MEASUREMENT INFORMATION

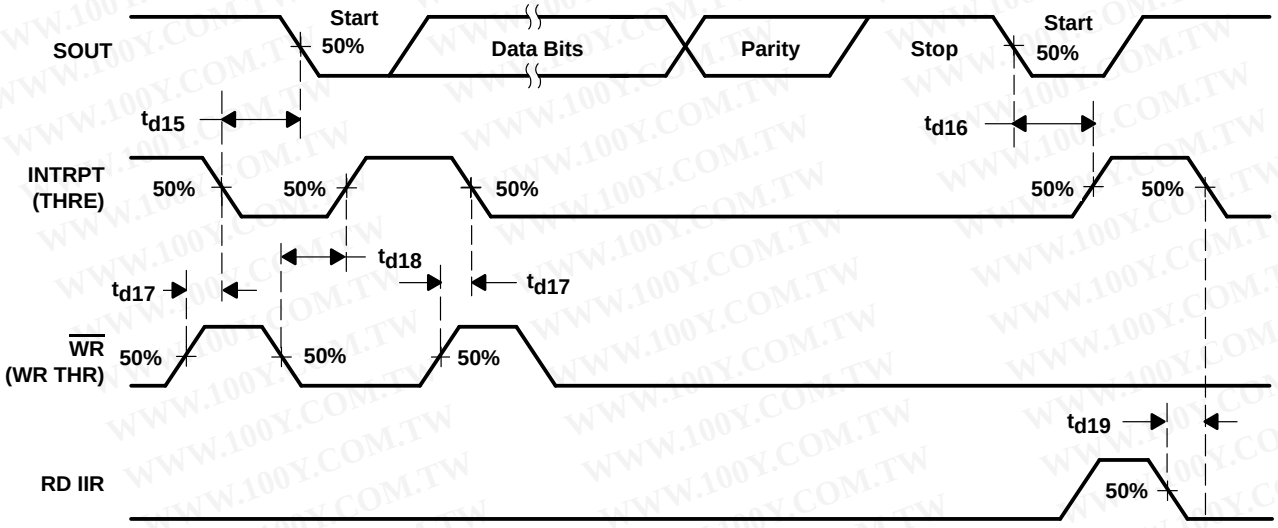


Figure 13. Transmitter Timing Waveforms

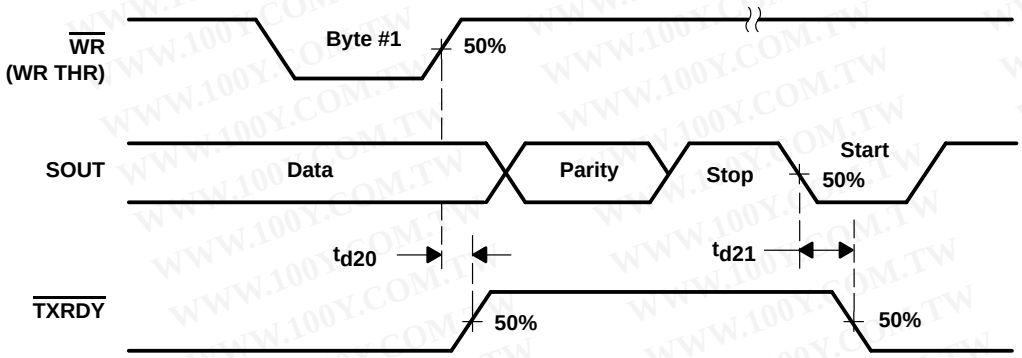


Figure 14. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

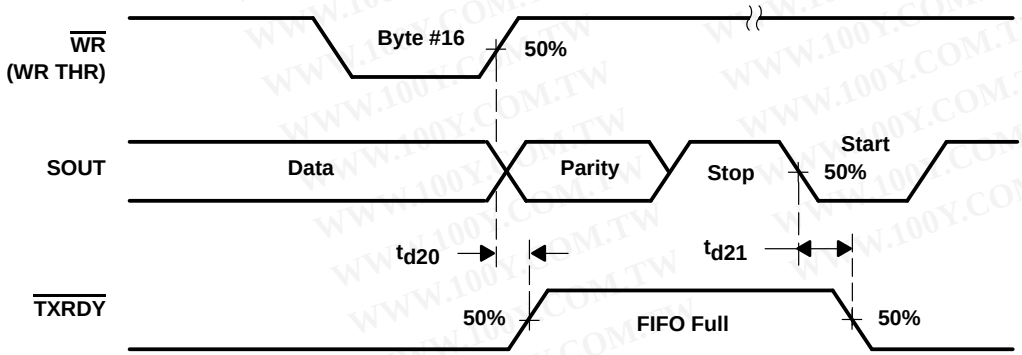


Figure 15. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

PARAMETER MEASUREMENT INFORMATION

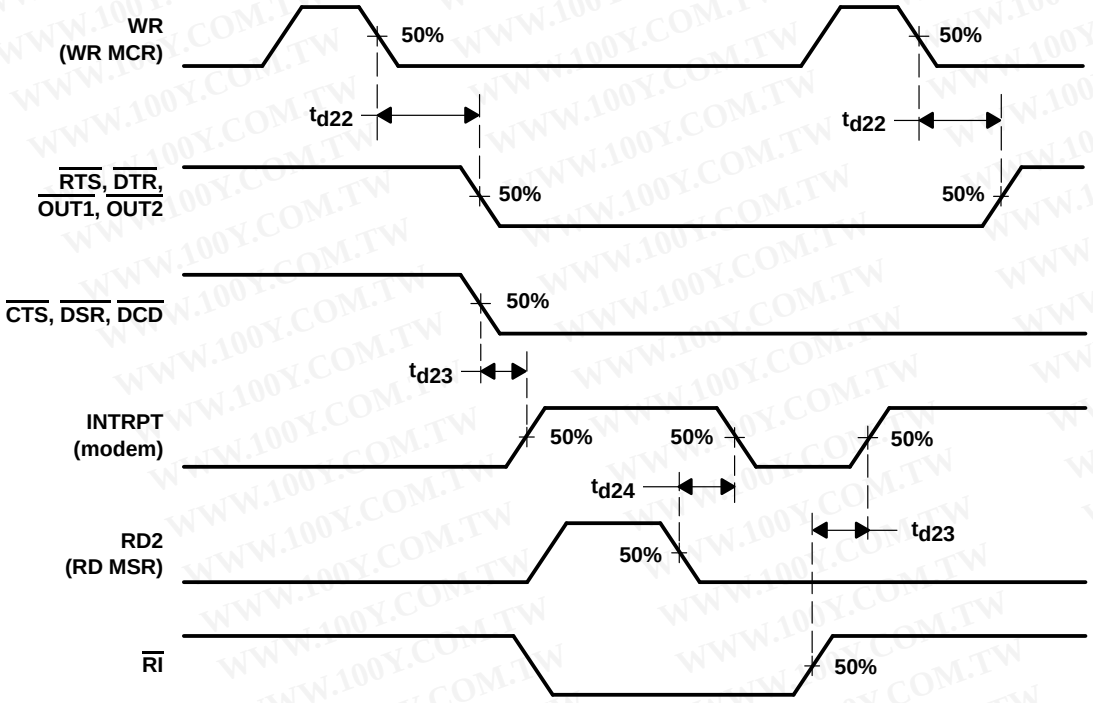


Figure 16. Modem Control Timing Waveforms

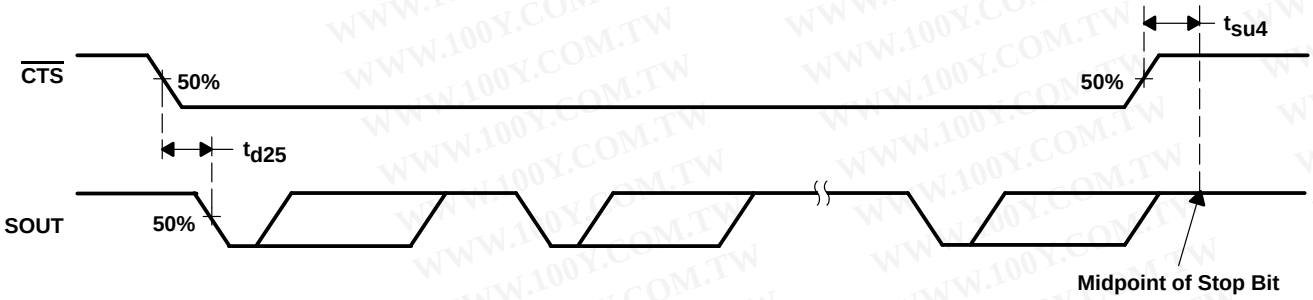


Figure 17. CTS and SOUT Autoflow Control Timing (Start and Stop) Waveforms

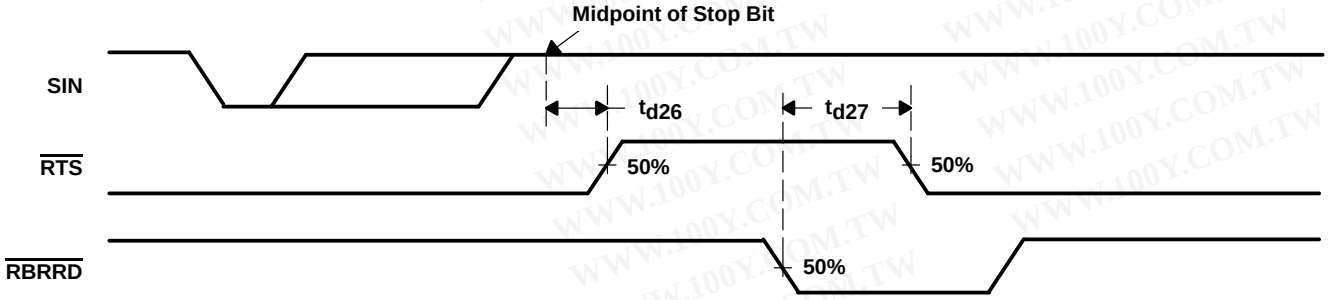


Figure 18. Auto-RTS Timing for RCV Threshold of 1, 4, or 8 Waveforms

PARAMETER MEASUREMENT INFORMATION

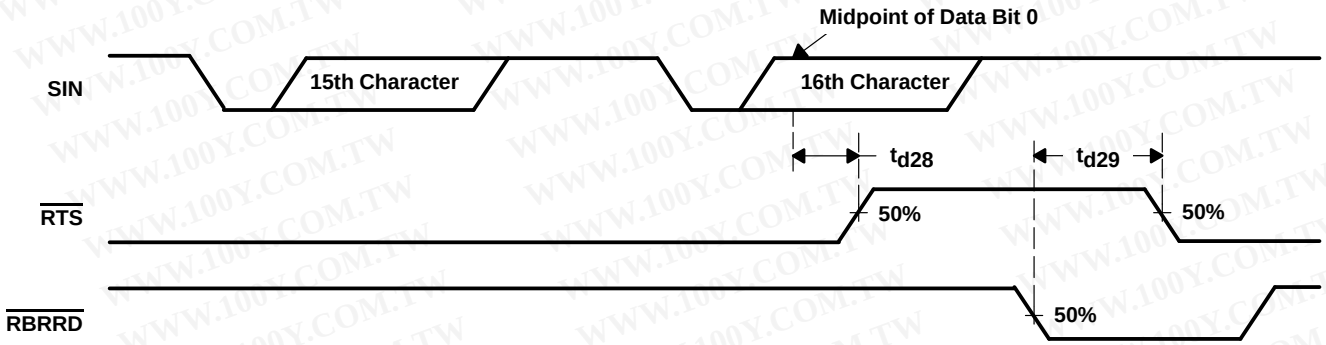


Figure 19. Auto-$\overline{\text{RTS}}$ Timing for RCV Threshold of 14 Waveforms

APPLICATION INFORMATION

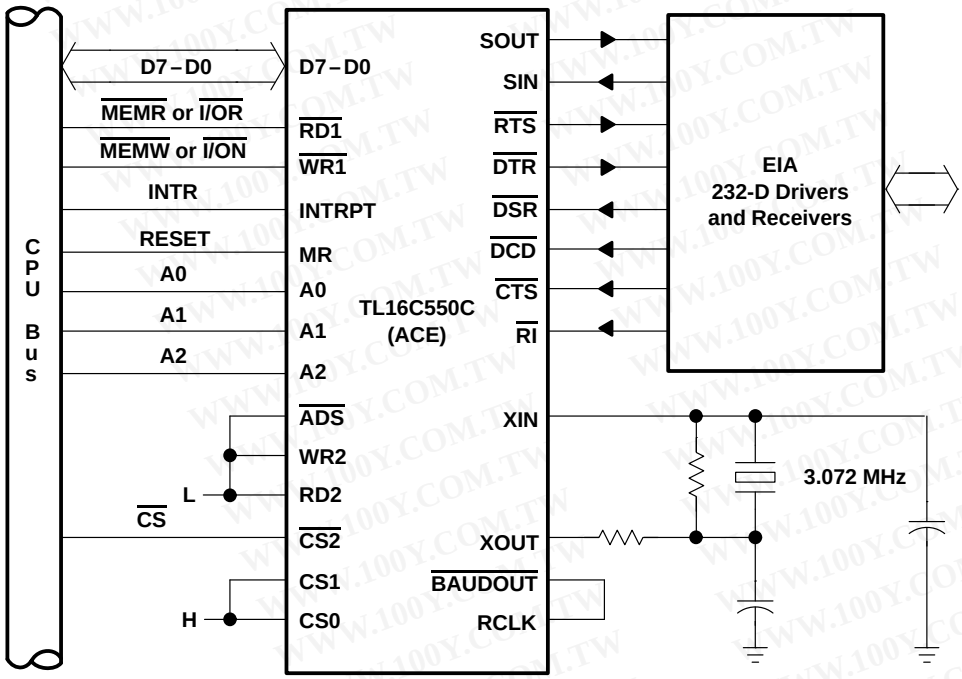


Figure 20. Basic TL16C550C Configuration

APPLICATION INFORMATION

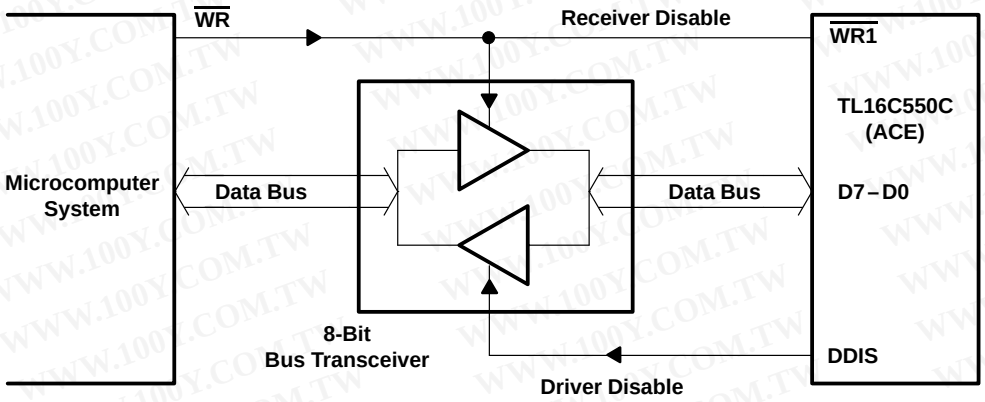
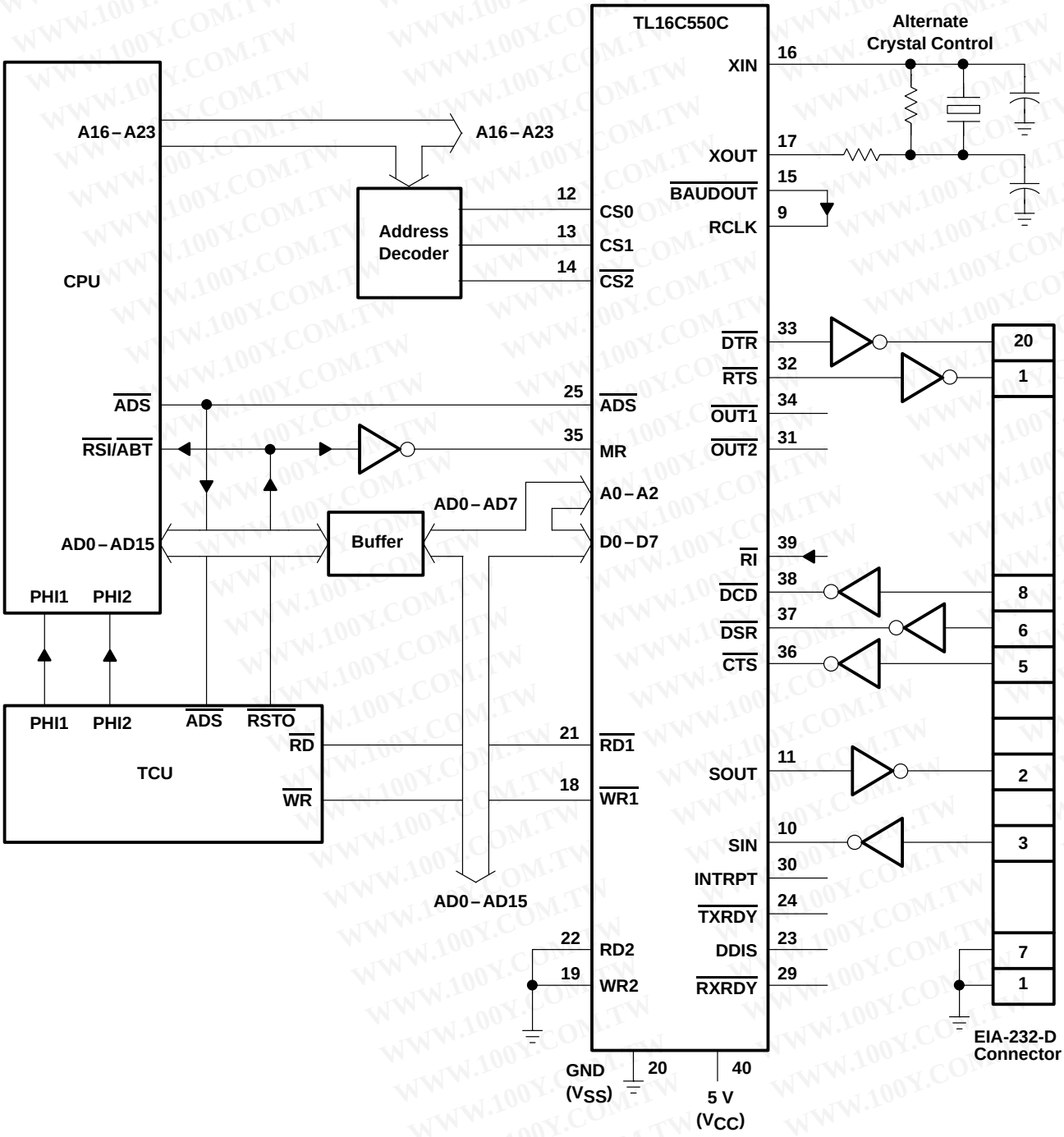


Figure 21. Typical Interface for a High Capacity Data Bus

APPLICATION INFORMATION



NOTE A: Terminal numbers shown are for the N package.

Figure 22. Typical TL16C550C Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 4).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, and bits 4–5 are permanently cleared
FIFO Control Register	Master Reset	All bits cleared
Line Control Register	Master Reset	All bits cleared
Modem Control Register	Master Reset	All bits cleared (6–7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are set; all other bits are cleared
Modem Status Register	Master Reset	Bits 0–3 are cleared; bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{\text{OUT2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT1}}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Register	Master Reset	No effect
Transmitter Holding Register	Master Reset	No effect
RCVR FIFO	MR/FCR1–FCR0/ΔFCR0	All bits cleared
XMIT FIFO	MR/FCR2–FCR0/ΔFCR0	All bits cleared

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 2. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

BIT NO.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERBI)	0 if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit 2	Transmitter FIFO Reset	Number of Stop Bits (STB)	OUT1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit 3 (see Note 4)	DMA Mode Select	Parity Enable (PEN)	OUT2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	Autoflow Control Enable (AFE)	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (see Note 4)	Receiver Trigger (LSB)	Break Control	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (see Note 4)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (see Note 4)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
NOTE 4: These bits are always 0 in the TL16C450 mode.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables and clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

- Bit 0: This bit, when set, enables the transmitter and receiver FIFOs. Bit 0 must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: This bit, when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The one that is written to this bit position is self clearing.
- Bit 2: This bit, when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The one that is written to this bit position is self clearing.
- Bit 3: When FCR0 is set, setting FCR3 causes $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ to change from level 0 to level 1.
- Bits 4 and 5: These two bits are reserved for future use.
- Bits 6 and 7: These two bits set the trigger level for the receiver FIFO interrupt (see Table 5).

Table 4. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1, IER2 = 1), a receiver interrupt occurs as follows:

1. The received data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06) has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set when a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

When the receiver FIFO and receiver interrupts are enabled:

1. FIFO time-out interrupt occurs if the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO occurred more than four continuous character times ago. This causes a maximum character received to interrupt an issued delay of 160 ms at 300 baud with a 12-bit character.
2. Character times are calculated by using the RCLK input for a clock signal (makes the delay proportional to the baud rate).
3. When a time-out interrupt has occurred, it is cleared and the timer is cleared when the microprocessor reads one character from the receiver FIFO.
4. When a time-out interrupt has not occurred, the time-out timer is cleared after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmitter FIFO and THRE interrupt are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register interrupt [IIR (3–0) = 2] occurs when the transmit FIFO is empty. It is cleared [IIR (3–0) = 1] when the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmitter FIFO empty indicator (LSR5 (THRE) = 1) is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time that THRE = 1. The first transmitter interrupt after changing FCR0 is immediate if it is enabled.

Character time-out and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt; transmit FIFO empty has the same priority as the current THRE interrupt.

FIFO polled mode operation

With FCR0 = 1 (transmitter and receiver FIFOs enabled), clearing IER0, IER1, IER2, IER3, or all four to 0 puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks receiver and transmitter status using the LSR. As stated previously:

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 – LSR4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode; the IIR is not affected since IER2 = 0.
- LSR5 indicates when the THR is empty.
- LSR6 indicates that both the THR and TSR are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

PRINCIPLES OF OPERATION

interrupt enable register (IER)

The IER enables each of the five types of interrupts (refer to Table 4) and enables INTRPT in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3 and are described in the following bullets.

- Bit 0: When set, this bit enables the received data available interrupt.
- Bit 1: When set, this bit enables the THRE interrupt.
- Bit 2: When set, this bit enables the receiver line status interrupt.
- Bit 3: When set, this bit enables the modem status interrupt.
- Bits 4 through 7: These bits are not used (always cleared).

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time-out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and encodes the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 2 and described in Table 4. Detail on each bit is as follows:

- Bit 0: This bit is used either in a hardwire prioritized or polled interrupt system. When bit 0 is cleared, an interrupt is pending If bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 3
- Bit 3: This bit is always cleared in TL16C450 mode. In FIFO mode, bit 3 is set with bit 2 to indicate that a time-out interrupt is pending.
- Bits 4 and 5: These two bits are not used (always cleared).
- Bits 6 and 7: These bits are always cleared in TL16C450 mode. They are set when bit 0 of the FIFO control register is set.

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Read the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode	Read the receiver buffer register
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time	Read the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Read the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Read the modem status register

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 6.

Table 6. Serial Character Word Length

BIT 1	BIT 0	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit 2 are shown in Table 7.

line control register (LCR) (continued)

Table 7. Number of Stop Bits Generated

BIT 2	WORD LENGTH SELECTED BY BITS 1 AND 2	NUMBER OF STOP BITS GENERATED
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set even parity (an even number of logic 1s in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This bit is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. If bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition; i.e., a condition where SOUT is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic; it only effects SOUT.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. DR is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: This bit is the overrun error (OE) indicator. When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

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line status register (LSR) (continued)†

- Bit 2‡: This bit is the parity error (PE) indicator. When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3‡: This bit is the framing error (FE) indicator. When FE is set, it indicates that the received character did not have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE samples this start bit twice and then accepts the input data.
- Bit 4‡: This bit is the break interrupt (BI) indicator. When BI is set, it indicates that the received data input was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state for at least two RCLK samples and then receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. THRE is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. TEMT bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550C mode, this bit is always cleared. In the TL16C450 mode, this bit is always cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the $\overline{\text{DTR}}$ output.
- Bit 1: This bit (RTS) controls the $\overline{\text{RTS}}$ output.
- Bit 2: This bit (OUT1) controls $\overline{\text{OUT1}}$, a user-designated output signal.
- Bit 3: This bit (OUT2) controls $\overline{\text{OUT2}}$, a user-designated output signal.

When any of bits 0 through 3 are set, the associated output is forced low. When any of these bits are cleared, the associated output is forced high.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

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modem control register (MCR) (continued)

- Bit 4: This bit (LOOP) provides a local loop back feature for diagnostic testing of the ACE. When LOOP is set, the following occurs:
  - The transmitter SOUT is set high.
  - The receiver SIN is disconnected.
  - The output of the TSR is looped back into the receiver shift register input.
  - The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
  - The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs.
  - The four modem control outputs are forced to the inactive (high) levels.
- Bit 5: This bit (AFE) is the autoflow control enable. When set, the autoflow control as described in the detailed description is enabled.

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt's sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

  The ACE flow can be configured by programming bits 1 and 5 of the MCR as shown in Table 8.

Table 8. ACE Flow Configuration

MCR BIT 5 (AFE)	MCR BIT 1 (RTS)	ACE FLOW CONFIGURATION
1	1	Auto-$\overline{RTS}$ and auto-$\overline{CTS}$ enabled (autoflow control enabled)
1	0	Auto-$\overline{CTS}$ only enabled
0	X	Auto-$\overline{RTS}$ and auto-$\overline{CTS}$ disabled

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the change in clear-to-send (ΔCTS) indicator. ΔCTS indicates that the $\overline{CTS}$ input has changed state since the last time it was read by the CPU. When ΔCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled (ΔCTS is cleared), no interrupt is generated.
- Bit 1: This bit is the change in data set ready (ΔDSR) indicator. ΔDSR indicates that the $\overline{DSR}$ input has changed state since the last time it was read by the CPU. When ΔDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of the ring indicator (TERI) detector. TERI indicates that the $\overline{RI}$ input to the chip has changed from a low to a high level. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

- Bit 3: This bit is the change in data carrier detect (ΔDCD) indicator. ΔDCD indicates that the $\overline{DCD}$ input to the chip has changed state since the last time it was read by the CPU. When ΔDCD is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the complement of the clear-to-send ($\overline{CTS}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 1 (RTS).
- Bit 5: This bit is the complement of the data set ready ($\overline{DSR}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 0 (DTR).
- Bit 6: This bit is the complement of the ring indicator ($\overline{RI}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 2 (OUT1).
- Bit 7: This bit is the complement of the data carrier detect ($\overline{DCD}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 16 MHz and divides it by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is:

divisor = XIN frequency input ÷ (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 9 and 10 illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38.4 kbits/s and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency (refer to Figure 23 for examples of typical clock circuits).

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 9. Baud Rates Using a 1.8432-MHz Crystal

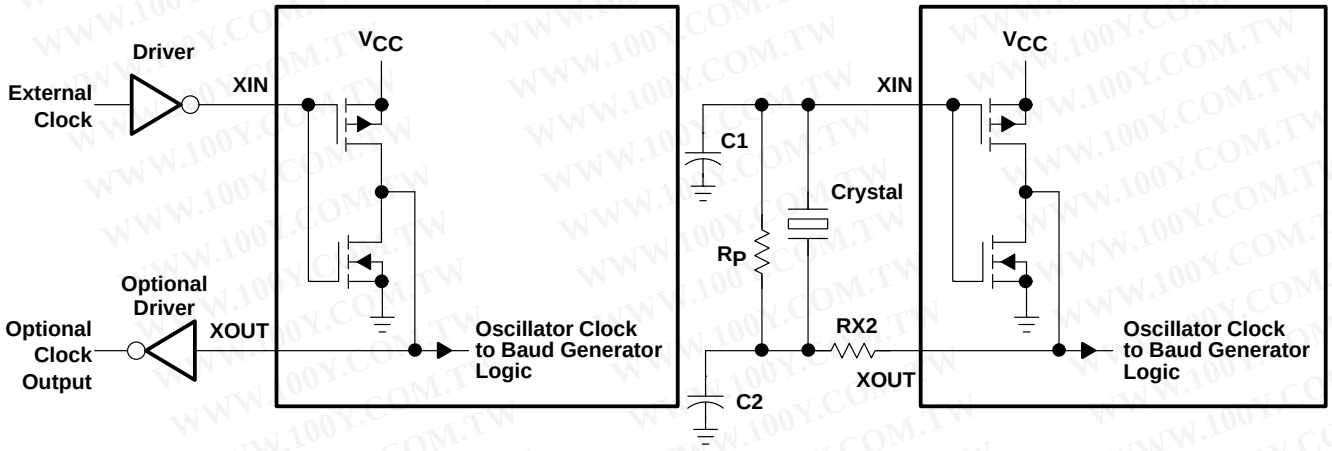
DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 × CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 10. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 × CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

PRINCIPLES OF OPERATION

programmable baud generator (continued)



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	R_P	RX2	C1	C2
3.072 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8432 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 23. Typical Clock Circuits

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE RSR receives serial data from SIN. The RSR then concatenates the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled (IER0 = 1), an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

scratch register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is supplied by $\overline{\text{BAUDOUT}}$. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at SOUT. In the TL16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER1 = 1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

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