1. INTRODUCTION

1.1 DESCRIPTION

The TMS 9901 Programmable Systems Interface is a multifunctioned component designed to provide low cost interrupts and I/O ports in a 9900/9980 microprocessor system. It is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs and outputs including the power supply (+ 5 V) and single-phase clock. The Programmable Systems Interface provides a 9900/9980 system with interrupt control, I/O ports, and a real-time clock as shown in Figure 1.

1.2 KEY FEATURES

- N-channel Silicon-Gate Process
- 9900 Series CRU Peripheral
- Performs Interrupt and I/O Interface Functions
  - 6 Dedicated Interrupt Input Lines
  - 7 Dedicated I/O Ports
  - 9 Ports Programmable as Interrupts or I/O
- Easily Stacked for Interrupt and I/O Expansion
- Interval and Event Timer
- Single 5 V Supply

2. FUNCTIONAL DESCRIPTION

2.1 CPU INTERFACE

The TMS 9901 interfaces to the CPU through the Communications Register Unit (CRU) and the interrupt control lines as shown in Figure 2. The CRU interface consists of 5 address select lines (S0-S4), chip enable ($\overline{CE}$), and 3 CRU lines (CRUIN, CRUOUT, CRUCLK). When $\overline{CE}$ becomes active (low), the 5 select lines point to the CRU bit being accessed (see Table 1). In the case of a write, the datum is strobed off the CRUOUT line by the CRUCLK signal. For a read, the datum is sent to the CPU on the CRUIN line. The interrupt control lines consist of an interrupt request line ($\overline{INTREQ}$) and 4 code lines (IC0-IC3). The interrupt section of the TMS 9901 prioritizes and encodes the highest priority active interrupt into the proper code to present to the CPU, and outputs this code on the IC0-IC3 code lines along with an active $\overline{INTREQ}$. Several TMS 9901's can be used with the CPU by connecting all CRU and address lines in parallel and providing a unique chip select to each device.

2.2 SYSTEM INTERFACE

The system interface consists of 22 pins divided into 3 groups. The 6 pins in Group 1 ($\overline{INT1}$ – $\overline{INT6}$) are normally dedicated to interrupt inputs (active low), but may also be used as input ports (true data in). Group 2 ($\overline{INT7}$/P15 – $\overline{INT15}$/P7) consists of 9 pins which can be individually programmed as interrupt inputs (active low), input ports (true data in), or output ports (true data out). The remaining 7 pins which comprise Group 3 (P0–P6) are dedicated as individually programmable I/O ports (true data).

2.3 INTERRUPT CONTROL

A block diagram of the interrupt control section is shown in Figure 3. The interrupt inputs (6 dedicated, 9 programmable) are sampled by $\overline{\phi}$ (active low) and are ANDED with their respective mask bits. If an interrupt input is active (low) and enabled (MASK=1), the signal is passed through to the priority encoder where the highest priority signal is encoded into a 4 bit binary code as shown in Table 2. The code along with interrupt request is then output via the CPU interface on the leading edge of the next $\overline{\phi}$ to ensure proper synchronization to the processor.

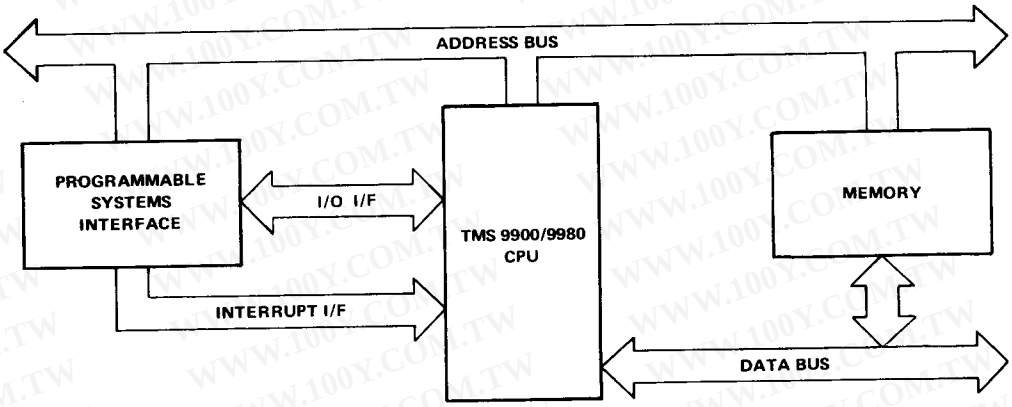


FIGURE 1 – 9900/9980 SYSTEM

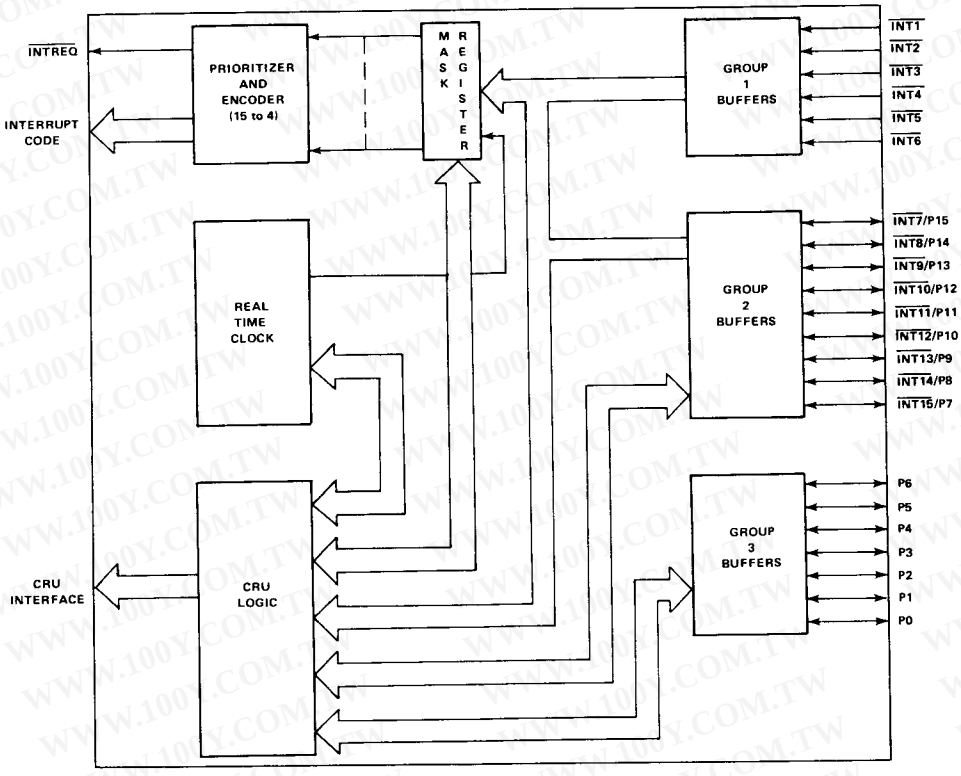


FIGURE 2 – TMS 9901 BLOCK DIAGRAM

TABLE 1
CRU BIT ASSIGNMENTS

CRU Bit	S_0 S_1 S_2 S_3 S_4	CRU Read Data	CRU Write Data
0	0 0 0 0 0	CONTROL BIT(1)	CONTROL BIT(1)
1	0 0 0 0 1	$\overline{INT}$1/CLK1(2)	Mask 1/CLK1(3)
2	0 0 0 1 0	$\overline{INT}$2/CLK2	Mask 2/CLK2
3	0 0 0 1 1	$\overline{INT}$3/CLK3	Mask 3/CLK3
4	0 0 1 0 0	$\overline{INT}$4/CLK4	Mask 4/CLK4
5	0 0 1 0 1	$\overline{INT}$5/CLK5	Mask 5/CLK5
6	0 0 1 1 0	$\overline{INT}$6/CLK6	Mask 6/CLK6
7	0 0 1 1 1	$\overline{INT}$7/CLK7	Mask 7/CLK7
8	0 1 0 0 0	$\overline{INT}$8/CLK8	Mask 8/CLK8
9	0 1 0 0 1	$\overline{INT}$9/CLK9	Mask 9/CLK9
10	0 1 0 1 0	$\overline{INT}$10/CLK10	Mask 10/CLK10
11	0 1 0 1 1	$\overline{INT}$11/CLK11	Mask 11/CLK11
12	0 1 1 0 0	$\overline{INT}$12/CLK12	Mask 12/CLK12
13	0 1 1 0 1	$\overline{INT}$13/CLK13	Mask 13/CLK13
14	0 1 1 1 0	$\overline{INT}$14/CLK14	Mask 14/CLK14
15	0 1 1 1 1	$\overline{INT15/INTREQ}$	Mask 15/$\overline{RST2}$(4)
16	1 0 0 0 0	PO Input(5)	PO Output(6)
17	1 0 0 0 1	P1 Input	P1 Output
18	1 0 0 1 0	P2 Input	P2 Output
19	1 0 0 1 1	P3 Input	P3 Output
20	1 0 1 0 0	P4 Input	P4 Output
21	1 0 1 0 1	P5 Input	P5 Output
22	1 0 1 1 0	P6 Input	P6 Output
23	1 0 1 1 1	P7 Input	P7 Output
24	1 1 0 0 0	P8 Input	P8 Output
25	1 1 0 0 1	P9 Input	P9 Output
26	1 1 0 1 0	P10 Input	P10 Output
27	1 1 0 1 1	P11 Input	P11 Output
28	1 1 1 0 0	P12 Input	P12 Output
29	1 1 1 0 1	P13 Input	P13 Output
30	1 1 1 1 0	P14 Input	P14 Output
31	1 1 1 1 1	P15 Input	P15 Output

NOTES: (1) 0 = Interrupt Mode 1 = Clock Mode

(2) Data present on $\overline{INT}$ input pin (or clock value) will be read regardless of mask value.

(3) While in the Interrupt Mode (Control Bit = 0) writing a "1" into mask will enable interrupt; a "0" will disable.

(4) Writing a zero to bit 15 while in the clock mode (control bit = 1) executes a software reset of the I/O pins.

(5) Data present on the pin will be read. Output data can be read without affecting the data.

(6) Writing data to the port will program the port to the output mode and output the data.

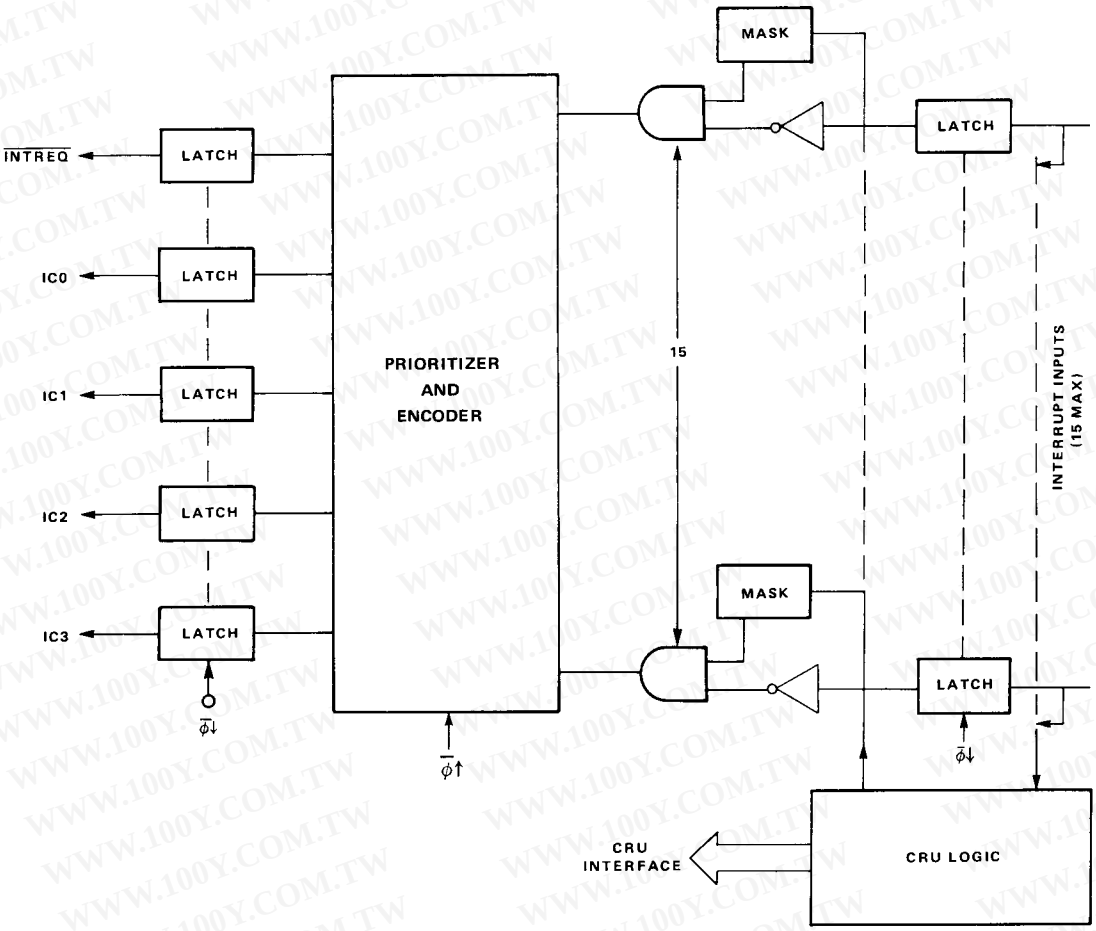


FIGURE 3 – INTERRUPT CONTROL LOGIC

TABLE 2
INTERRUPT CODE GENERATION

INTERRUPT/STATE	PRIORITY	I_{C0}	I_{C1}	I_{C2}	I_{C3}	$\overline{INTREQ}$
$\overline{INT}$ 1	1 (HIGHEST)	0	0	0	1	0
$\overline{INT}$ 2	2	0	0	1	0	0
$\overline{INT}$ 3/CLOCK	3	0	0	1	1	0
$\overline{INT}$ 4	4	0	1	0	0	0
$\overline{INT}$ 5	5	0	1	0	1	0
$\overline{INT}$ 6	6	0	1	1	0	0
$\overline{INT}$ 7	7	0	1	1	1	0
$\overline{INT}$ 8	8	1	0	0	0	0
$\overline{INT}$ 9	9	1	0	0	1	0
$\overline{INT}$ 10	10	1	0	1	0	0
$\overline{INT}$ 11	11	1	0	1	1	0
$\overline{INT}$ 12	12	1	1	0	0	0
$\overline{INT}$ 13	13	1	1	0	1	0
$\overline{INT}$ 14	14	1	1	1	0	0
$\overline{INT}$ 15	15 (LOWEST)	1	1	1	1	0
NO INTERRUPT	–	1	1	1	1	1

The output signals will remain valid until the corresponding interrupt input is removed, the interrupt is disabled (MASK=0), or a higher priority enabled interrupt becomes active. When the highest priority enabled interrupt is removed, the code corresponding to the next highest priority enabled interrupt is output. If no enabled interrupt is active, all CPU interface lines ($\overline{INTREQ}$, IC0-IC3) are held high. $\overline{RST}$1 (power-up-reset) will force the output code to (0,0,0,0) with $\overline{INTREQ}$ held high and will reset all mask bits low (interrupts disabled). Individual interrupts can be subsequently enabled (disabled) by programming the appropriate command bits. Unused interrupt inputs may be used as datum inputs by disabling the interrupt (MASK=0).

2.4 INPUT/OUTPUT

A block diagram of the I/O section is shown in Figure 4. Up to 16 individually controlled I/O ports are available (7 dedicated, 9 programmable). $\overline{RST}$1 or $\overline{RST}$2 (a command bit) will program all ports to the input mode. Writing a datum to any port will program that port to the output mode and latch out the datum. The port will then remain in the output mode until either $\overline{RST}$1 or $\overline{RST}$2 are executed. Data present on the Group 2 pins can be read by either the Read Interrupt Commands or the Read Input Commands. Group 2 pins being used as input ports should have their respective Interrupt Mask values reset (low) to prevent false interrupts from occurring. In applications where Group 1 pins are not required as interrupt inputs, they may be used as input ports and read using the Read Input commands. As with Group 2 ports, any pins being used as input ports should have their respective Interrupt Masks disabled.

2.5 PROGRAMMABLE REAL TIME CLOCK

A block diagram of the programmable real time clock section is shown in Figure 5. The clock consists of a 14 bit counter that decrements at a rate of F(ϕ)/64 (at 3 MHz this results in a maximum interval of 349 ms with a resolution of 21.3 μs) and can be used as either an interval timer or as an event timer.

The clock is accessed by writing a one into the control bit (address 0) to force CRU bits 1-15 to clock mode. (See Table 1.) Writing a nonzero value into the clock register then enables the clock and sets its frequency. During system set up this entire operation can be accomplished with one additional I/O instruction (LDCR) as shown in Table 3. The clock functions as an interval timer by decrementing to zero, issuing an interrupt, and restarting at the programmed start

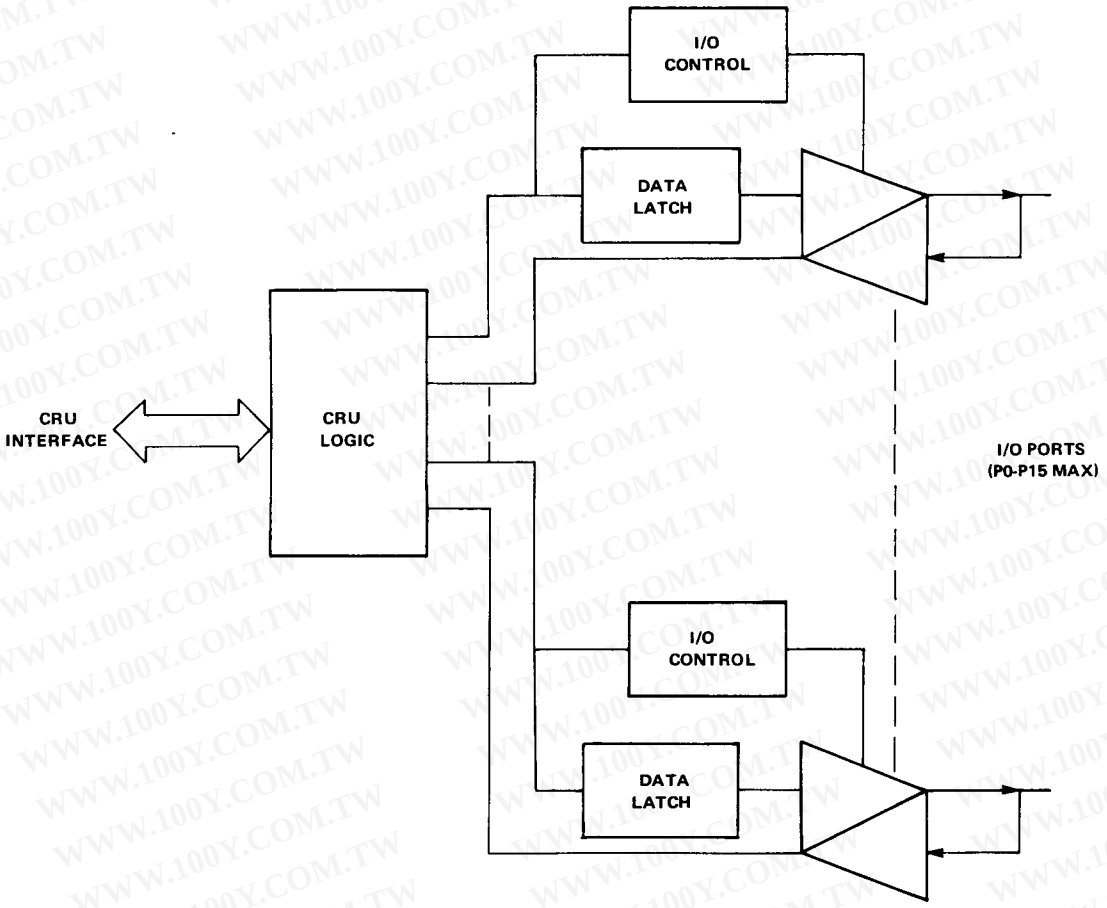


FIGURE 4 – I/O INTERFACE

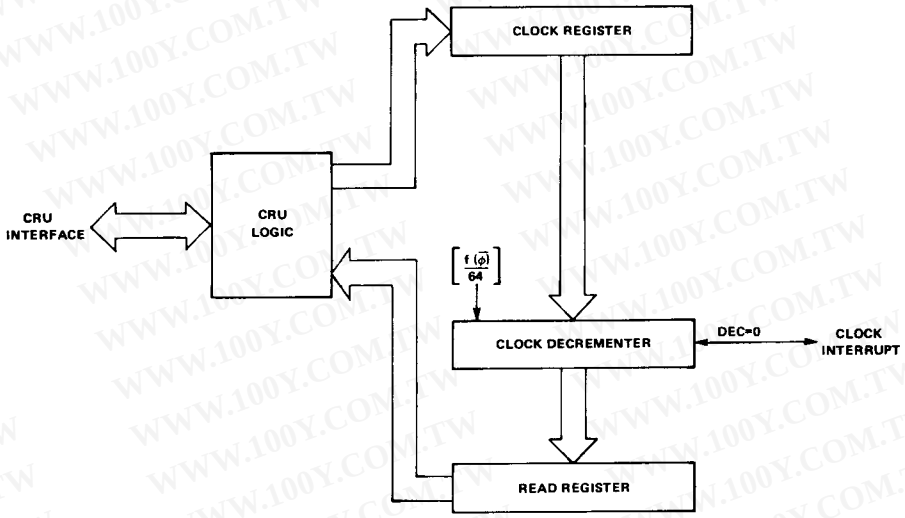


FIGURE 5 – REAL TIME CLOCK

TABLE 3
SOFTWARE EXAMPLES

ASSUMPTIONS

- System uses clock at maximum interval
- Total of 6 interrupts are used
- 8 bits are used as output port
- 8 bits are used as input port
- $\overline{RST}$1 (power up reset) has already been applied.

```
System Setup for Interrupt
        LI      R12,PSIBAS      Setup CRU Base Address to point to 9901
        LDCR    @X,0            Program Clock with maximum interval
        LDCR    @Y,7            Re-enter interrupt mode and enable top 6 interrupts

System Setup for Output Ports
        LI      R12,PSIBAS+ 16  Move CRU Base to point to I/O port
        LDCR    R1,8            Move most significant byte of R1 to output port

Read Programmed Inputs
        LI      R12,PSIBAS+ 24  Move CRU Base to point to input ports
        STCR    R2,8            Move input port to most significant byte of R2

        (X) ----> FFFF

        (Y) ----> 7FXX

                  Don't Cares

        BLWP    CLKVCT          Save Interrupt Mask
         .
         .
         .
CLKPC   LIMI    0               Disable INTERRUPTS
        LI      R12,PSIBAS +1   Set up CRU Base
        SBO     -1              Set 9901 into Clock Mode, Latch Clock Value
        STCR    R4, 14          Store Read Register Latch Value into R4
        SBZ     -1              Reenter Interrupt Mode and Restarting Clock
        RTWP                    Restore Interrupt Mask
         .
         .
         .
CLKVCT  DATA    CLKWP, CLKPC
```

value. When the clock interrupt is active, the clock mask (mask bit 3) must be written into (with either a "1" or a "0") to clear the interrupt.

If a value other than that initially programmed is required, a new 14-bit clock start value is similarly programmed by executing a CRU write operation to the same locations. During programming the decrementer is restarted with the current start value after each start value bit is written. A timer restart can be easily implemented by writing a single bit to any of the clock bits.

The clock is disabled by $\overline{RST}$I (power-up-clear) or by writing a zero value into the clock register. Enabling the clock programs the third priority interrupt ($\overline{INT}$3) as the clock interrupt and disables generation of interrupts from the $\overline{INT}$3 input pin. When accessing the clock all interrupts should be disabled to ensure that system integrity is maintained.

The clock can also function as an event timer since whenever the device is switched to the clock mode, by writing a one to the control bit, the current value of the clock is stored in the clock read register. Reading this value, and thus the elapsed event time, is accomplished by executing a 14 bit CRU read operation (addresses 1-14). The software example (Table 3) shows a read of the event timer.

The current status of the machine can always be obtained by reading the control (address zero) bit. A "0" indicates the machine is in an interrupt mode. Bits 1 thru 15 would normally be the interrupt input lines in this mode, but if any are not needed for interrupts they may also be read with a CRU input command and interpreted as normal data inputs. A "1" read on the control bit indicates that the 9901 is in the clock mode. Reading bits 1 thru 14 completes the event timer operation as described above. Reading bit 15 indicates whether the interrupt request line is active.

A software reset $\overline{RST}$2 can be performed by writing a "1" to the control bit followed by writing a "1" to bit 15, which forces all I/O ports to the input mode.

2.6 SYSTEM OPERATION

During power up $\overline{RST}$I must be activated (low) for a minimum of 2 clock cycles to force the TMS 9901 into a known state. $\overline{RST}$1 will disable all interrupts, disable the clock, program all I/O ports to the input mode, and force IC0-IC3 to (0,0,0,0) with $\overline{INTREQ}$ held high. System software must then enable the proper interrupts, program the clock (if used), and configure the I/O ports as required (See Table 3 for an example). After initial power up, the TMS 9901 will be accessed only as needed to service the clock, enable (disable) interrupts, or read (write) data to the I/O ports. The I/O ports can be reconfigured by use of the $\overline{RST}$2 command bit.

Figure 6 illustrates the use of a TMS 9901 with a TMS 9900. The TIM 9904 is used to generate RST to reset the 9900 and the 9901 (connected to RST1). Figure 7 shows a TMS 9980 system using the TMS 9901. The reset function, load interrupt, and 4 maskable interrupts allowed in a 9980 are encoded as shown in Table 4. Connecting the system as shown ensures that the proper reset will be applied to the 9980.

TABLE 4
9980 INTERRUPT LEVEL DATA

INTERRUPT CODE (IC0–IC2)	FUNCTION	VECTOR LOCATION (MEMORY ADDRESS IN HEX)	DEVICE ASSIGNMENT	INTERRUPT MASK VALUES TO ENABLE (ST12 THROUGH ST15)
1 1 0	Level 4	0 0 1 0	External Device	4 Through F
1 0 1	Level 3	0 0 0 C	External Device	3 Through F
1 0 0	Level 2	0 0 0 8	External Device	2 Through F
0 1 1	Level 1	0 0 0 4	External Device	1 Through F
0 0 1	Reset	0 0 0 0	Reset Stimulus	Don't Care
0 1 0	Load	3 F F C	Load Stimulus	Don't Care
0 0 0	Reset	0 0 0 0	Reset Stimulus	Don't Care
1 1 1	No-Op	------	------	

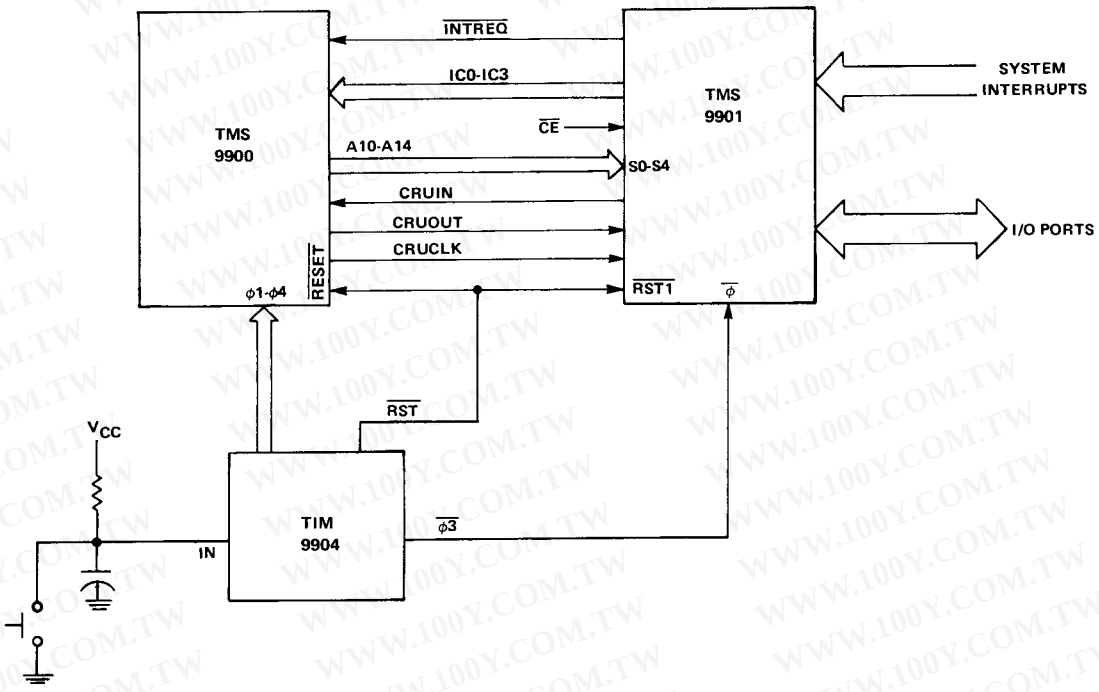


FIGURE 6 – TMS 9900–TMS 9901 INTERFACE

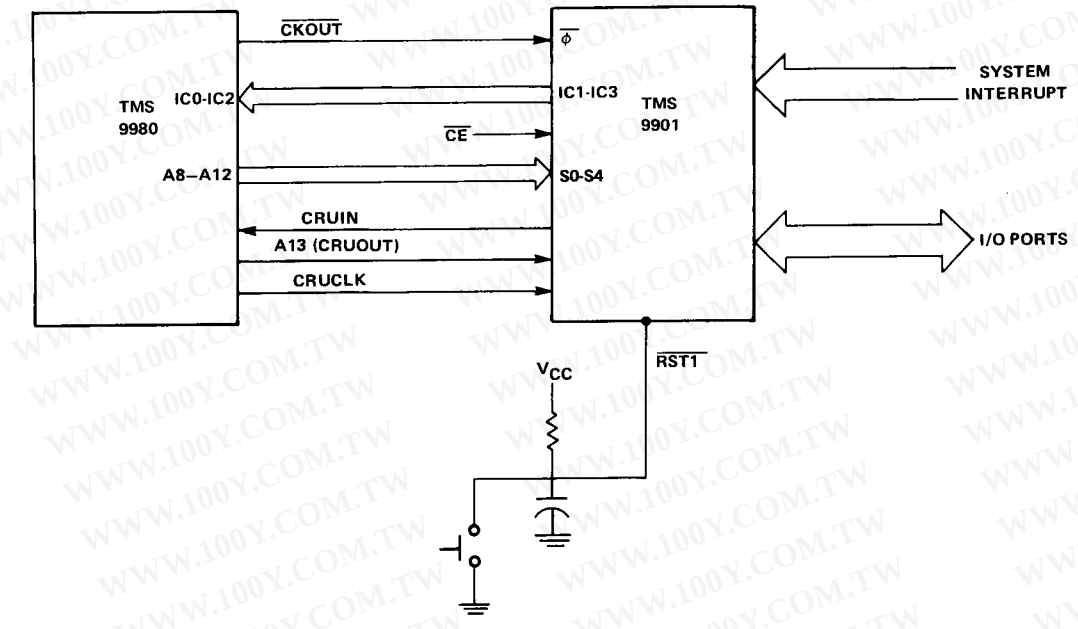


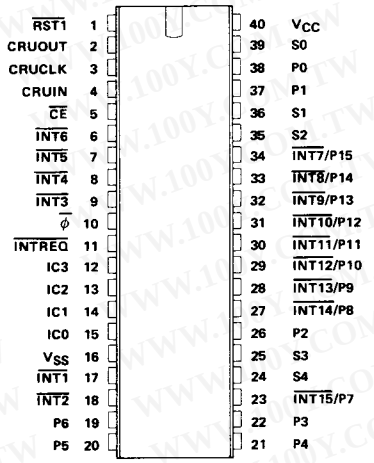
FIGURE 7 – TMS 9980–TMS 9901 INTERFACE

2.7 PIN DEFINITIONS

Table 5 defines the TMS 9901 pin assignments and describes the function of each pin.

TABLE 5
TMS 9901 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{\text{INTREQ}}$	11	OUT	INTERRUPT Request. When active (low) $\overline{\text{INTREQ}}$ indicates that an enabled interrupt has been received. $\overline{\text{INTREQ}}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0-IC3 output the binary code corresponding to the highest priority enabled interrupt. If no enabled interrupts are active IC0—IC3 = (1,1,1,1).
IC1	14	OUT	
IC2	13	OUT	
IC3 (LSB)	12	OUT	
$\overline{\text{CE}}$	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. $\overline{\text{CE}}$ has no effect on the interrupt control section.
S0	39	IN	Address select lines. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0-S4.
S1	36	IN	
S2	35	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{\text{CE}}$ is not active CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{\text{CE}}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0-S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{\text{RST}}$1	1	IN	Power Up Reset. When active (low) $\overline{\text{RST}}$1 resets all interrupt masks to "0", disables the clock, and programs all I/O ports to inputs. $\overline{\text{RST}}$1 has a Schmitt-Trigger input to allow implementation with an RC circuit as shown in Figure 6.
V_{CC}	40		Supply Voltage. +5 V nominal.
V_{SS}	16		Ground Reference
$\overline{\phi}$	10		System clock ($\overline{\phi}$3 in TMS 9900 system, $\overline{\text{CKOUT}}$ in TMS 9980 system).
$\overline{\text{INT}}$1	17	IN	Group 1, interrupt inputs. When active.
$\overline{\text{INT}}$2	18	IN	(Low) the signal is ANDed with its corresponding mask bit and if enabled sent to the interrupt control section.
$\overline{\text{INT}}$3	9	IN	INT1 has highest priority.
$\overline{\text{INT}}$4	8	IN	
$\overline{\text{INT}}$5	7	IN	
$\overline{\text{INT}}$6	6	IN	
$\overline{\text{INT}}$7/ P15	34	I/O	Group 2, programmable interrupt (active low) or I/O pins (true logic). Each pin is individually programmable as an interrupt, an input port, or an output port.
$\overline{\text{INT}}$8/ P14	33	I/O	
$\overline{\text{INT}}$9/ P13	32	I/O	
$\overline{\text{INT}}$10/P12	31	I/O	
$\overline{\text{INT}}$11/P11	30	I/O	
$\overline{\text{INT}}$12/P10	29	I/O	
$\overline{\text{INT}}$13/P9	28	I/O	
$\overline{\text{INT}}$14/P8	27	I/O	
$\overline{\text{INT}}$15/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as an input port or an output port.
P1	37	I/O	
P2	26	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	



3. TMS 9901 ELECTRICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltages, V_{CC} and V_{SS}	−0.3 V to 10 V
All input and output voltages	−0.3 V to 10 V
Continuous power dissipation	0.75 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.2	2.4	V_{cc}	V
Low-level input voltage, V_{IL}		0.8	0.8	V
Operating free-air temperature, T_A	0	25	70	°C

3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

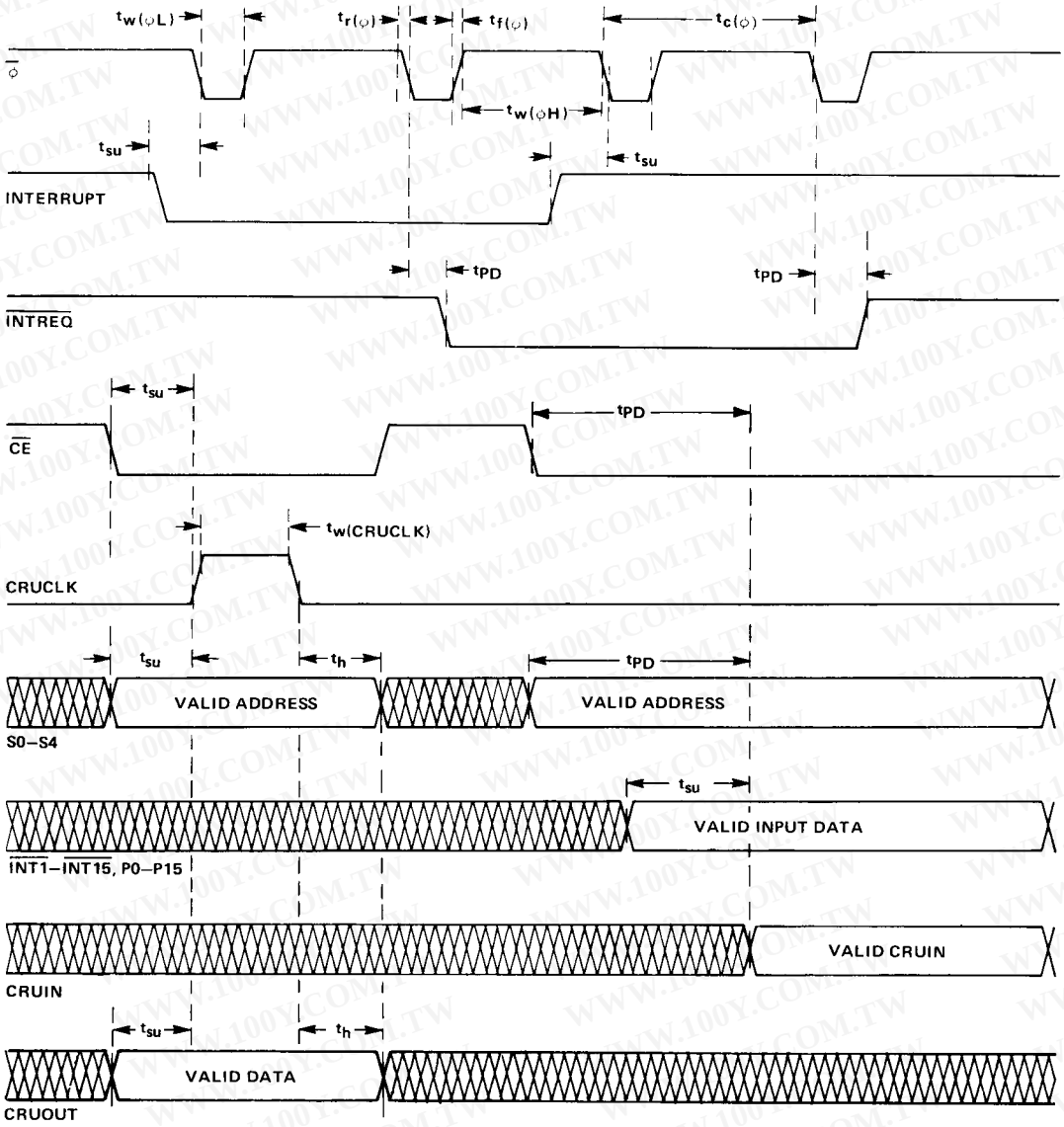
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current (any input)	V_I = 0 V to V_{CC}		±10	±100	μA
V_{OH}	High level output voltage	I_{OH} = −100 μA	2.4	2.4		V
		I_{OH} = −400 μA	2.0	2		V
V_{OL}	Low level output voltage	I_{OL} = 3.2 mA		0.4	0.65	V
I_{CC}	Supply current from V_{CC}			100		mA
I_{SS}	Supply current from V_{SS}			200	200	mA
$I_{CC(av)}$	Average supply current from V_{CC}	$t_{c(\phi)}$ = 333 ns, T_A = 25°C		60	200	mA
C_i	Capacitance, any input	f = 1 MHz, All other		10	15	pF
C_o	Capacitance, any output	Pins at 0 V		20	25	pF

3.4 TIMING REQUIREMENTS OVER FULL RANGE OF OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time	300	333	2000	ns
$t_{r(\phi)}$	Clock rise time	10	10		ns
$t_{f(\phi)}$	Clock fall time	10	10		ns
$t_{w(\phi L)}$	Clock pulse low width	45	55		ns
$t_{w(\phi H)}$	Clock pulse high width	200	240		ns
t_{su}	Setup time for S0-S4, $\overline{CE}$, or CRUOUT before CRUCLK		200	330	ns
t_{su}	Setup time, input before valid CRUIN		200	330	ns
t_{su}	Setup time, interrupt before $\overline{\phi}$ low		40	65	ns
$t_{w(CRUCLK)}$	CRU clock pulse width	90	100	300	ns
t_h	Address hold time	80			ns

3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay, $\overline{\phi}$ low to valid $\overline{INTREQ}$, I_{C0}–I_{C3}	C_L = 100 pF, 2 TTL loads		80	110	ns
t_{PD}	Propagation delay, S0-S4 or $\overline{CE}$ to valid CRUIN	C_L = 100 pF		300	400	ns

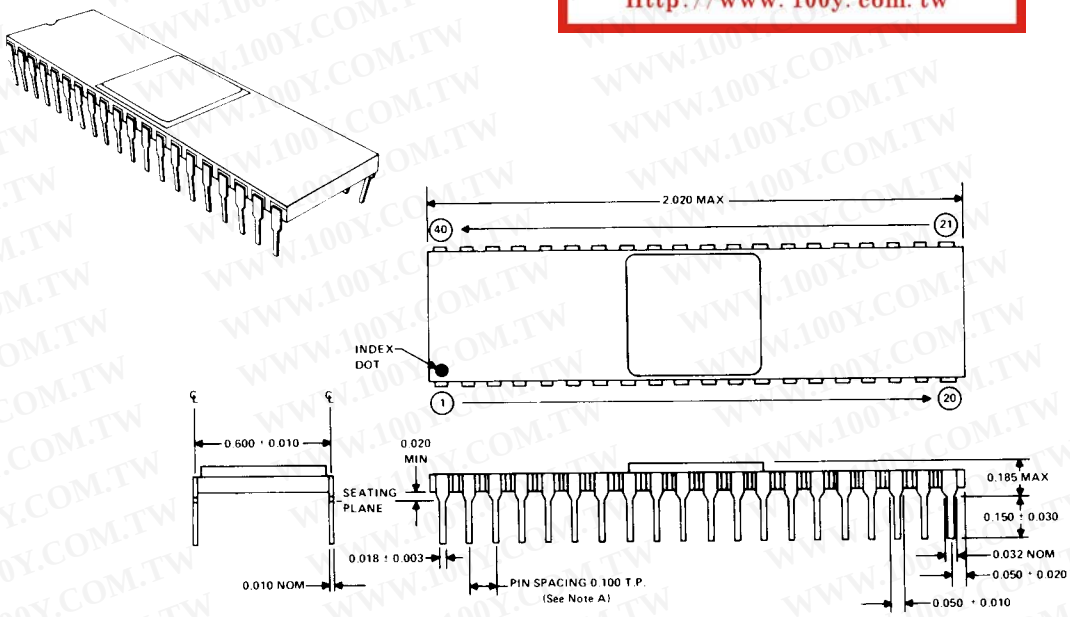


NOTE 1: ALL TIMING MEASUREMENTS ARE FROM 10% and 90% POINTS

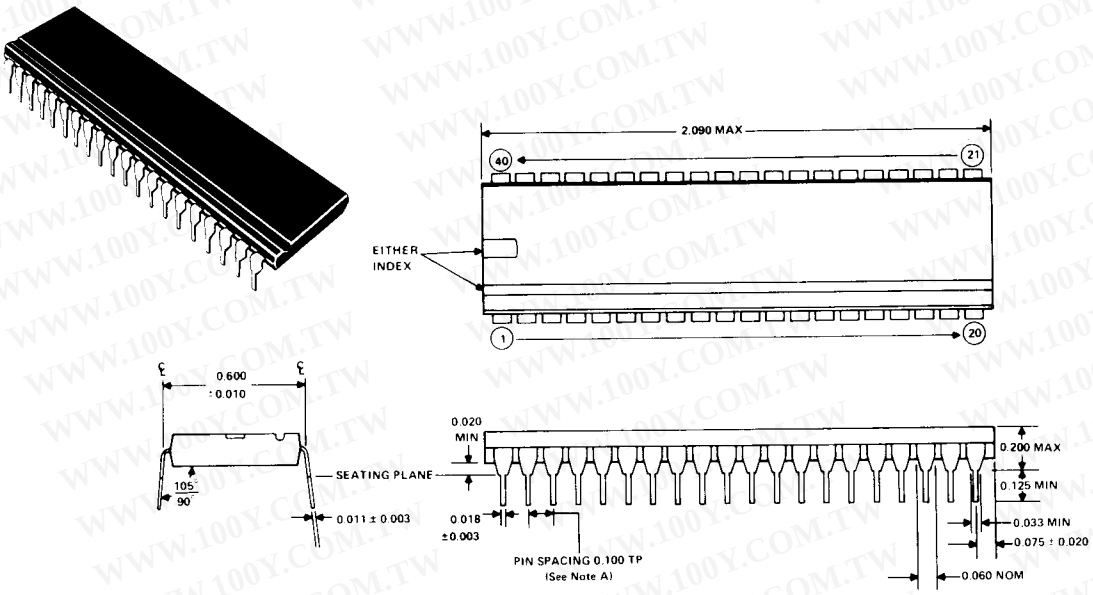
FIGURE 8 – SWITCHING CHARACTERISTICS

4. MECHANICAL DATA

4.1 TMS 9901 – 40 PIN CERAMIC PACKAGE



4.2 TMS 9901 – 40 PIN PLASTIC PACKAGE



NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.