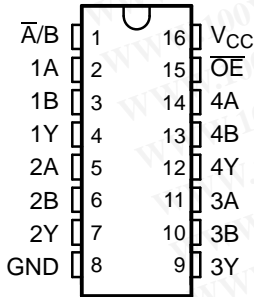


FEATURES

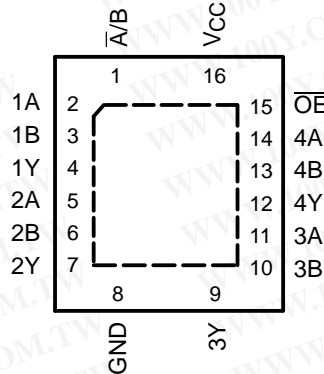
- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.6 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$

- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

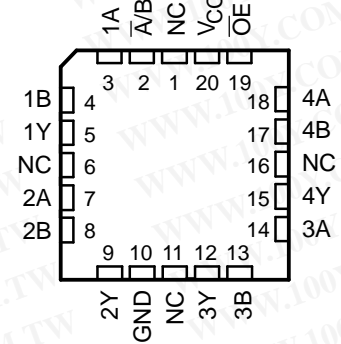
SN54LVC257A ... J OR W PACKAGE
SN74LVC257A ... D, DB, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC257A ... RGY PACKAGE
(TOP VIEW)



SN54LVC257A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable (\overline{OE}) input is at a high logic level.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LVC257ARGYR | LC257A |
| | | Tube of 40 | SN74LVC257AD | LVC257A |
| | SOIC – D | Reel of 2500 | SN74LVC257ADR | |
| | | Reel of 250 | SN74LVC257ADT | |
| | SOP – NS | Reel of 2000 | SN74LVC257ANSR | LVC257A |
| | SSOP – DB | Reel of 2000 | SN74LVC257ADBR | LC257A |
| | | | Tube of 90 | SN74LVC257APW |
| | | TSSOP – PW | Reel of 2000 | SN74LVC257APWR |
| Reel of 250 | | | SN74LVC257APWT | |
| –55°C to 125°C | CDIP – J | Tube of 25 | SNJ54LVC257AJ | SNJ54LVC257AJ |
| | CFP – W | Tube of 150 | SNJ54LVC257AW | SNJ54LVC257AW |
| | LCCC – FK | Tube of 55 | SNJ54LVC257AFK | SNJ54LVC257AFK |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LVC257A, SN74LVC257A
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

SCAS294N–JANUARY 1993–REVISED JUNE 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

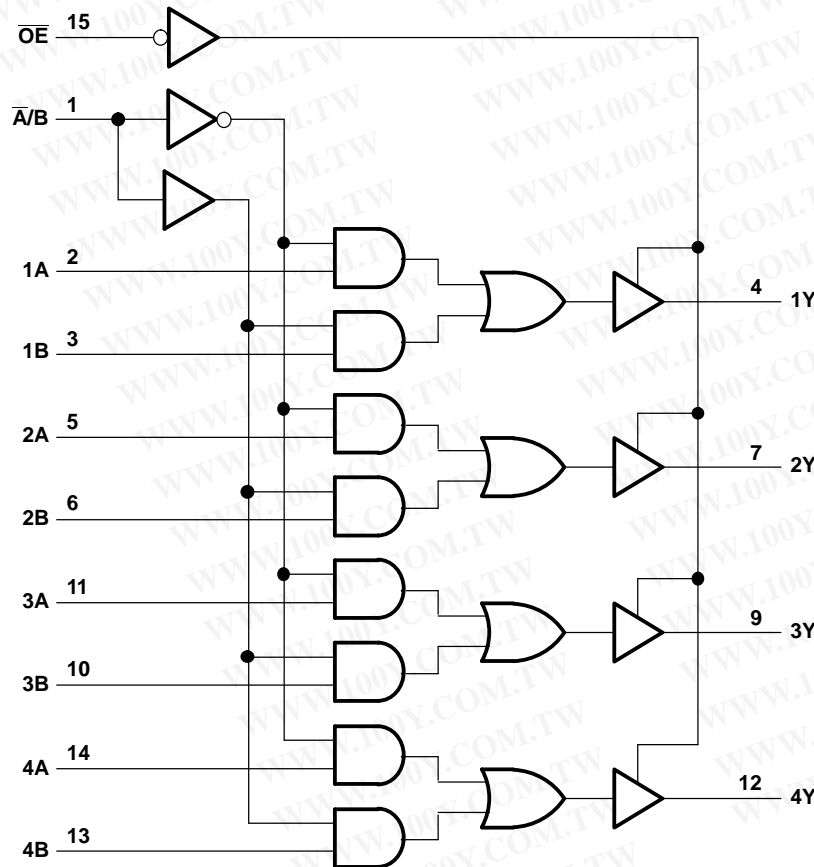
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

| \overline{OE} | INPUTS | | | OUTPUT Y |
|-----------------|--------|---|---|-------------|
| | A/B | A | B | |
| H | X | X | X | Z |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, DB, J, NS, PW, RGY, and W packages.

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|--|----------------------------|----------------|------|
| V_{CC} | Supply voltage range | –0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | –0.5 | 6.5 | V |
| V_O | Output voltage range ⁽²⁾⁽³⁾ | –0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | –50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | –50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance | D package ⁽⁴⁾ | 73 | °C/W |
| | | DB package ⁽⁴⁾ | 82 | |
| | | NS package ⁽⁴⁾ | 64 | |
| | | PW package ⁽⁴⁾ | 108 | |
| | | RGY package ⁽⁵⁾ | 39 | |
| T_{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

| | | SN54LVC257A | | SN74LVC257A | | UNIT | |
|---------------------|------------------------------------|---|----------|-------------|----------------------|------|----|
| | | MIN | MAX | MIN | MAX | | |
| V_{CC} | Supply voltage | Operating | 2 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | |
| V_{IH} | High-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | | | $0.65 \times V_{CC}$ | | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | | 1.7 | | |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2 | | 2 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | | | $0.35 \times V_{CC}$ | | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | | 0.7 | | |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | | 0.8 | 0.8 | | |
| V_I | Input voltage | 0 | 5.5 | 0 | 5.5 | V | |
| V_O | Output voltage | 0 | V_{CC} | 0 | V_{CC} | V | |
| I_{OH} | High-level output current | $V_{CC} = 1.65\text{ V}$ | | | | –4 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | | | | –8 | |
| | | $V_{CC} = 2.7\text{ V}$ | | –12 | | –12 | |
| | | $V_{CC} = 3\text{ V}$ | | –24 | | –24 | |
| I_{OL} | Low-level output current | $V_{CC} = 1.65\text{ V}$ | | | | 4 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | | | | 8 | |
| | | $V_{CC} = 2.7\text{ V}$ | | 12 | | 12 | |
| | | $V_{CC} = 3\text{ V}$ | | 24 | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V | |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVC257A, SN74LVC257A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SCAS294N–JANUARY 1993–REVISED JUNE 2005

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN54LVC257A | | | SN74LVC257A | | | UNIT |
|--------------------------|---|-----------------|-----------------------|--------------------|------|-----------------------|--------------------|-----|------|
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | |
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 3.6 V | | | | V _{CC} - 0.2 | | | V |
| | I _{OH} = -100 μA | 2.7 V to 3.6 V | V _{CC} - 0.2 | | | | | | |
| | I _{OH} = -4 mA | 1.65 V | | | | 1.2 | | | |
| | I _{OH} = -8 mA | 2.3 V | | | | 1.7 | | | |
| | I _{OH} = -12 mA | 2.7 V | 2.2 | | | 2.2 | | | |
| | | 3 V | 2.4 | | | 2.4 | | | |
| I _{OH} = -24 mA | 3 V | 2.2 | | | 2.2 | | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | | 0.2 | | | V |
| | | 2.7 V to 3.6 V | 0.2 | | | | | | |
| | I _{OL} = 4 mA | 1.65 V | | | | 0.45 | | | |
| | I _{OL} = 8 mA | 2.3 V | | | | 0.7 | | | |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | | 0.4 | | | |
| 3 V | | 0.55 | | | 0.55 | | | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | | | | ±5 | | | μA |
| I _{OZ} | V _O = V _{CC} or GND | 3.6 V | | | | ±15 | | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | | | 10 | | | μA |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | 500 | | | 500 | | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 5 | | | 5 | | | pF |
| C _o | V _O = V _{CC} or GND | 3.3 V | 5 | | | 5 | | | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVC257A | | | | UNIT |
|--------------------|-------------------|-------------|-------------------------|-----|---------------------------------|-----|------|
| | | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | 5.4 | | 1 4.6 | | ns |
| | \bar{A}/\bar{B} | | 7.5 | | 1 6.4 | | |
| t _{en} | \bar{OE} | Y | 6.7 | | 1 5.6 | | ns |
| t _{dis} | \bar{OE} | Y | 4.7 | | 0.5 4.3 | | ns |
| t _{sk(o)} | | | | | 1 | | ns |

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC257A | | | | | | | | UNIT |
|--------------------|-------------------|-------------|----------------------------------|------|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
| | | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | 1 | 13.5 | 1 | 7.4 | 1 | 5.4 | 1 | 4.6 | ns |
| | \bar{A}/\bar{B} | | 1 | 15.6 | 1 | 9.5 | 1 | 7.5 | 1 | 6.4 | |
| t _{en} | \bar{OE} | Y | 1 | 14.6 | 1 | 8.7 | 1 | 6.7 | 1 | 5.6 | ns |
| t _{dis} | \bar{OE} | Y | 1 | 15.4 | 1 | 6.7 | 1 | 4.7 | 1 | 4.3 | ns |
| t _{sk(o)} | | | | | | | | | 1 | | ns |

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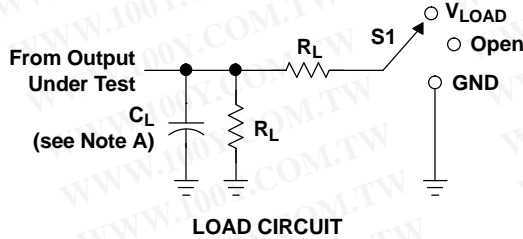
Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|--|---------------------|-------------------------|-------------------------|-------------------------|------|
| | | TYP | TYP | TYP | |
| C_{pd} Power dissipation capacitance | $f = 10\text{ MHz}$ | 13.5 | 14.5 | 15.5 | pF |

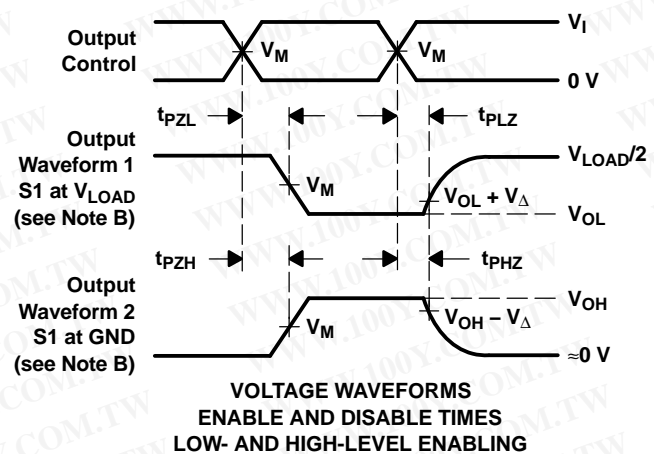
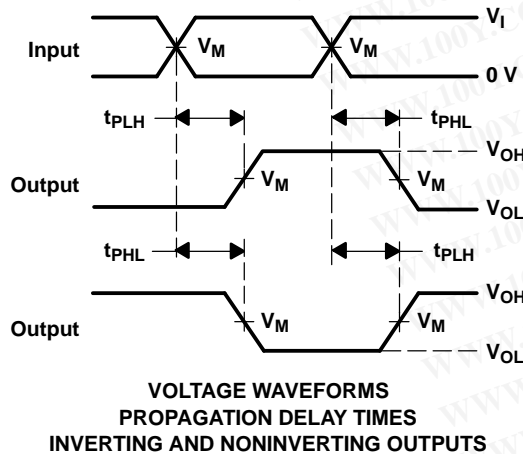
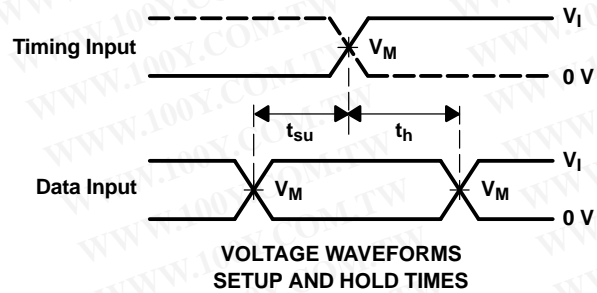
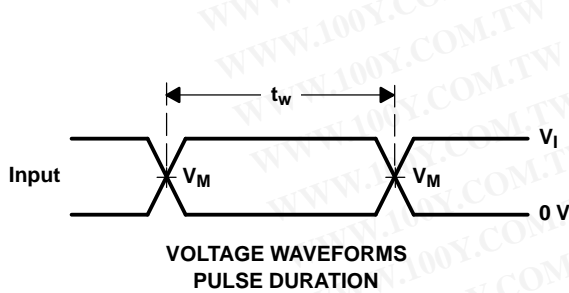
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PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-0050901Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-0050901QEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 5962-0050901QFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| SN74LVC257AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ADBLE | OBSOLETE | SSOP | DB | 16 | | TBD | Call TI | Call TI |
| SN74LVC257ADBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ADBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ADT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ADTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ANSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257APW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257APWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257APWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257APWLE | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI |
| SN74LVC257APWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257APWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257APWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257APWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257APWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257APWTG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC257ARGYR | ACTIVE | QFN | RGY | 16 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |

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| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LVC257ARGYRG4 | ACTIVE | QFN | RGY | 16 | | TBD | Call TI | Call TI |
| SNJ54LVC257AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54LVC257AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54LVC257AW | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

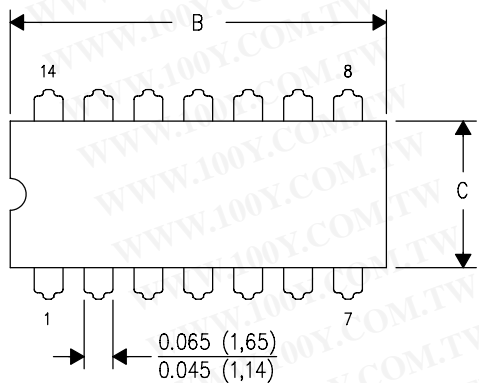
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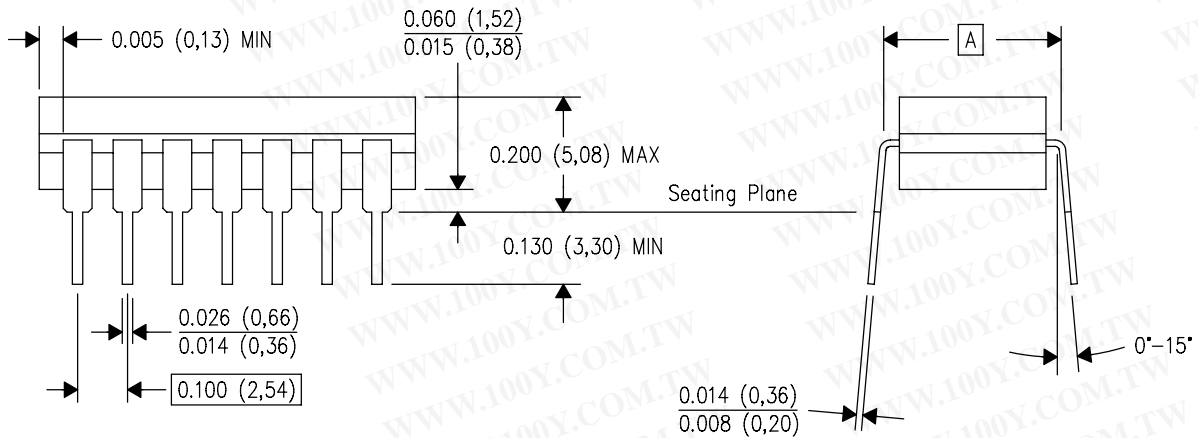
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J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE
 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM | PINS ** | | | |
|-------|------------------------|------------------------|------------------------|------------------------|
| | 14 | 16 | 18 | 20 |
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



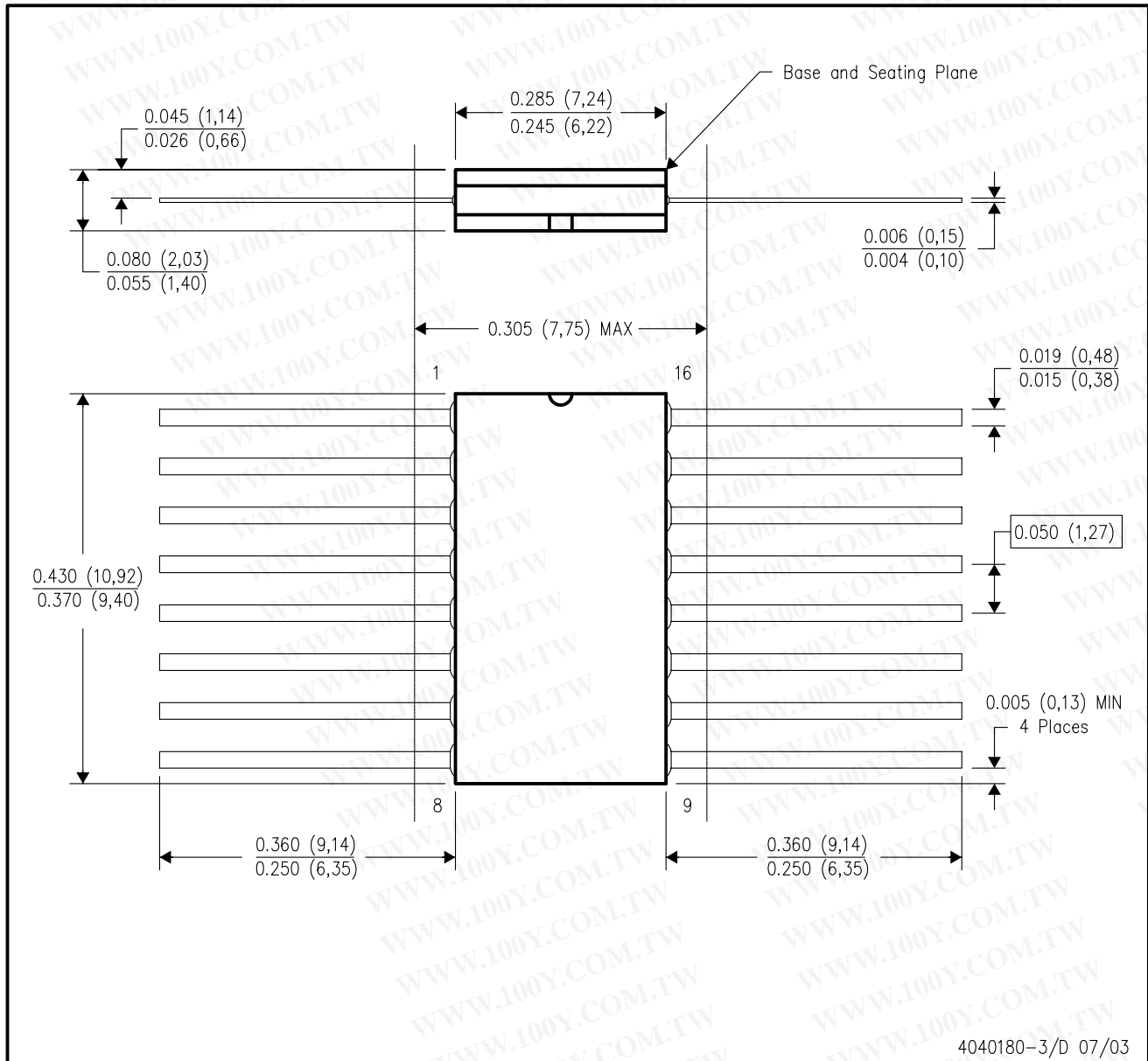
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



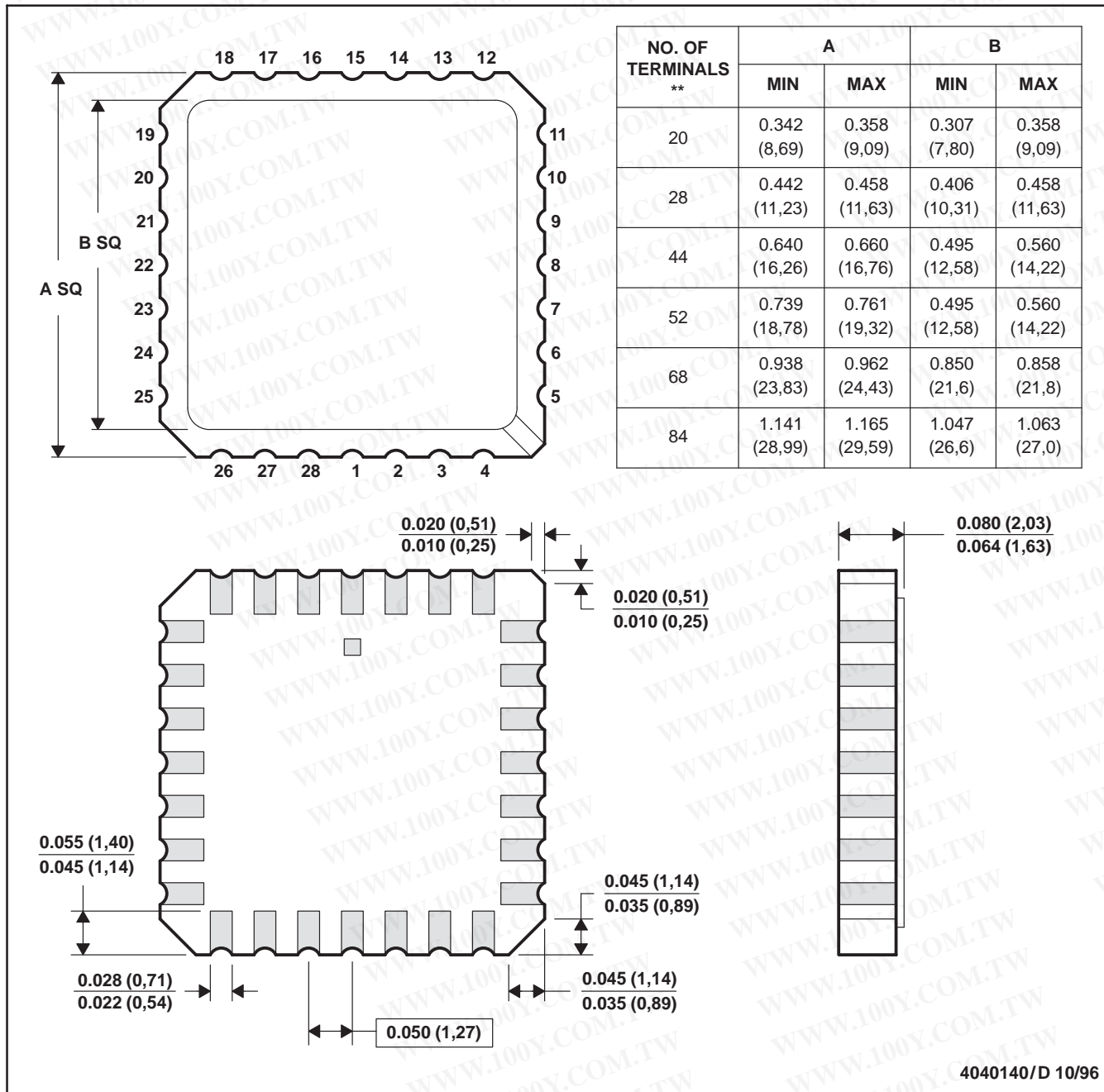
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

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FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

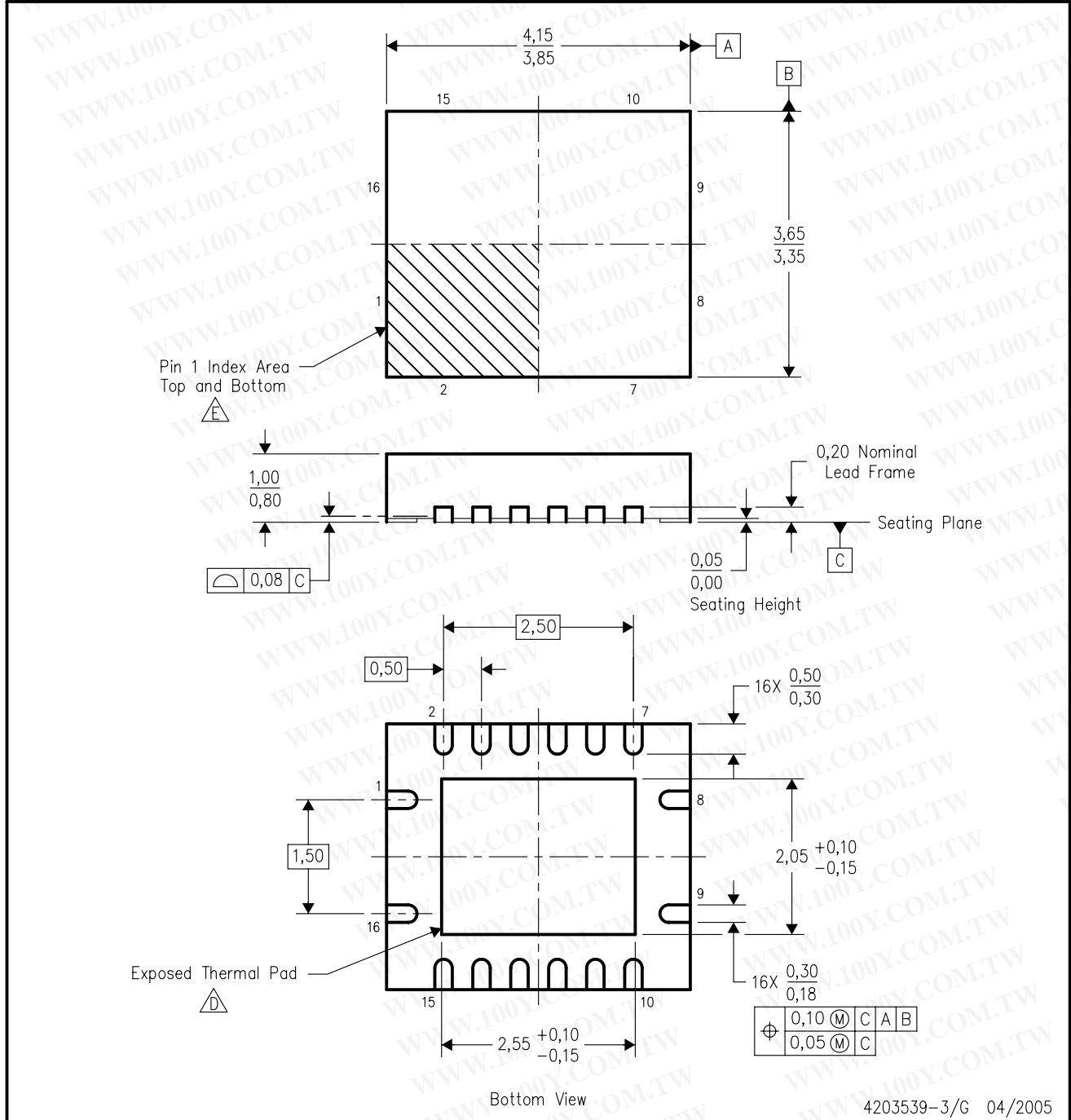


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

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RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK



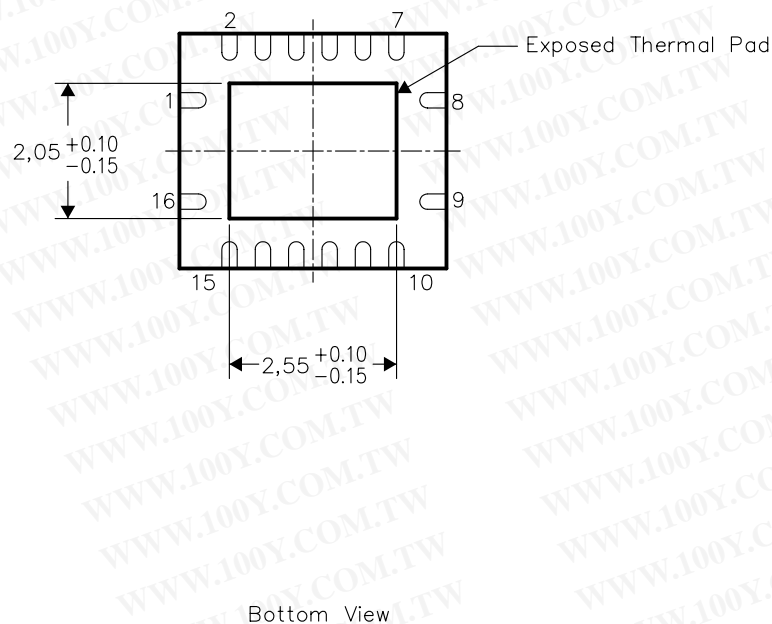
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BB.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

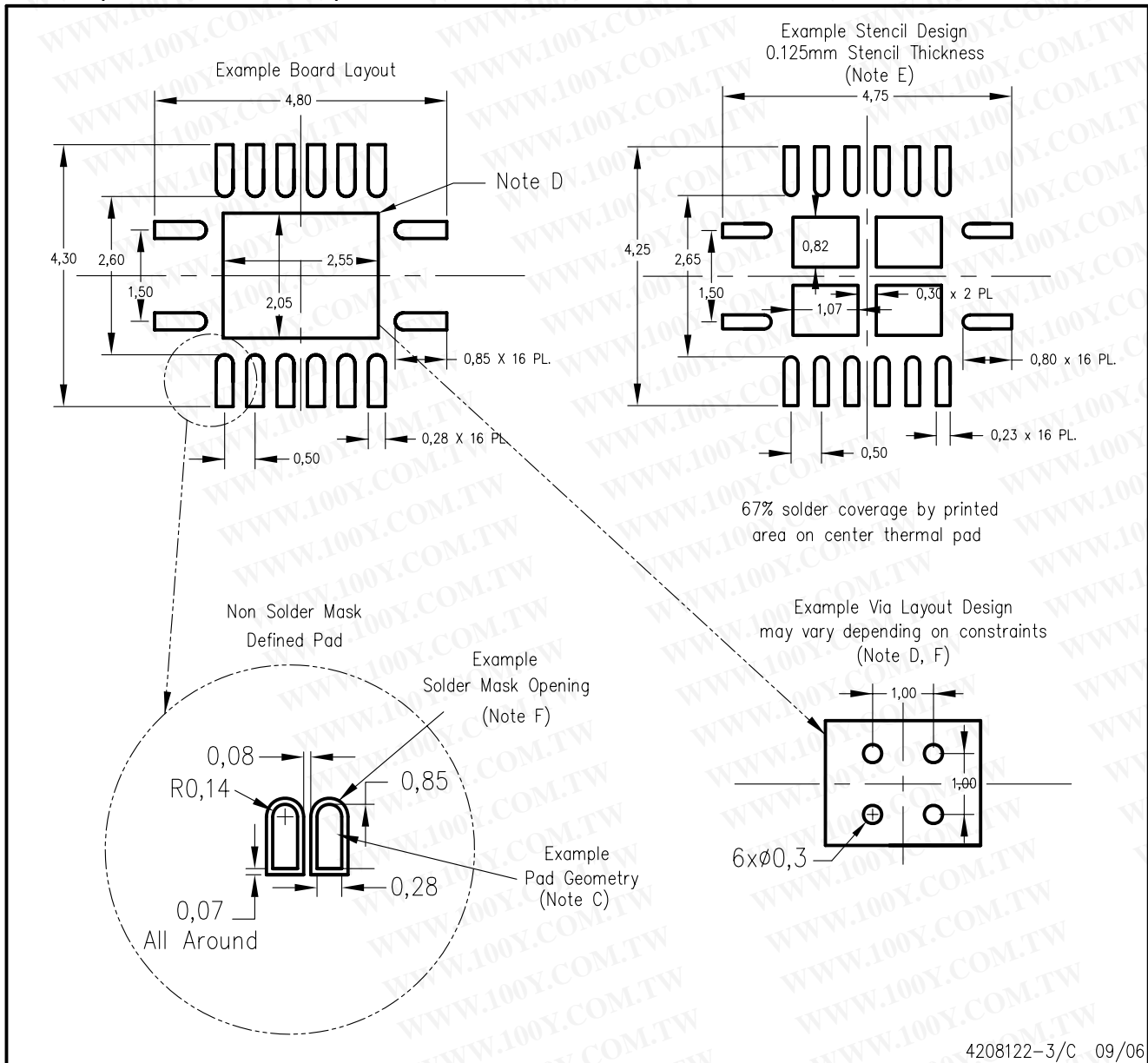


NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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RGY (R-PQFP-N16)



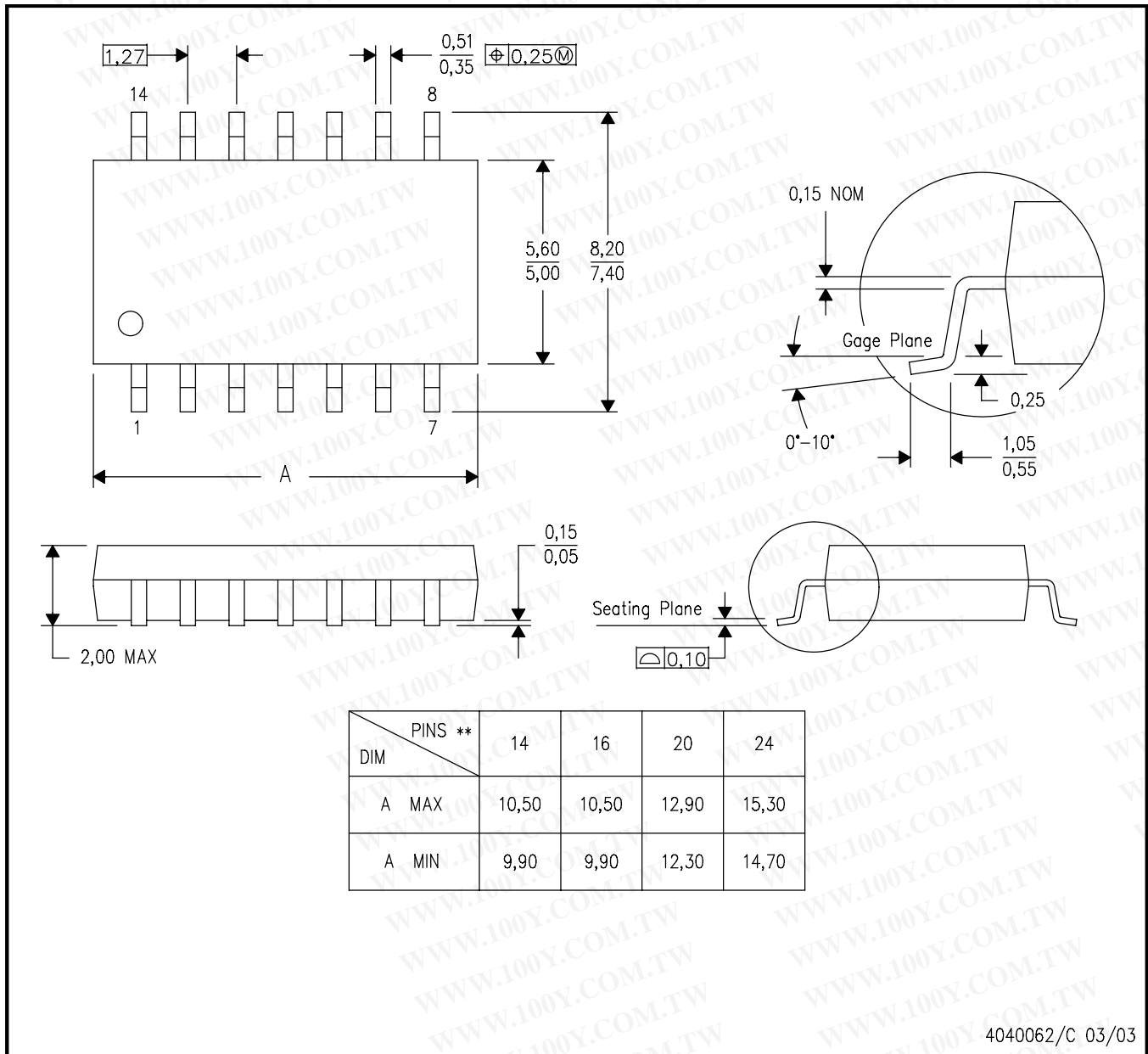
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



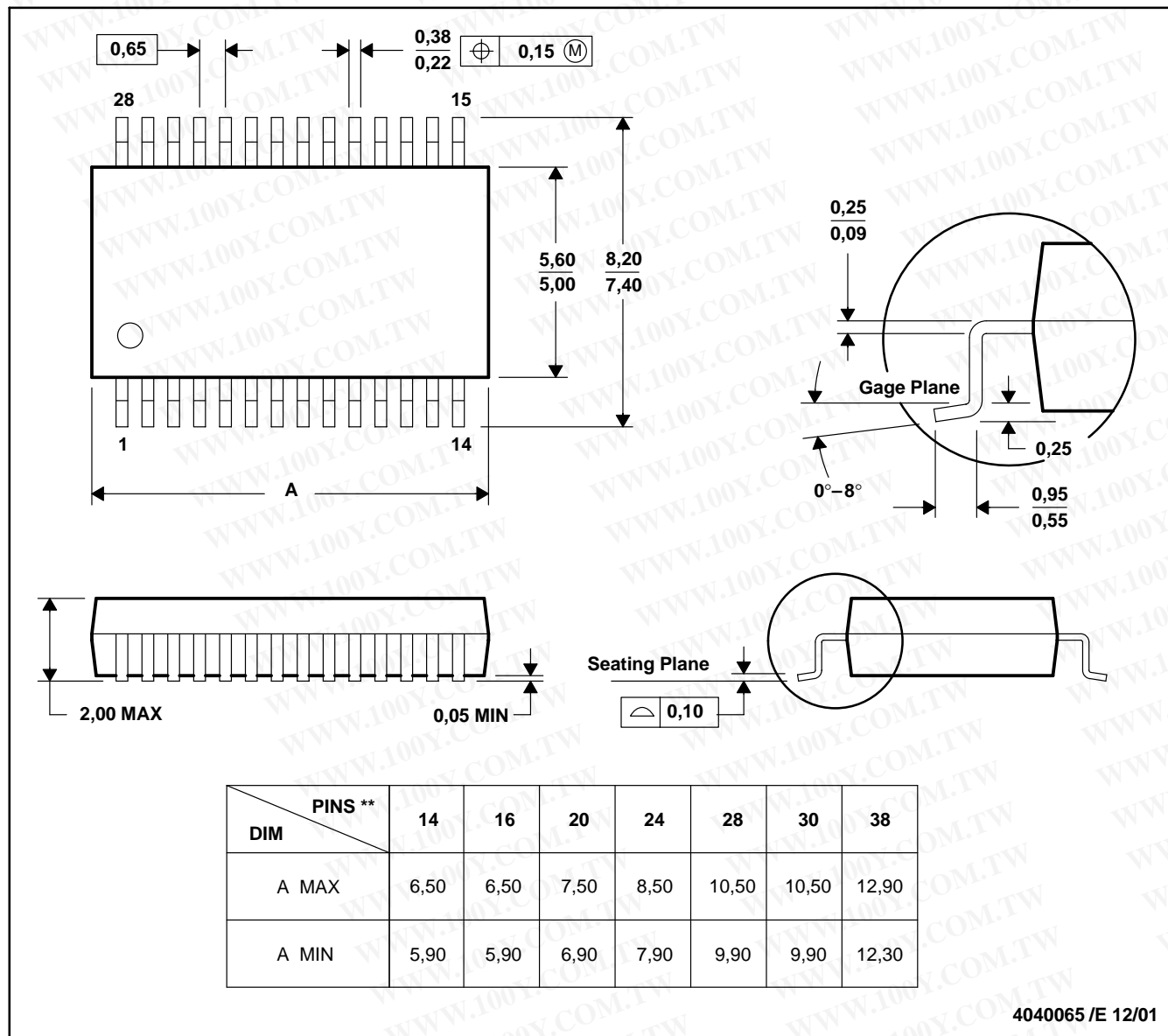
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



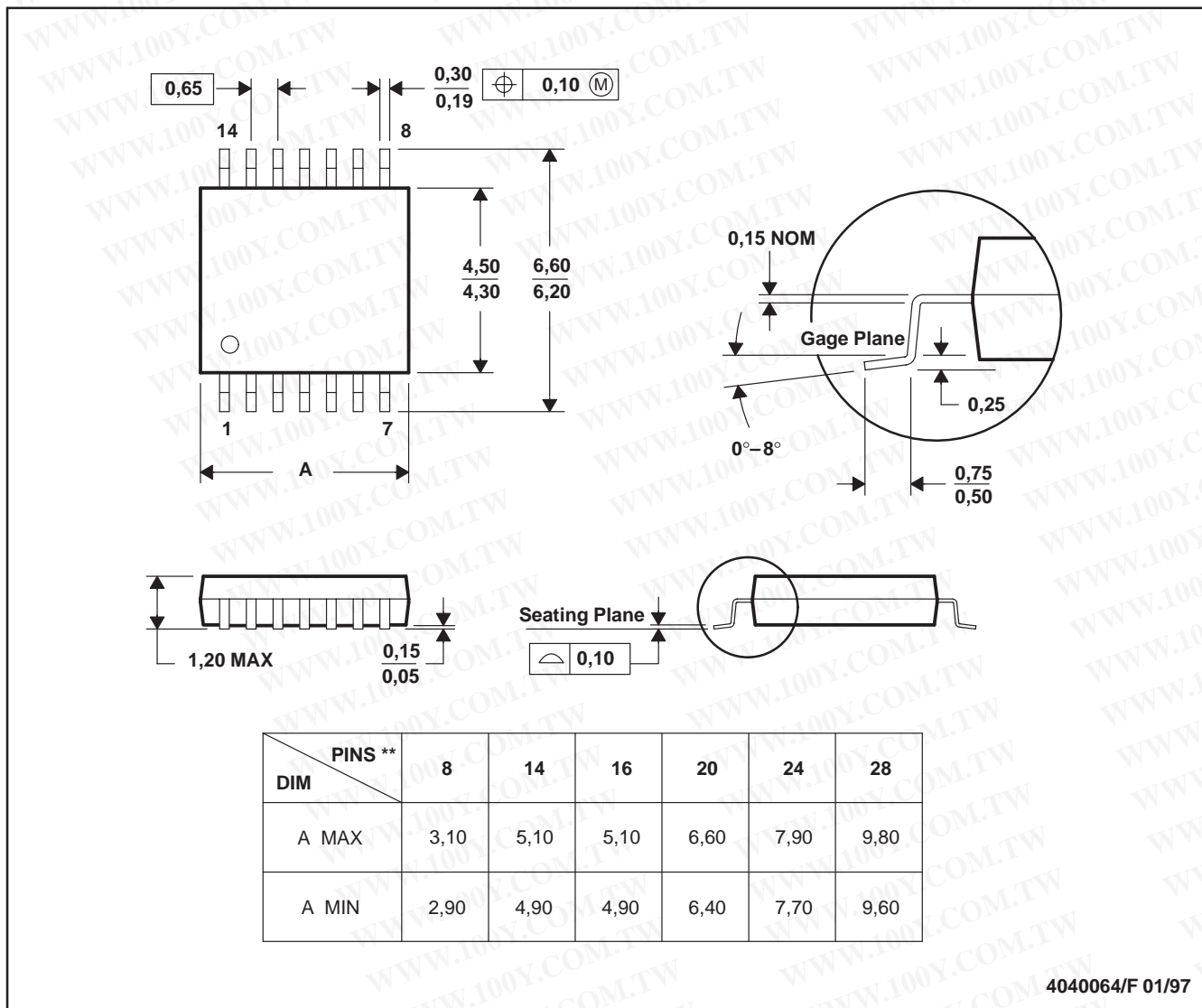
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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