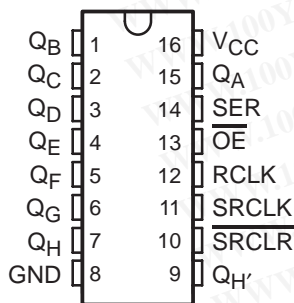
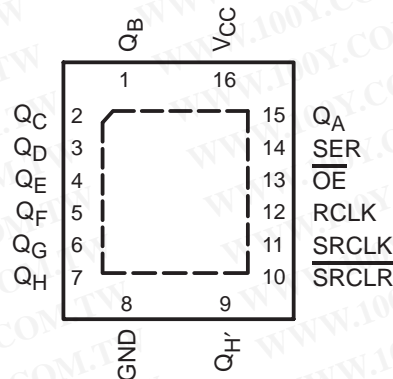


- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 7.1 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- 8-Bit Serial-In, Parallel-Out Shift
- I_{off} Supports Partial-Power-Down Mode Operation
- Shift Register Has Direct Clear
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

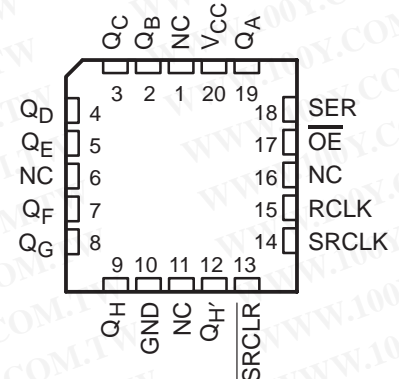
SN54LV595A ... J OR W PACKAGE
 SN74LV595A ... D, DB, NS,
 OR PW PACKAGE
 (TOP VIEW)



SN74LV595A ... RGY PACKAGE
 (TOP VIEW)



SN54LV595A ... FK PACKAGE
 (TOP VIEW)



NC – No internal connection

description/ordering information

The 'LV595A devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING		
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV595ARGYR	LV595A		
	SOIC – D	Tube of 40	SN74LV595AD	LV595A		
		Reel of 2500	SN74LV595ADR			
	–55°C to 125°C	SOP – NS	Reel of 2000	SN74LV595ANSR	74LV595A	
		SSOP – DB	Reel of 2000	SN74LV595ADBR	LV595A	
			Tube of 90	SN74LV595APW		
Reel of 2000			SN74LV595APWR			
–55°C to 125°C	TSSOP – PW	Reel of 250	SN74LV595APWT	LV595A		
		CDIP – J	Tube of 25		SNJ54LV595AJ	SNJ54LV595AJ
		CFP – W	Tube of 150		SNJ54LV595AW	SNJ54LV595AW
	LCCC – FK	Tube of 55	SNJ54LV595AFK	SNJ54LV595AFK		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated

SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

description/ordering information (continued)

These devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{\text{SRCLR}}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{\text{OE}}$) input is high, all outputs except Q_H are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

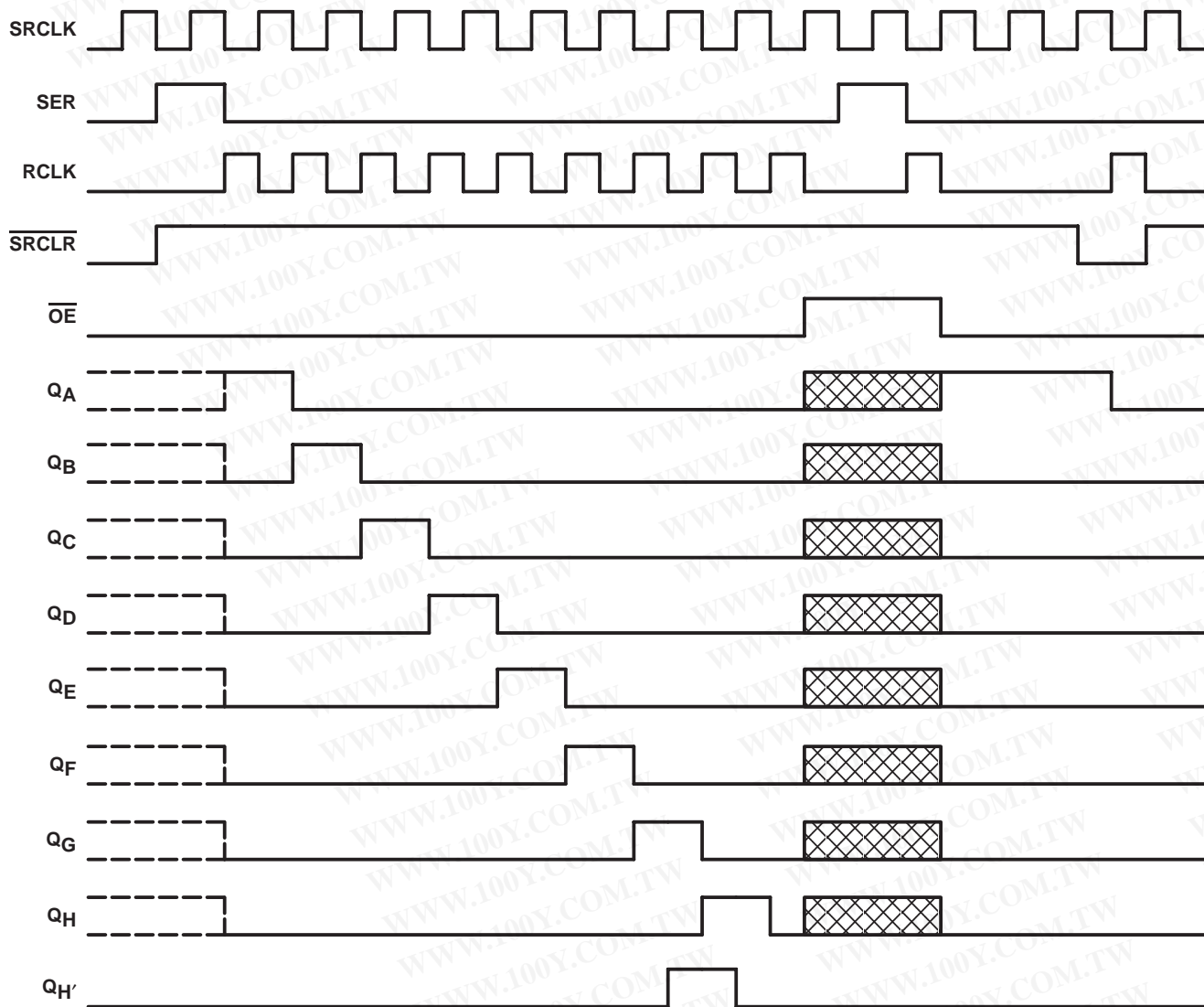
INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled.
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.


勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

timing diagram



NOTE:  implies that the output is in 3-State mode.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



SN54LV595A, SN74LV595A 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

recommended operating conditions (see Note 5)

		SN54LV595A		SN74LV595A		UNIT	
		MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	2	5.5	2	5.5	V	
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	0.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
V_I	Input voltage	0	5.5	0	5.5	V	
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	μA	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		-2	-2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		-8	-8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-16	-16		
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	μA	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		2	2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		8	8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		16	16		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		200	200	ns/V	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		100	100		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		20	20		
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$	

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV595A			SN74LV595A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	Q _{H'}	3 V	2.48			2.48			
	Q _A -Q _H		2.48			2.48			
	Q _{H'}	4.5 V	3.8			3.8			
	Q _A -Q _H		3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V				0.1			V
	I _{OL} = 2 mA	2.3 V				0.4			
	Q _{H'}	3 V				0.44			
	Q _A -Q _H					0.44			
	Q _{H'}	4.5 V				0.55			
	Q _A -Q _H					0.55			
I _I	V _I = 5.5 V or GND	0 to 5.5 V				±1			μA
I _{OZ}	V _O = V _{CC} or GND, Q _A -Q _H	5.5 V				±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V				20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0				5			μA
C _i	V _I = V _{CC} or GND	3.3 V	3.5			3.5			pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54LV595A		SN74LV595A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	SRCLK high or low	7		7.5		7.5		ns
		RCLK high or low	7		7.5		7.5		
		SRCLR low	6		6.5		6.5		
t _{su}	Setup time	SER before SRCLK↑	5.5		5.5		5.5		ns
		SRCLK↑ before RCLK↑†	8		9		9		
		SRCLR low before RCLK↑	8.5		9.5		9.5		
		SRCLR high (inactive) before SRCLK↑	4		4		4		
t _h	Hold time	SER after SRCLK↑	1.5		1.5		1.5		ns

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV595A, SN74LV595A 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV595A		SN74LV595A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	5.5	5.5	5.5	5.5	ns	
		RCLK high or low	5.5	5.5	5.5			
		\overline{SRCLR} low	5	5	5			
t_{su}	Setup time	SER before SRCLK \uparrow	3.5	3.5	3.5	ns		
		SRCLK \uparrow before RCLK $\uparrow\uparrow$	8	8.5	8.5			
		\overline{SRCLR} low before RCLK \uparrow	8	9	9			
		\overline{SRCLR} high (inactive) before SRCLK \uparrow	3	3	3			
t_h	Hold time	SER after SRCLK \uparrow	1.5	1.5	1.5	ns		

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV595A		SN74LV595A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	5	5	5	5	ns	
		RCLK high or low	5	5	5			
		\overline{SRCLR} low	5.2	5.2	5.2			
t_{su}	Setup time	SER before SRCLK \uparrow	3	3	3	ns		
		SRCLK \uparrow before RCLK $\uparrow\uparrow$	5	5	5			
		\overline{SRCLR} low before RCLK \uparrow	5	5	5			
		\overline{SRCLR} high (inactive) before SRCLK \uparrow	2.5	2.5	2.5			
t_h	Hold time	SER after SRCLK \uparrow	2	2	2	ns		

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

勝特力材料 86-3-5753170
 胜特力电子(上海) 86-21-54151736
 胜特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV595A		SN74LV595A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	65*	80*		45*		45		MHz
			$C_L = 50\text{ pF}$	60	70		40		40		
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 15\text{ pF}$		8.4*	14.2*	1*	15.8*	1	15.8	ns
t_{PHL}					8.4*	14.2*	1*	15.8*	1	15.8	
t_{PLH}	SRCLK	Q_H'			9.4*	19.6*	1*	22.2*	1	22.2	
t_{PHL}					9.4*	19.6*	1*	22.2*	1	22.2	
t_{PHL}	$\overline{\text{SRCLR}}$	Q_H'			8.7*	14.6*	1*	16.3*	1	16.3	
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H			8.2*	13.9*	1*	15*	1	15	
t_{PZL}					10.9*	18.1*	1*	20.3*	1	20.3	
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H			8.3*	13.7*	1*	15.6*	1	15.6	
t_{PLZ}					9.2*	15.2*	1*	16.7*	1	16.7	
t_{PLH}	RCLK	Q_A-Q_H		$C_L = 50\text{ pF}$		11.2	17.2	1	19.3	1	
t_{PHL}					11.2	17.2	1	19.3	1	19.3	
t_{PLH}	SRCLK	Q_H'			13.1	22.5	1	25.5	1	25.5	
t_{PHL}					13.1	22.5	1	25.5	1	25.5	
t_{PHL}	$\overline{\text{SRCLR}}$	Q_H'			12.4	18.8	1	21.1	1	21.1	
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H			10.8	17	1	18.3	1	18.3	
t_{PZL}					13.4	21	1	23	1	23	
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H			12.2	18.3	1	19.5	1	19.5	
t_{PLZ}					14	20.9	1	22.6	1	22.6	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV595A, SN74LV595A 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV595A		SN74LV595A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	80*	120*		70*	70			MHz
			C _L = 50 pF	55	105		50	50			
t _{PLH}	RCLK	Q _A -Q _H	C _L = 15 pF		6*	11.9*	1*	13.5*	1	13.5	ns
t _{PHL}					6*	11.9*	1*	13.5*	1	13.5	
t _{PLH}	SRCLK	Q _{H'}			6.6*	13*	1*	15*	1	15	
t _{PHL}					6.6*	13*	1*	15*	1	15	
t _{PHL}	$\overline{\text{SRCLR}}$	Q _{H'}			6.2*	12.8*	1*	13.7*	1	13.7	
t _{PZH}	$\overline{\text{OE}}$	Q _A -Q _H			6*	11.5*	1*	13.5*	1	13.5	
t _{PZL}					7.8*	11.5*	1*	13.5*	1	13.5	
t _{PHZ}	$\overline{\text{OE}}$	Q _A -Q _H			6.1*	14.7*	1*	15.2*	1	15.2	
t _{PLZ}					6.3*	14.7*	1*	15.2*	1	15.2	
t _{PLH}	RCLK	Q _A -Q _H		C _L = 50 pF		7.9	15.4	1	17	1	
t _{PHL}					7.9	15.4	1	17	1	17	
t _{PLH}	SRCLK	Q _{H'}			9.2	16.5	1	18.5	1	18.5	
t _{PHL}					9.2	16.5	1	18.5	1	18.5	
t _{PHL}	$\overline{\text{SRCLR}}$	Q _{H'}			9	16.3	1	17.2	1	17.2	
t _{PZH}	$\overline{\text{OE}}$	Q _A -Q _H			7.8	15	1	17	1	17	
t _{PZL}					9.6	15	1	17	1	17	
t _{PHZ}	$\overline{\text{OE}}$	Q _A -Q _H			8.1	15.7	1	16.2	1	16.2	
t _{PLZ}					9.3	15.7	1	16.2	1	16.2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LV595A, SN74LV595A
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV595A		SN74LV595A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	135*	170*		115*		115		MHz
			$C_L = 50\text{ pF}$	120	140		95		95		
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 15\text{ pF}$	4.3*	7.4*	1*	8.5*	1	8.5	ns	
t_{PHL}				4.3*	7.4*	1*	8.5*	1	8.5		
t_{PLH}	SRCLK	Q_H'		4.5*	8.2*	1*	9.4*	1	9.4		
t_{PHL}				4.5*	8.2*	1*	9.4*	1	9.4		
t_{PHL}	$\overline{\text{SRCLR}}$	Q_H'		4.5*	8*	1*	9.1*	1	9.1		
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H		4.3*	8.6*	1*	10*	1	10		
t_{PZL}				5.4*	8.6*	1*	10*	1	10		
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H		2.4*	6*	1*	7.1*	1	7.1		
t_{PLZ}				2.7*	5.1*	1*	7.2*	1	7.2		
t_{PLH}	RCLK	Q_A-Q_H		$C_L = 50\text{ pF}$	5.6	9.4	1	10.5	1		10.5
t_{PHL}			5.6		9.4	1	10.5	1	10.5		
t_{PLH}	SRCLK	Q_H'	6.4		10.2	1	11.4	1	11.4		
t_{PHL}			6.4		10.2	1	11.4	1	11.4		
t_{PHL}	$\overline{\text{SRCLR}}$	Q_H'	6.4		10	1	11.1	1	11.1		
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H	5.7		10.6	1	12	1	12		
t_{PZL}			6.8		10.6	1	12	1	12		
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H	3.5		10.3	1	11	1	11		
t_{PLZ}			3.4		10.3	1	11	1	11		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 6)

PARAMETER		SN74LV595A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	111	pF
			5 V	114	

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

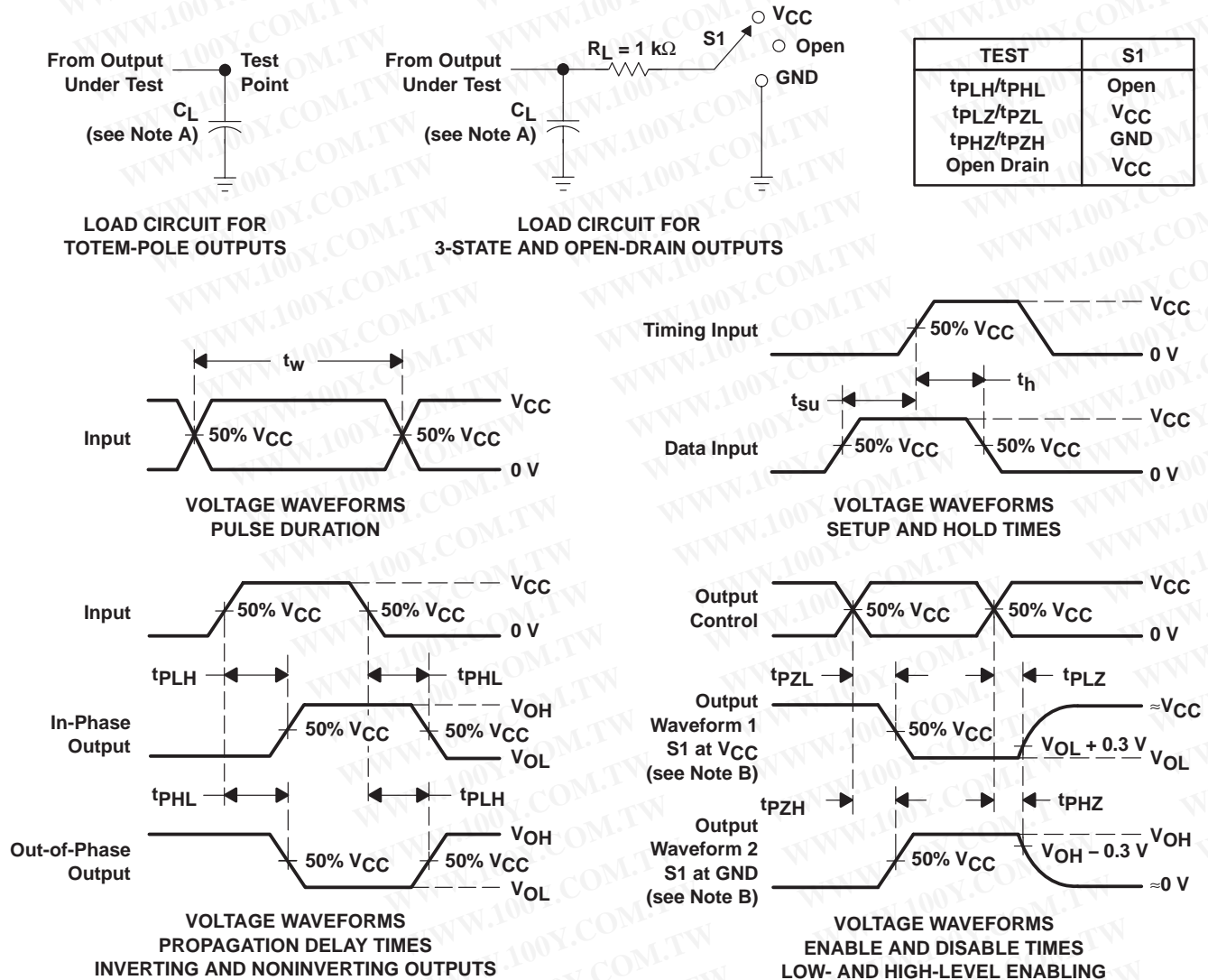


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV595A, SN74LV595A 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS414N – APRIL 1998 – REVISED APRIL 2005

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV595AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV595ARGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LV595ARGYRG4	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

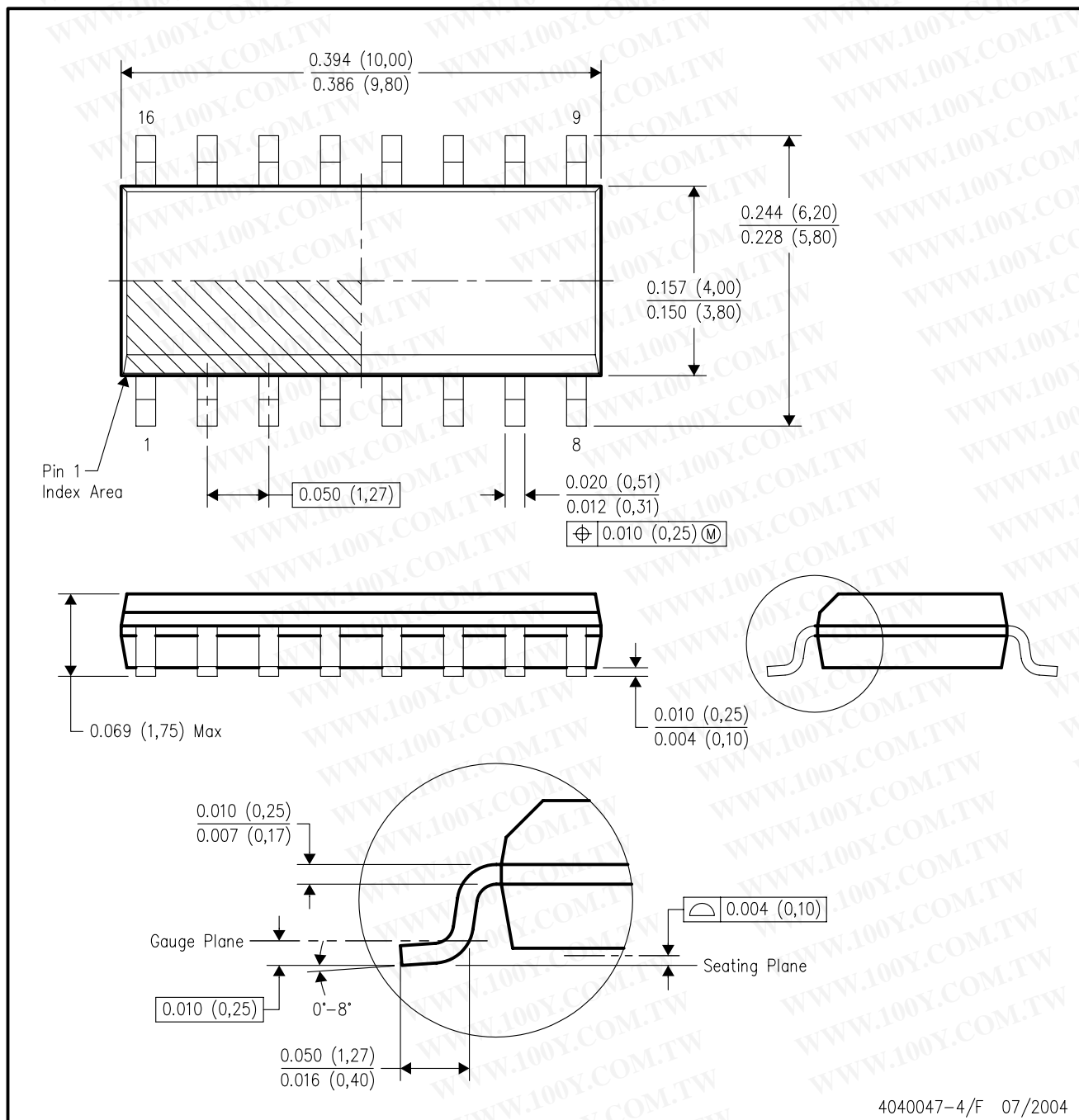
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

D (R-PDSO-G16)

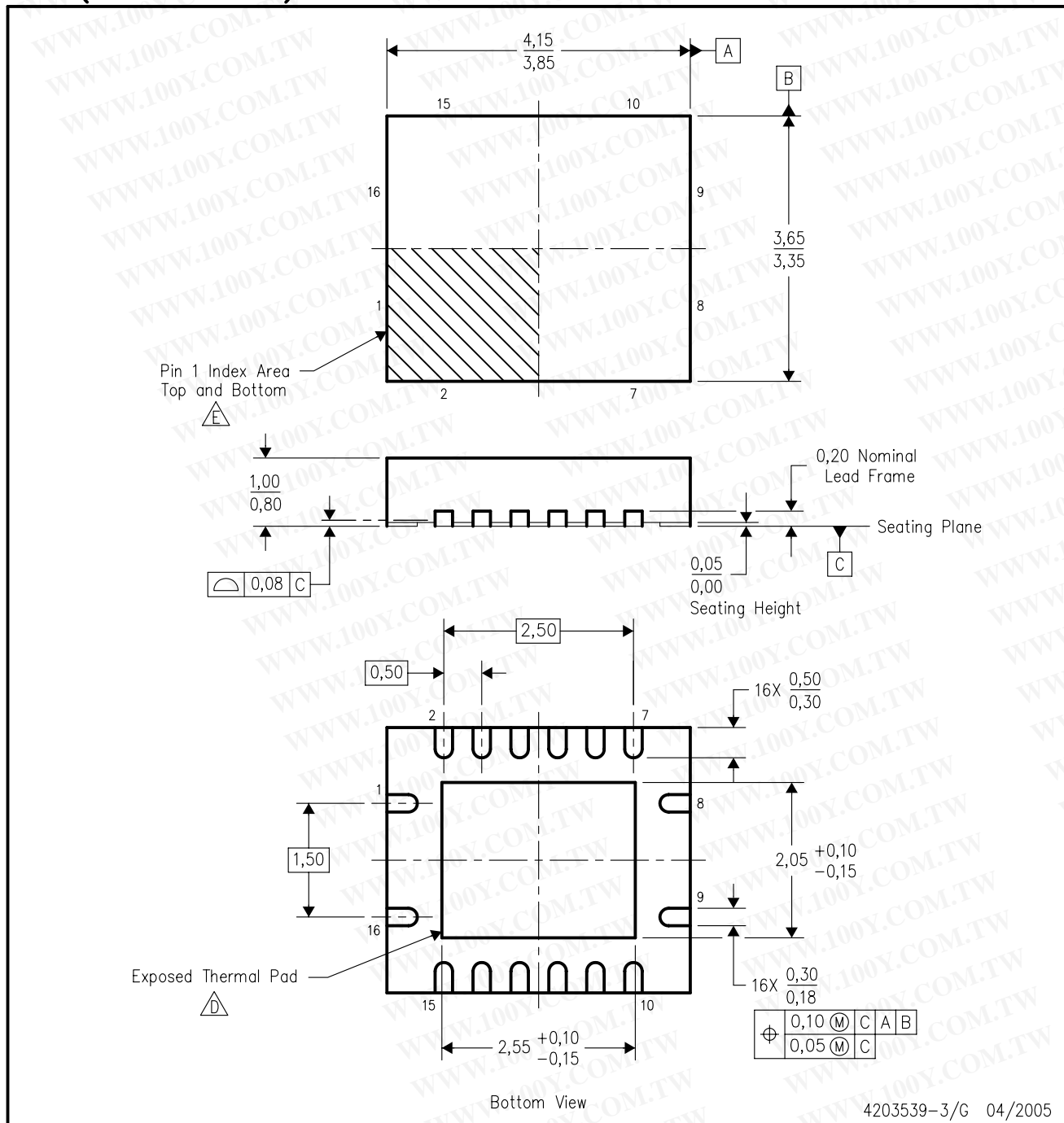
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK



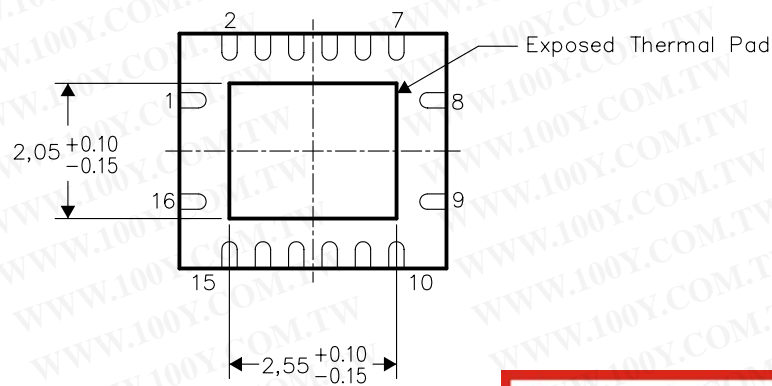
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BB.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



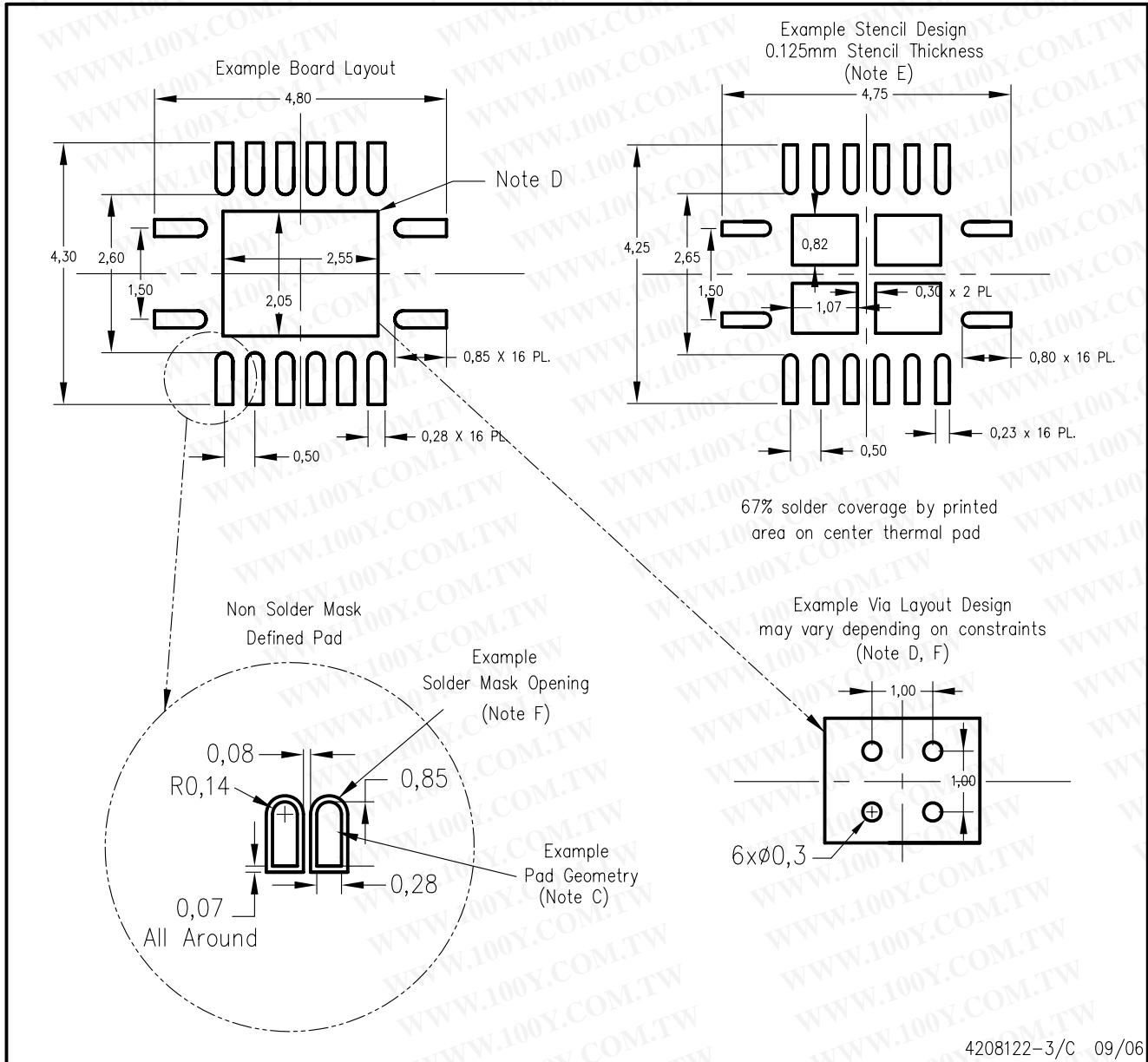
Bottom View

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R-PQFP-N16)



4208122-3/C 09/06

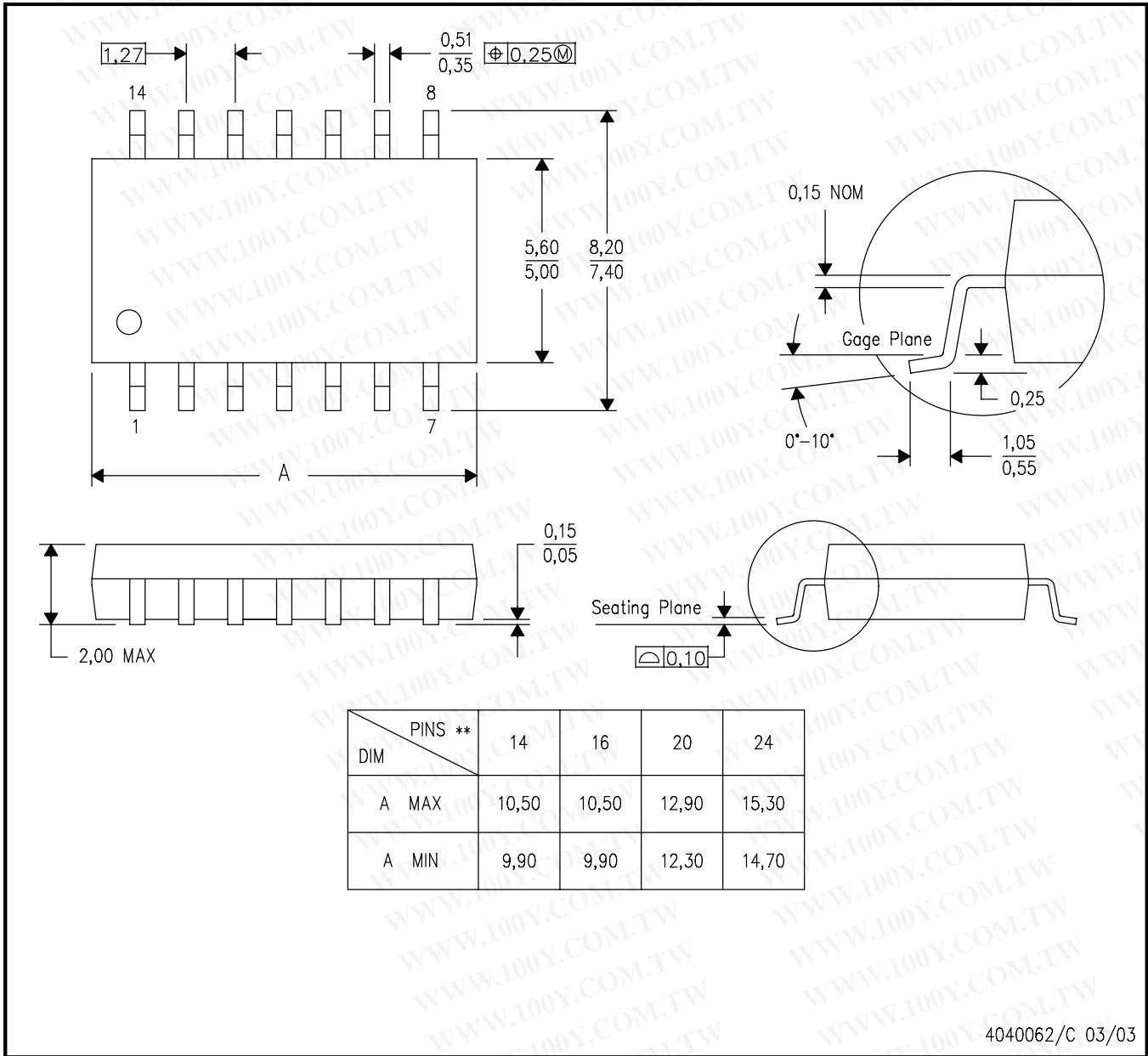
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



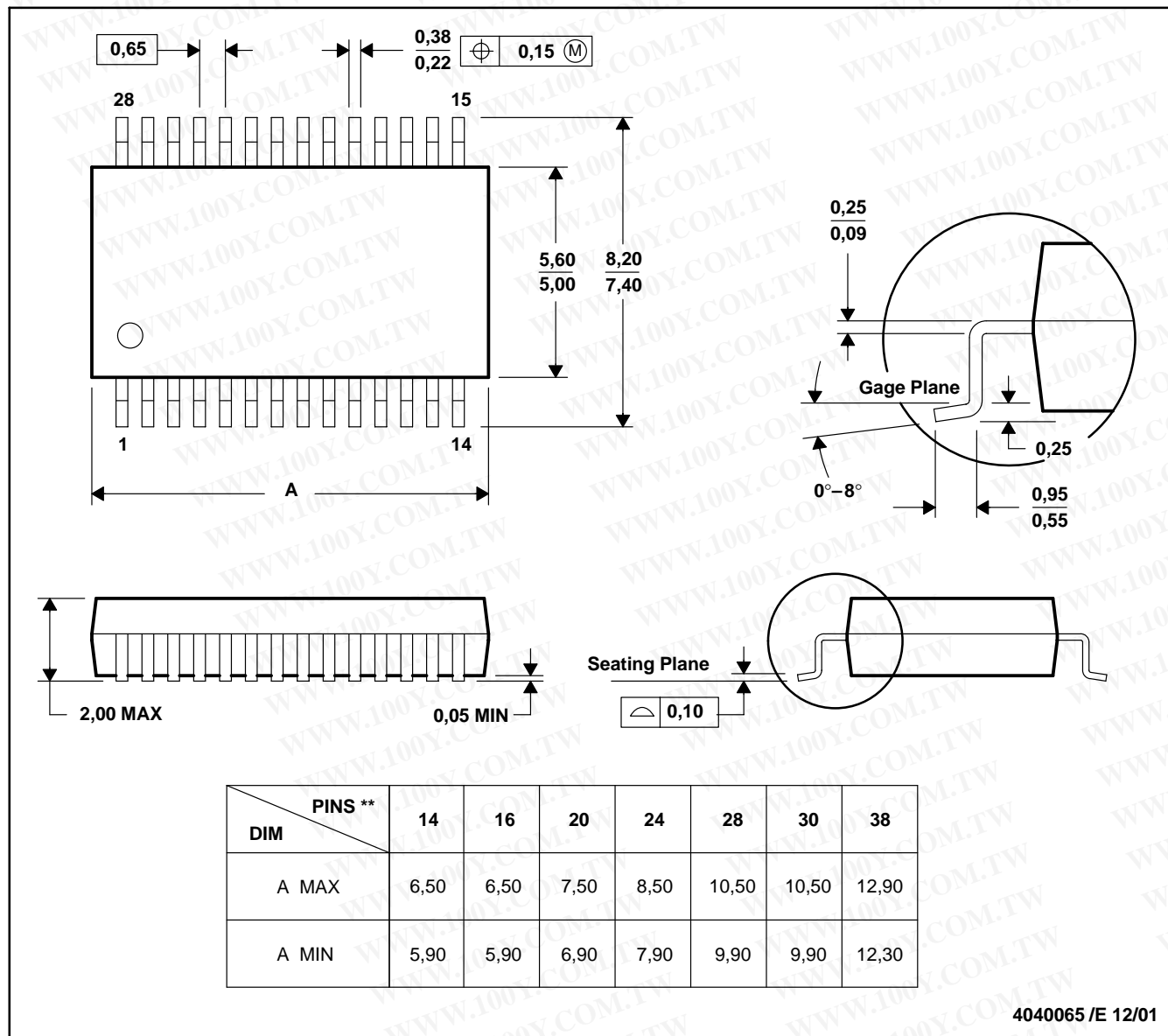
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



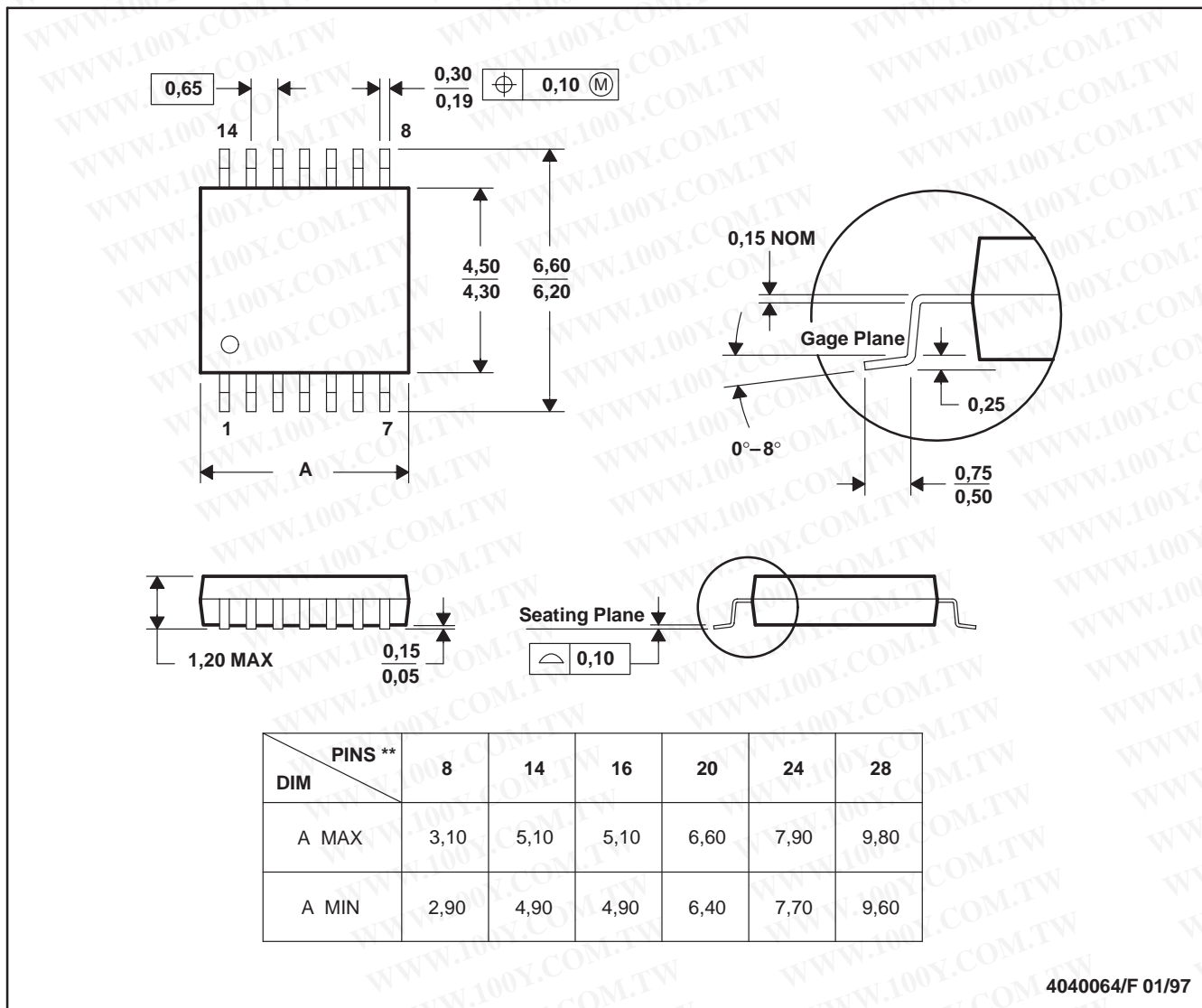
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265