

SN54LV4052A, SN74LV4052A DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS429H – MAY 1999 – REVISED APRIL 2005

- 2-V to 5.5-V V_{CC} Operation
- Support Mixed-Mode Voltage Operation on All Ports
- Fast Switching
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Extremely Low Input Current
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

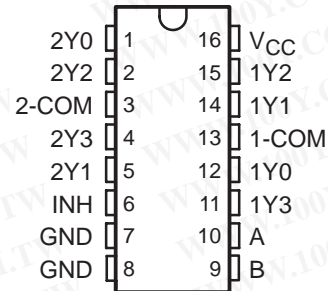
description/ordering information

These dual 4-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

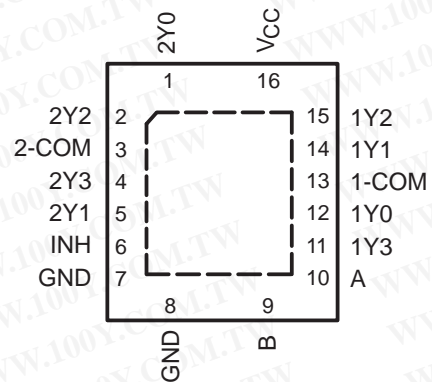
The 'LV4052A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

SN54LV4052A . . . J OR W PACKAGE
SN74LV4052A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV4052A . . . RGY PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74LV4052AN	SN74LV4052AN
	QFN – RGY	Reel of 1000	SN74LV4052ARGYR	LW052A
	SOIC – D	Tube of 40	SN74LV4052AD	LV4052A
		Reel of 2500	SN74LV4052ADR	
	SOP – NS	Reel of 2000	SN74LV4052ANSR	74LV4052A
	SSOP – DB	Reel of 2000	SN74LV4052ADBDR	LW052A
	TSSOP – PW	Tube of 90	SN74LV4052APW	LW052A
		Reel of 2000	SN74LV4052APWR	
Reel of 250		SN74LV4052APWT		
TVSOP – DGV	Reel of 2000	SN74LV4052ADGVR	LW052A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV4052AJ	SNJ54LV4052AJ
	CFP – W	Tube of 150	SNJ54LV4052AW	SNJ54LV4052AW

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated

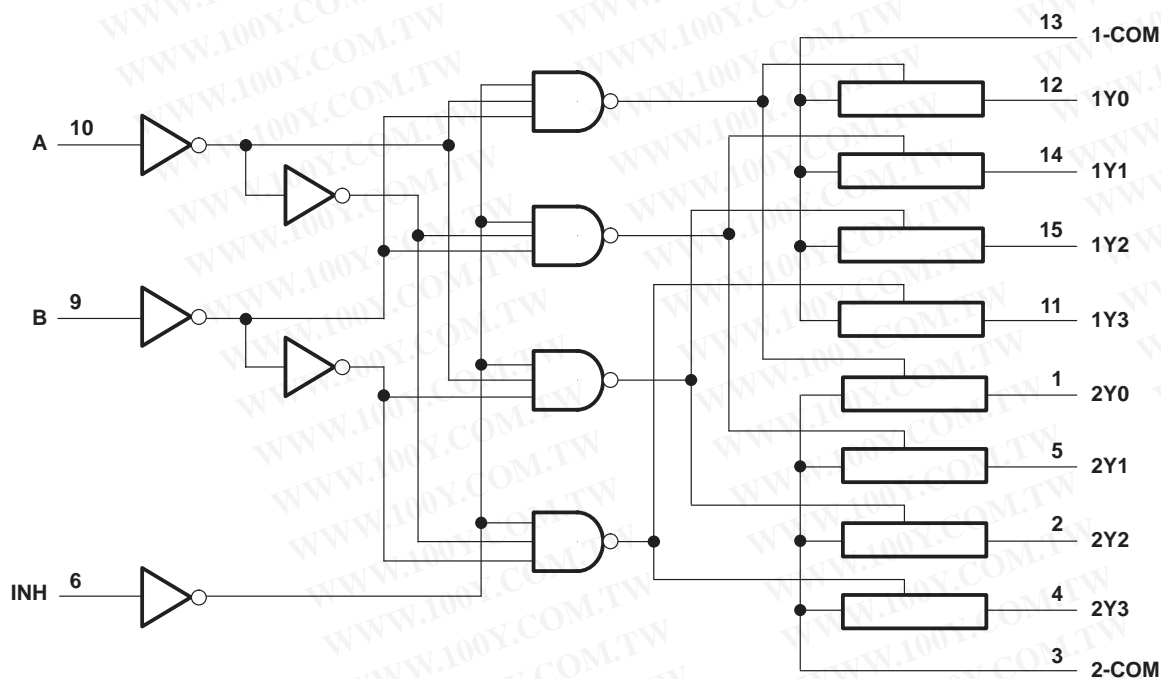
SN54LV4052A, SN74LV4052A DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS429H – MAY 1999 – REVISED APRIL 2005

FUNCTION TABLE

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

logic diagram (positive logic)



勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7.0 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7.0 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$)	–50 mA
Switch through current, I_T ($V_{IO} = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): DGV package	120°C/W
(see Note 3): N package	67°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

		SN54LV4052A		SN74LV4052A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2‡	5.5	2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	$V_{CC} = 2$ V	0.5	0.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
V_I	Control input voltage	0	5.5	0	5.5	V
V_{IO}	Input/output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	200	200		ns/V
		$V_{CC} = 3$ V to 3.6 V	100	100		
		$V_{CC} = 4.5$ V to 5.5 V	20	20		
T_A	Operating free-air temperature	–55	125	–40	85	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV4052A, SN74LV4052A DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS429H – MAY 1999 – REVISED APRIL 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54LV4052A		SN74LV4052A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r _{on} On-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 1)	2.3 V		43	180		225		225	Ω
		3 V		34	150		190		190	
		4.5 V		25	75		100		100	
r _{on(p)} Peak on-state resistance	I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V		133	500		600		600	Ω
		3 V		63	180		225		225	
		4.5 V		35	100		125		125	
Δr _{on} Difference in on-state resistance between switches	I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V		1.5	30		40		40	Ω
		3 V		1.1	20		30		30	
		4.5 V		0.7	15		20		20	
I _I Control input current	V _I = 5.5 V or GND	0 to 5.5 V			±0.1		±1		±1	μA
I _{S(off)} Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} . V _{INH} = V _{IH} (see Figure 2)	5.5 V			±0.1		±1		±1	μA
I _{S(on)} On-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 3)	5.5 V			±0.1		±1		±1	μA
I _{CC} Supply current	V _I = V _{CC} or GND	5.5 V					20		20	μA
C _{IC} Control input capacitance	f = 10 MHz	3.3 V		2.1						pF
C _{IS} Common terminal capacitance		3.3 V		13.1						pF
C _{OS} Switch terminal capacitance		3.3 V		5.6						pF
C _F Feedthrough capacitance		3.3 V		0.5						pF

勝 特 力 材 料 886-3-5753170
勝 特 力 电 子 (上 海) 86-21-54151736
勝 特 力 电 子 (深 圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV4052A, SN74LV4052A DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS429H – MAY 1999 – REVISED APRIL 2005

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4052A		SN74LV4052A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y	Y or COM	C _L = 15 pF, (see Figure 4)	1.9	10	16	16	16	16	ns
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y	C _L = 15 pF, (see Figure 5)	8	18	23	23	23	23	ns
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y	C _L = 15 pF, (see Figure 5)	8.3	18	23	23	23	23	ns
t _{PLH} t _{PHL}	Propagation delay time	COM or Y	Y or COM	C _L = 50 pF, (see Figure 4)	3.8	12	18	18	18	18	ns
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y	C _L = 50 pF, (see Figure 5)	9.4	28	35	35	35	35	ns
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y	C _L = 50 pF, (see Figure 5)	12.4	28	35	35	35	35	ns

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4052A		SN74LV4052A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y	Y or COM	C _L = 15 pF, (see Figure 4)	1.2	6	10	10	10	10	ns
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y	C _L = 15 pF, (see Figure 5)	5.7	12	15	15	15	15	ns
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y	C _L = 15 pF, (see Figure 5)	6.6	12	15	15	15	15	ns
t _{PLH} t _{PHL}	Propagation delay time	COM or Y	Y or COM	C _L = 50 pF, (see Figure 4)	2.5	9	12	12	12	12	ns
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y	C _L = 50 pF, (see Figure 5)	6.7	20	25	25	25	25	ns
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y	C _L = 50 pF, (see Figure 5)	9.5	20	25	25	25	25	ns

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV4052A, SN74LV4052A DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULPLEXERS

SCLS429H – MAY 1999 – REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4052A		SN74LV4052A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL} Propagation delay time	COM or Y	Y or COM	C _L = 15 pF, (see Figure 4)		0.7	4		7		7	ns
t _{PZH} t _{PZL} Enable delay time	INH	COM or Y	C _L = 15 pF, (see Figure 5)		4	8		10		10	ns
t _{PHZ} t _{PLZ} Disable delay time	INH	COM or Y	C _L = 15 pF, (see Figure 5)		5	8		10		10	ns
t _{PLH} t _{PHL} Propagation delay time	COM or Y	Y or COM	C _L = 50 pF, (see Figure 4)		1.5	6		8		8	ns
t _{PZH} t _{PZL} Enable delay time	INH	COM or Y	C _L = 50 pF, (see Figure 5)		4.7	14		18		18	ns
t _{PHZ} t _{PLZ} Disable delay time	INH	COM or Y	C _L = 50 pF, (see Figure 5)		6.9	14		18		18	ns

analog switch characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	T _A = 25°C			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	COM or Y	Y or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 6 and Figure 6)	2.3 V		30	MHz	
				3 V		35		
				4.5 V		50		
Crosstalk (between any switches)	COM or Y	Y or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 7 and Figure 7)	2.3 V		-45	dB	
				3 V		-45		
				4.5 V		-45		
Crosstalk (control input to signal output)	INH	COM or Y	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave) (see Figure 8)	2.3 V		20	mV	
				3 V		35		
				4.5 V		65		
Feedthrough attenuation (switch off)	COM or Y	Y or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 7 and Figure 9)	2.3 V		-45	dB	
				3 V		-45		
				4.5 V		-45		
Sine-wave distortion	COM or Y	Y or COM	C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave) (see Figure 10)	V _I = 2 V _{p-p}	2.3 V	0.1	%	
				V _I = 2.5 V _{p-p}	3 V	0.1		
				V _I = 4 V _{p-p}	4.5 V	0.1		

NOTES: 6. Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.
7. Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	11.8	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

PARAMETER MEASUREMENT INFORMATION

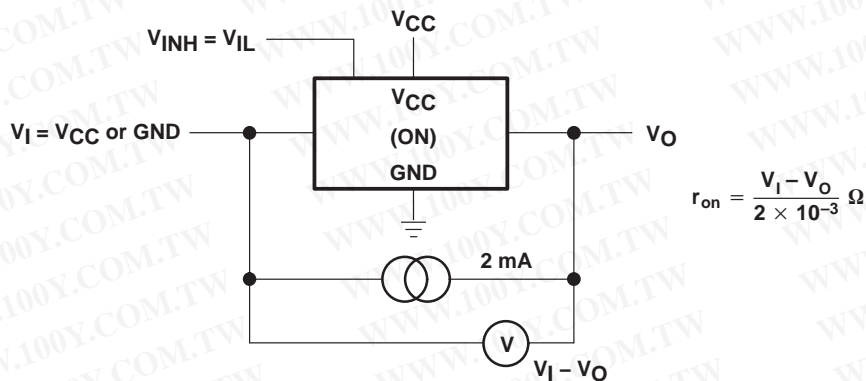
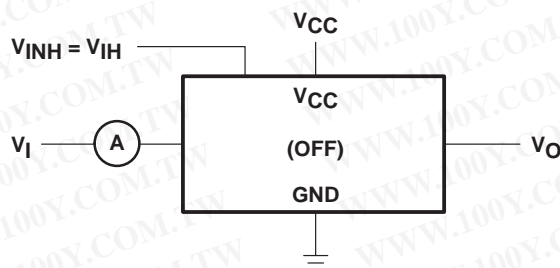


Figure 1. On-State Resistance Test Circuit



Condition 1: $V_I = 0, V_O = V_{CC}$
 Condition 2: $V_I = V_{CC}, V_O = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit

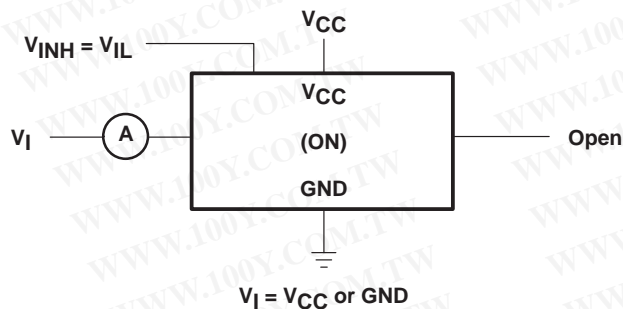


Figure 3. On-State Switch Leakage-Current Test Circuit

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

SN54LV4052A, SN74LV4052A DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS429H – MAY 1999 – REVISED APRIL 2005

PARAMETER MEASUREMENT INFORMATION

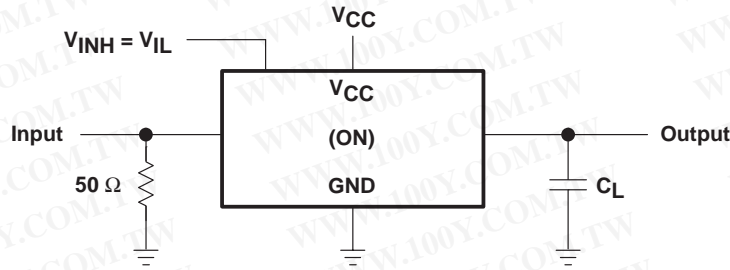
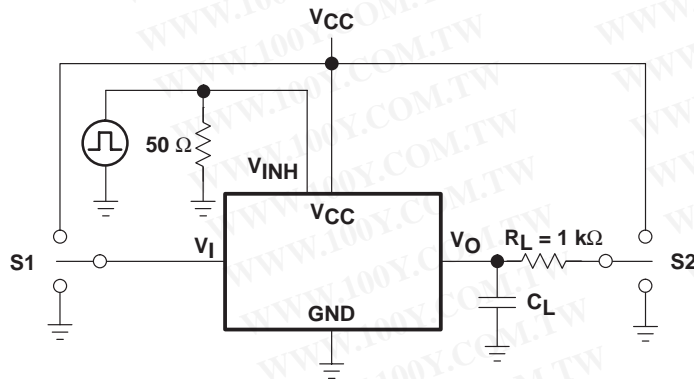


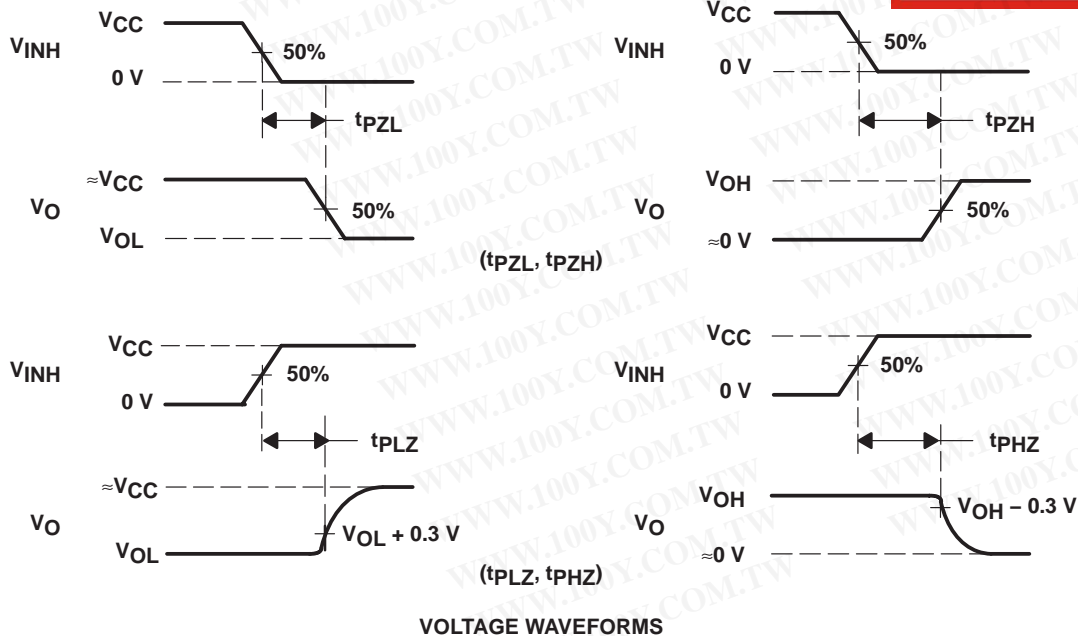
Figure 4. Propagation Delay Time, Signal Input to Signal Output



TEST CIRCUIT

TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

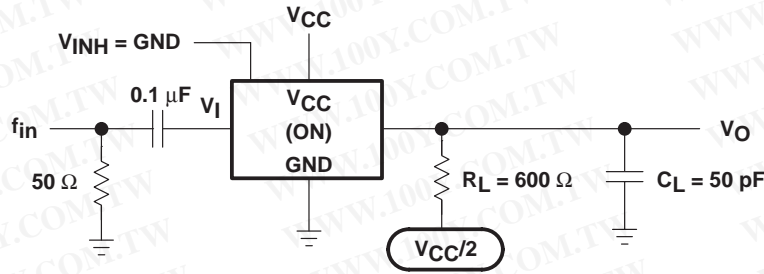
勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL} , t_{PLZ} , t_{PHZ} , t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION



NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

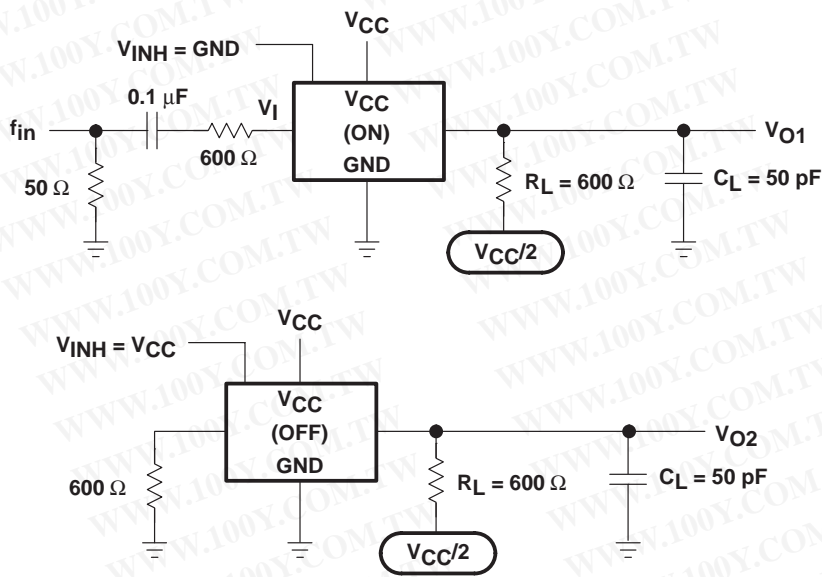


Figure 7. Crosstalk Between Any Two Switches

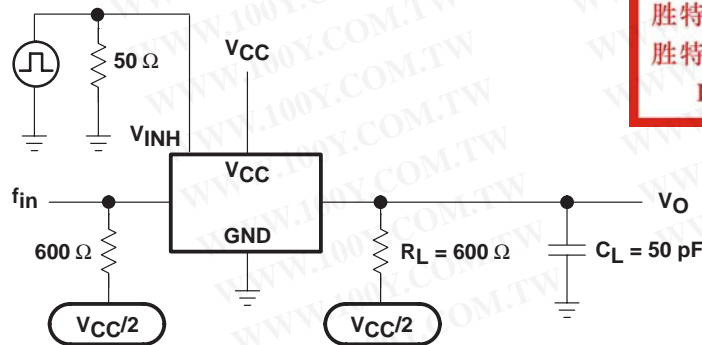


Figure 8. Crosstalk Between Control Input and Switch Output

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

SN54LV4052A, SN74LV4052A DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS429H – MAY 1999 – REVISED APRIL 2005

PARAMETER MEASUREMENT INFORMATION

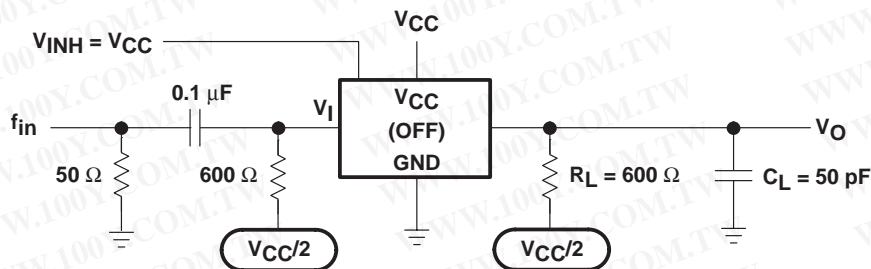


Figure 9. Feedthrough Attenuation (Switch Off)

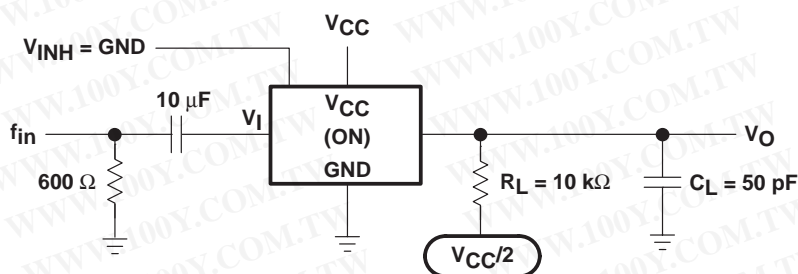


Figure 10. Sine-Wave Distortion

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV4052AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV4052ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV4052ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4052ARGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LV4052ARGYRG4	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

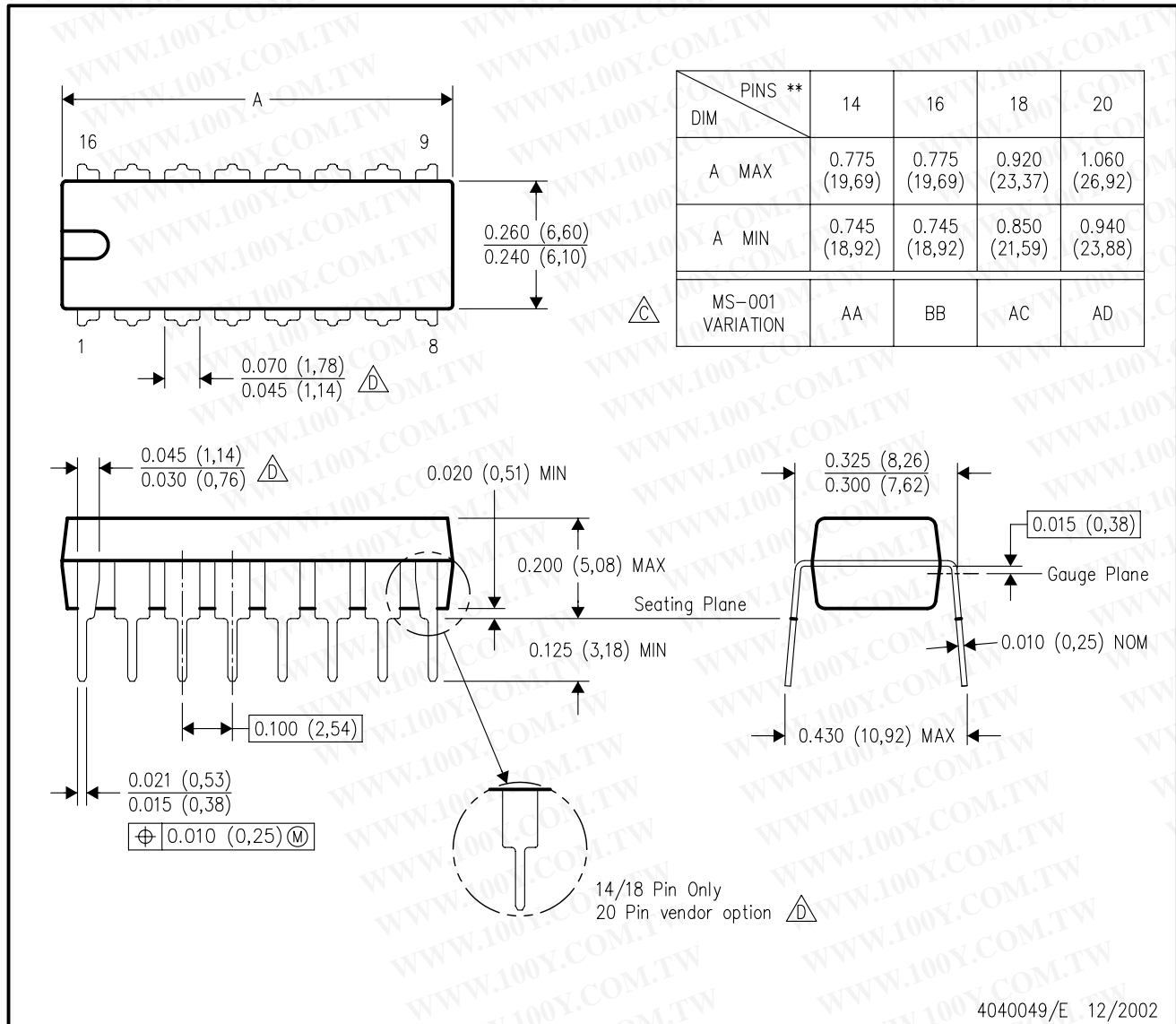
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



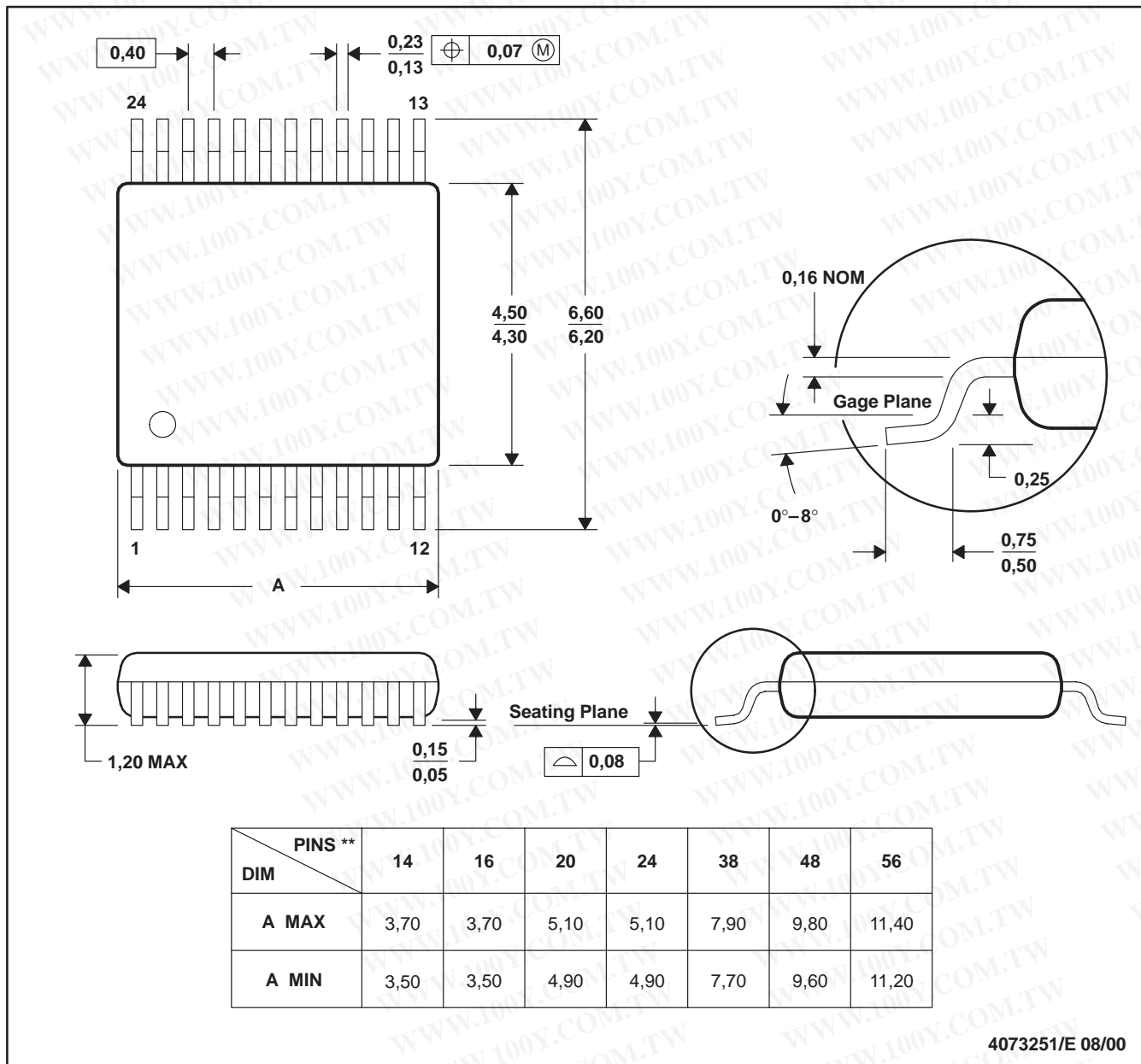
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



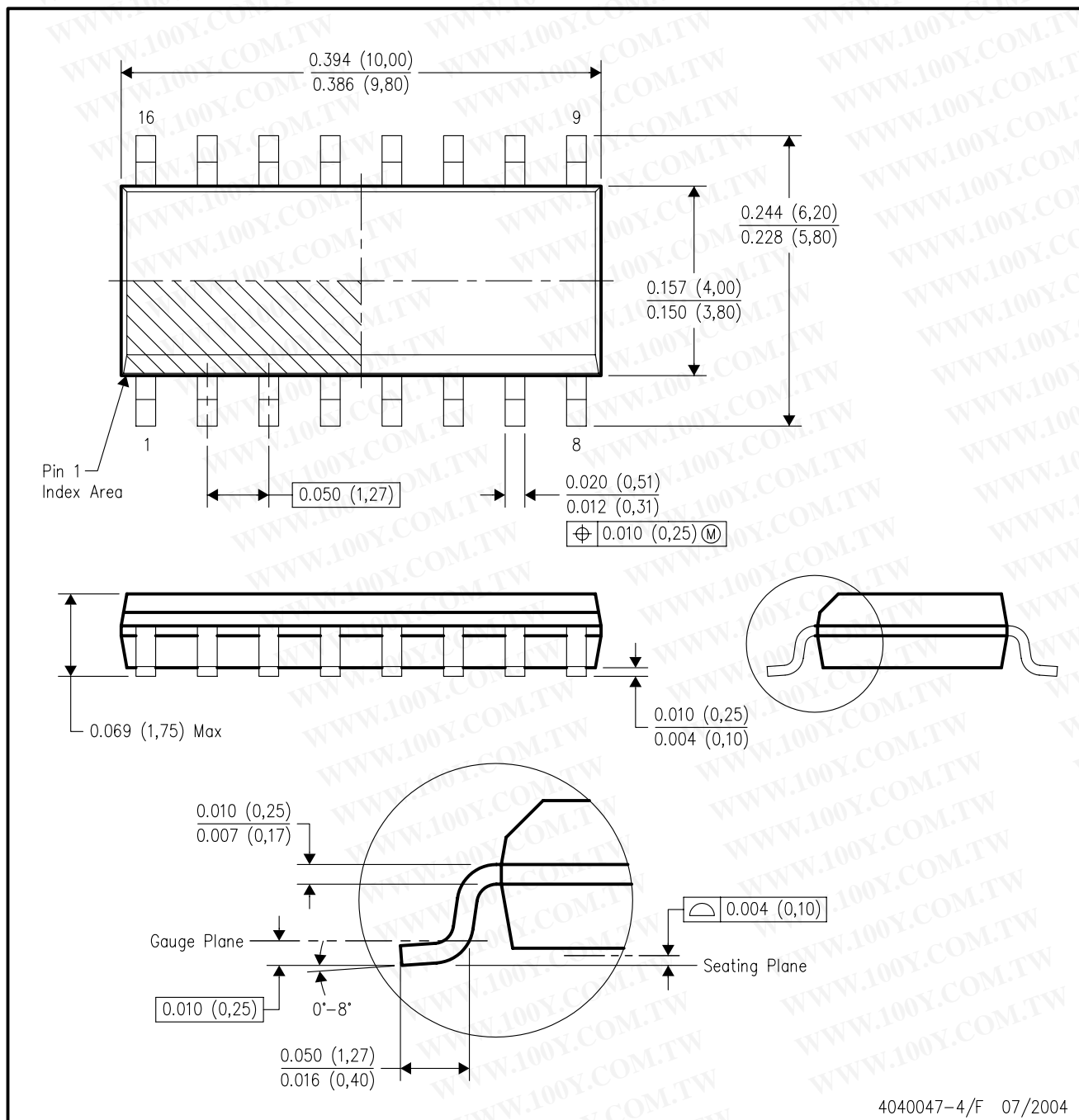
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



D (R-PDSO-G16)

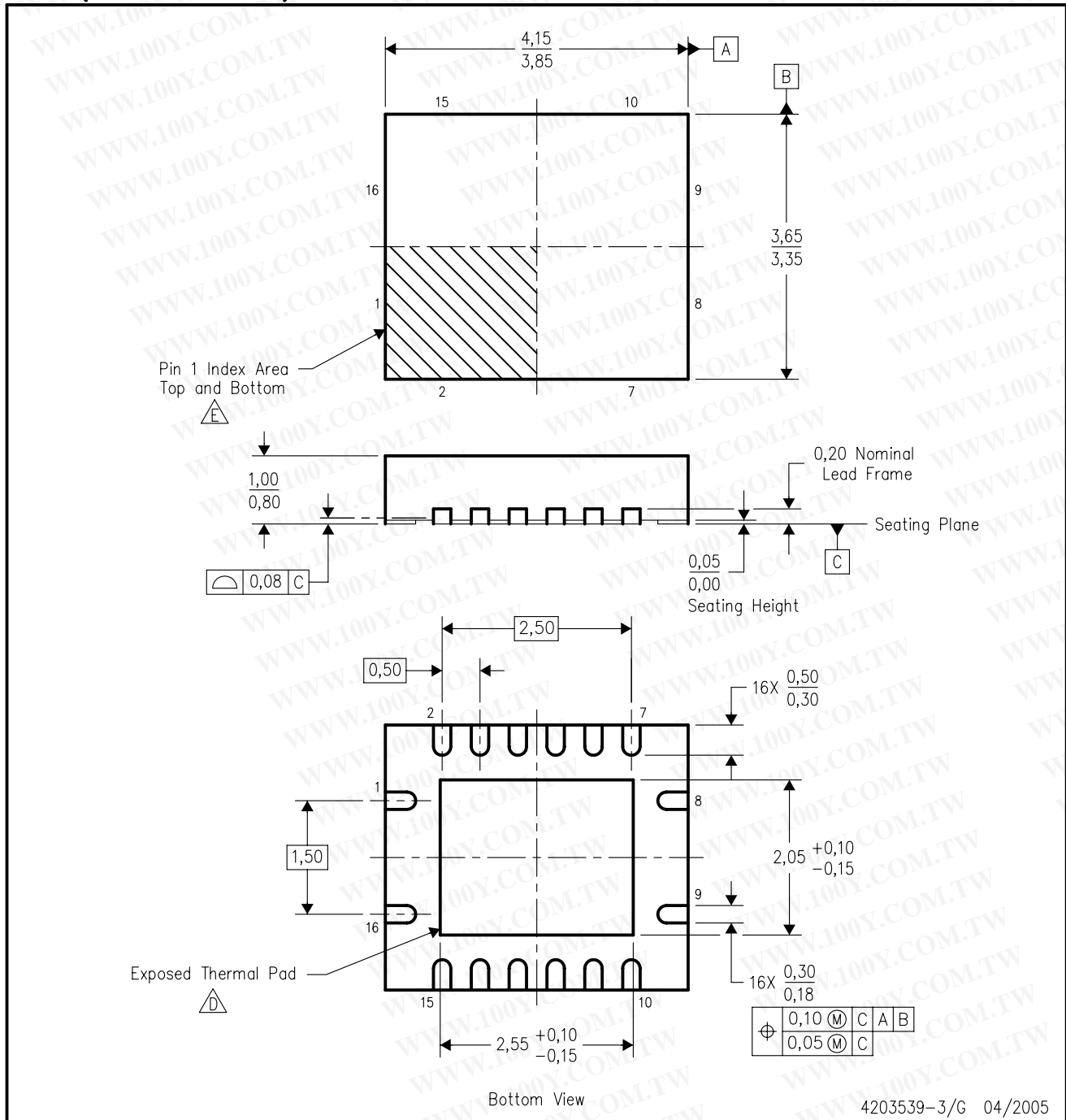
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK



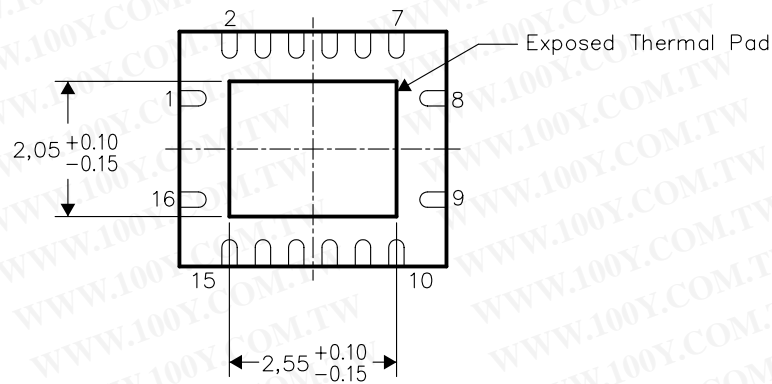
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BB.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

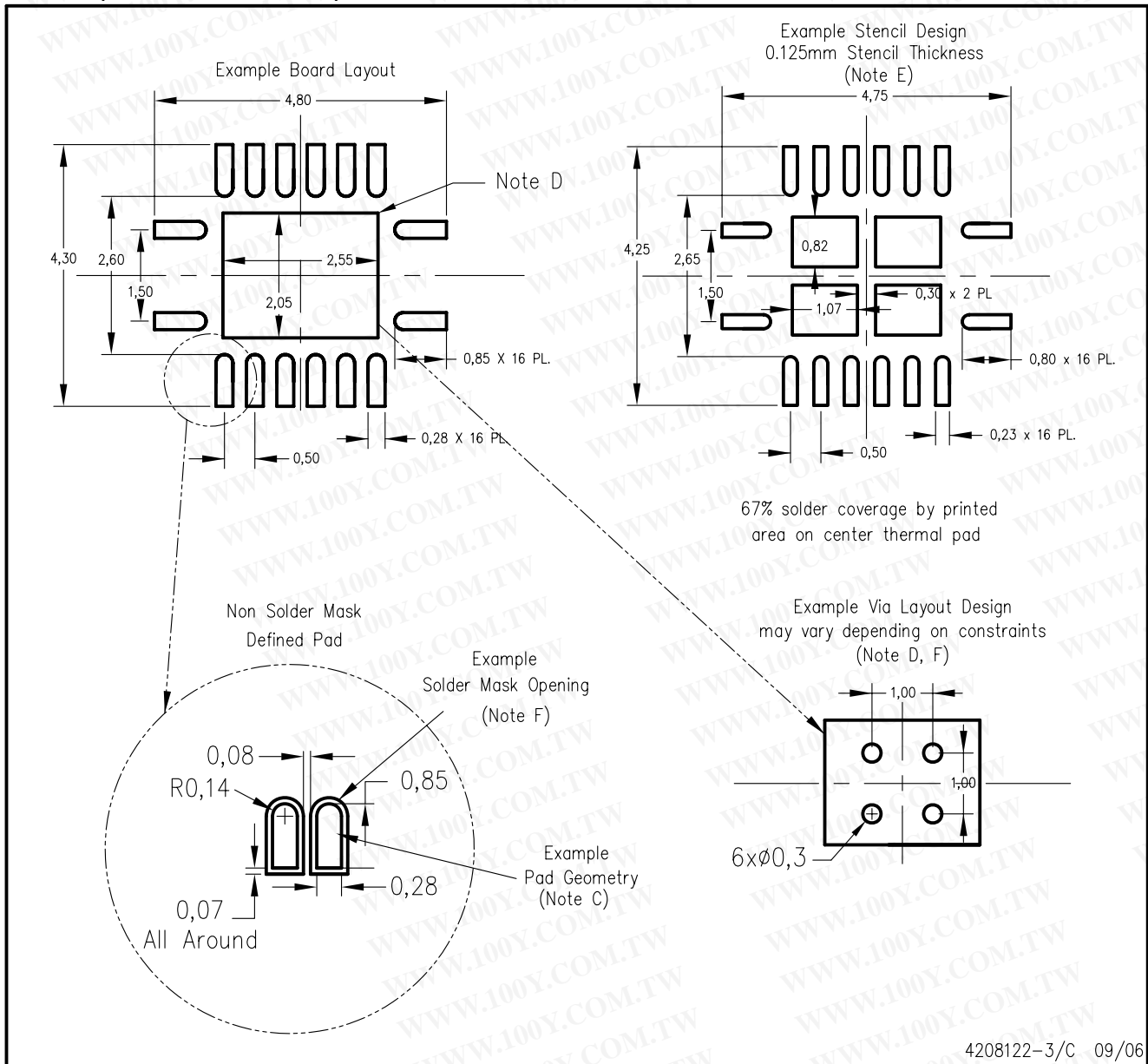


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R-PQFP-N16)



4208122-3/C 09/06

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

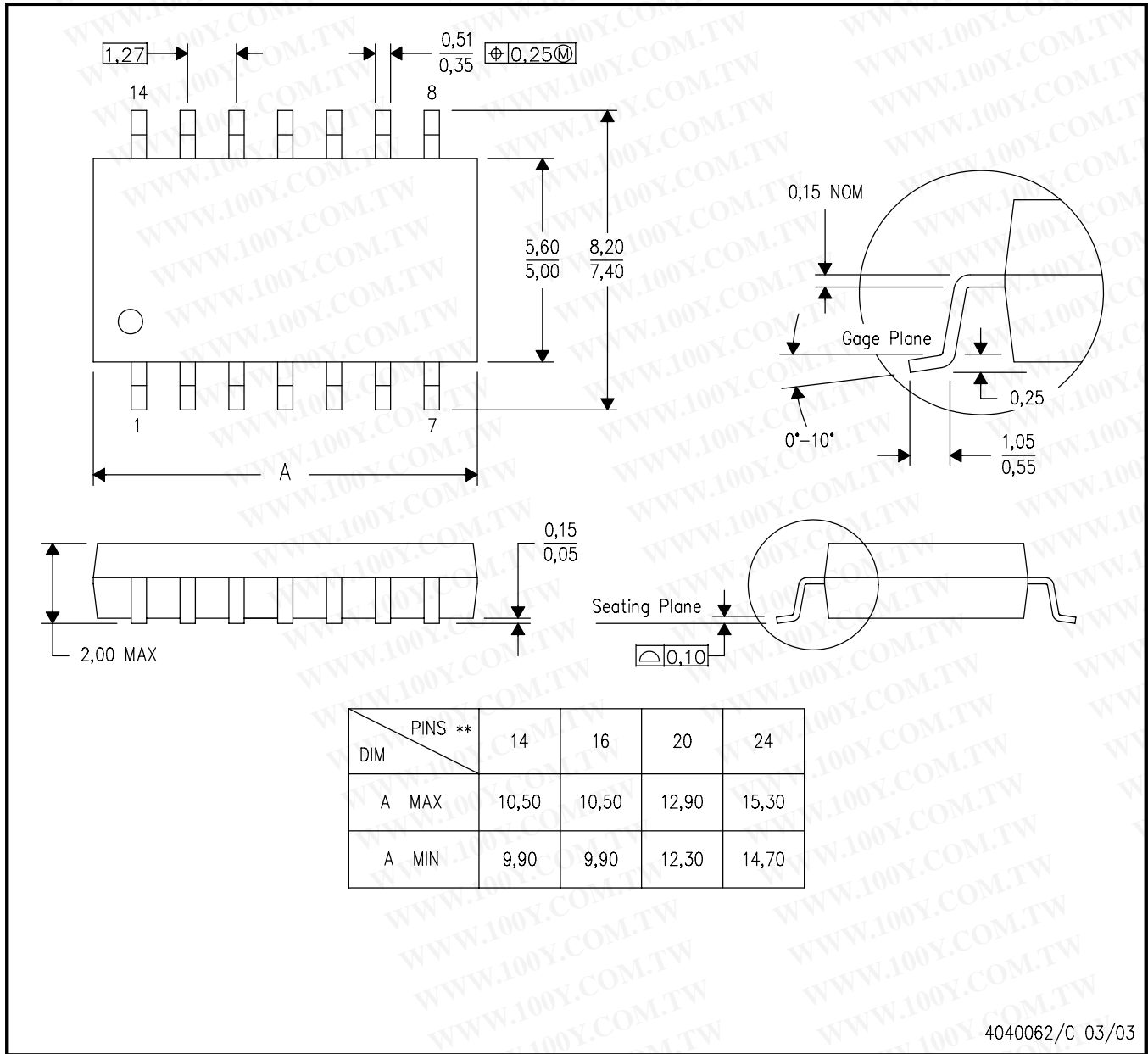
勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

NS (R-PDSO-G**)

14-PINS SHOWN

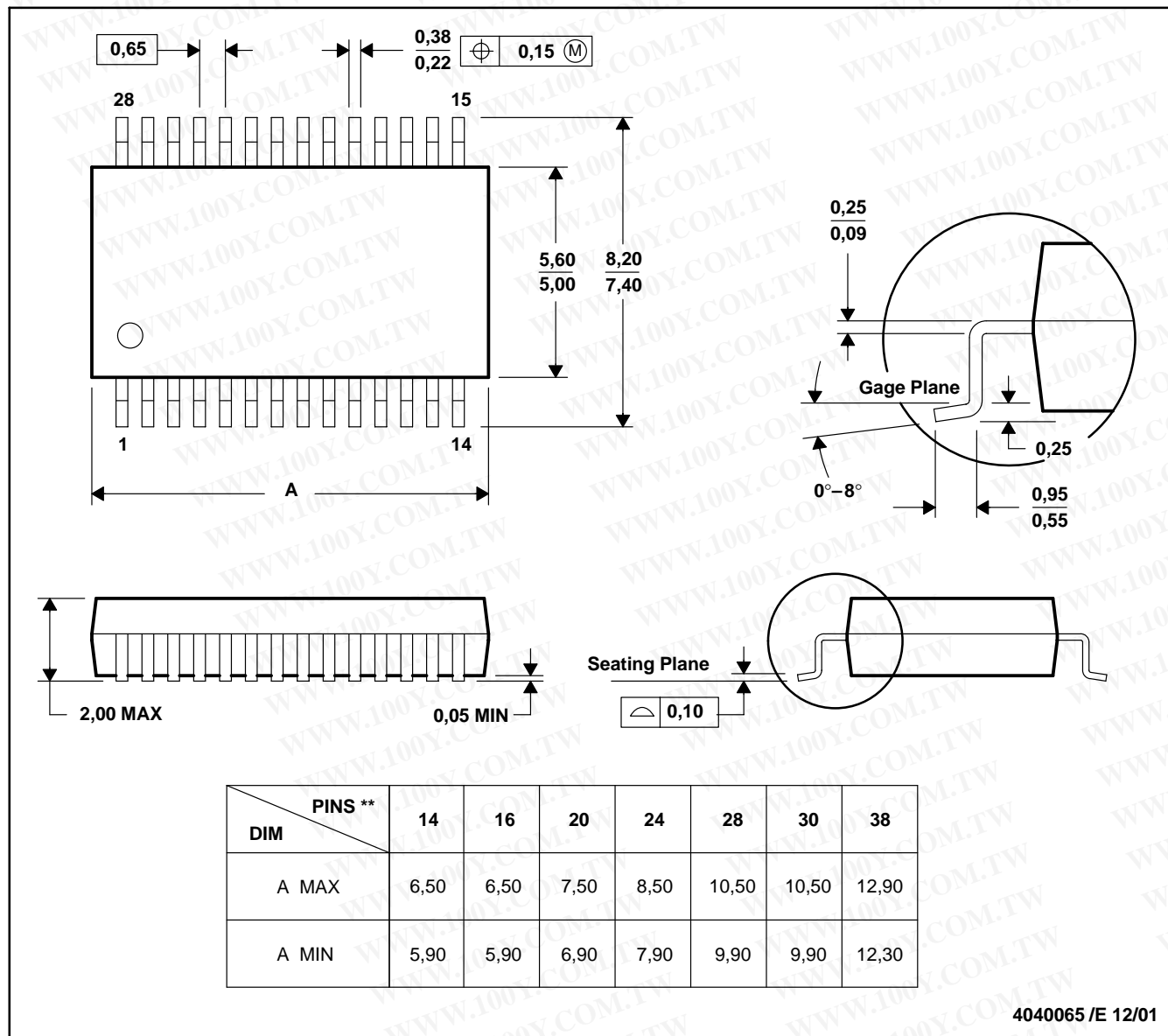


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



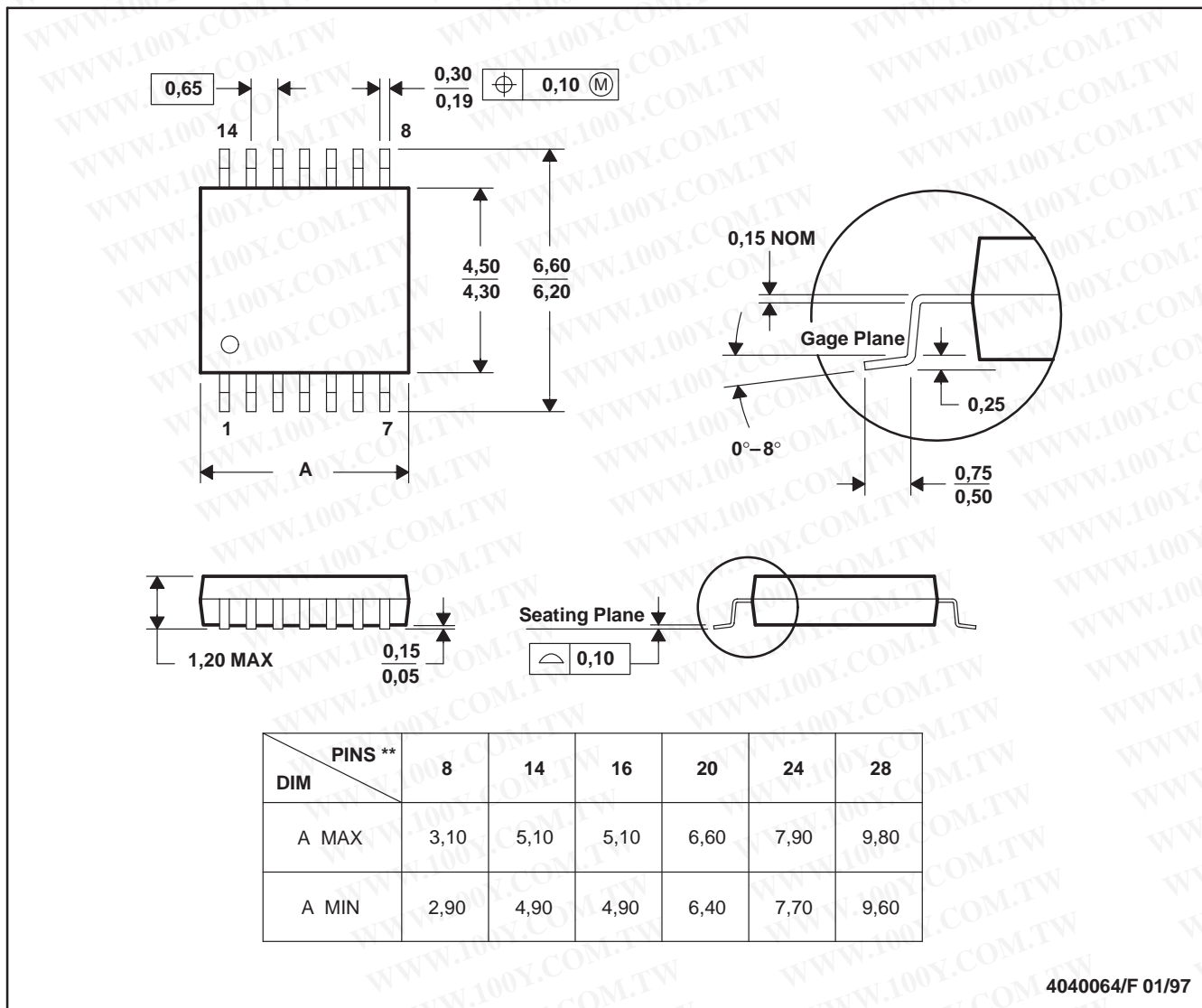
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265