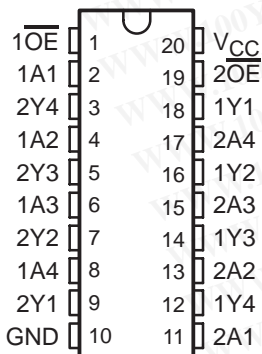# SN54LV244A, SN74LV244A
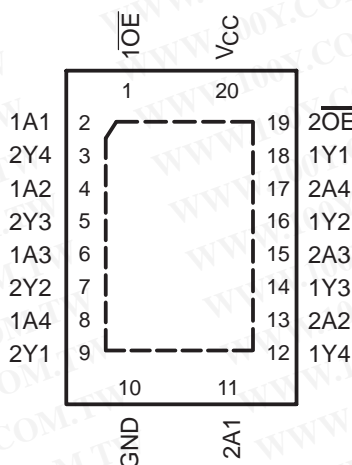# OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCLS383L – SEPTEMBER 1997 – REVISED APRIL 2005

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports

- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  – 2000-V Human-Body Model (A114-A)
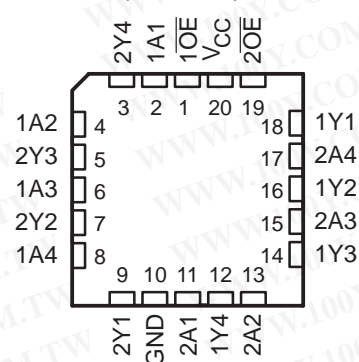 – 200-V Machine Model (A115-A)
  – 1000-V Charged-Device Model (C101)

SN54LV244A . . . J OR W PACKAGE
SN74LV244A . . . DB, DGV, DW, NS
OR PW PACKAGE
(TOP VIEW)

1OE	1	20	V_{CC}
1A1	2	19	2OE
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1

SN74LV244A . . . RGY PACKAGE
(TOP VIEW)

Pins (top): 1OE (1), V_{CC} (20)

1A1	2	19	2OE
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4

Pins (bottom): GND (10), 2A1 (11)

SN54LV244A . . . FK PACKAGE
(TOP VIEW)

Pins (top): 2Y4 (4), 1A1 (3), 1OE (2), V_{CC} (1), 2OE (20)

1A2	4	18	1Y1
2Y3	5	17	2A4
1A3	6	16	1Y2
2Y2	7	15	2A3
1A4	8	14	1Y3

Pins (bottom): 2Y1 (9), GND (10), 2A1 (11), 1Y4 (12), 2A2 (13)

description/ordering information

These octal buffers/line drivers are designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV244ARGYR	LV244A
	SOIC – DW	Tube of 25	SN74LV244ADW	LV244A
		Reel of 2000	SN74LV244ADWR	
	SOP – NS	Reel of 2000	SN74LV244ANSR	74LV244A
	SSOP – DB	Reel of 2000	SN74LV244ADBR	LV244A
	TSSOP – PW	Tube of 70	SN74LV244APW	LV244A
		Reel of 2000	SN74LV244APWR	
		Reel of 250	SN74LV244APWT	
	TVSOP – DGV	Reel of 2000	SN74LV244ADGVR	LV244A
−55°C to 125°C	CDIP – J	Tube of 20	SNJ54LV244AJ	SNJ54LV244AJ
	CFP – W	Tube of 85	SNJ54LV244AW	SNJ54LV244AW
	LCCC – FK	Tube of 55	SNJ54LV244AFK	SNJ54LV244AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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1

description/ordering information (continued)

The 'LV244A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.
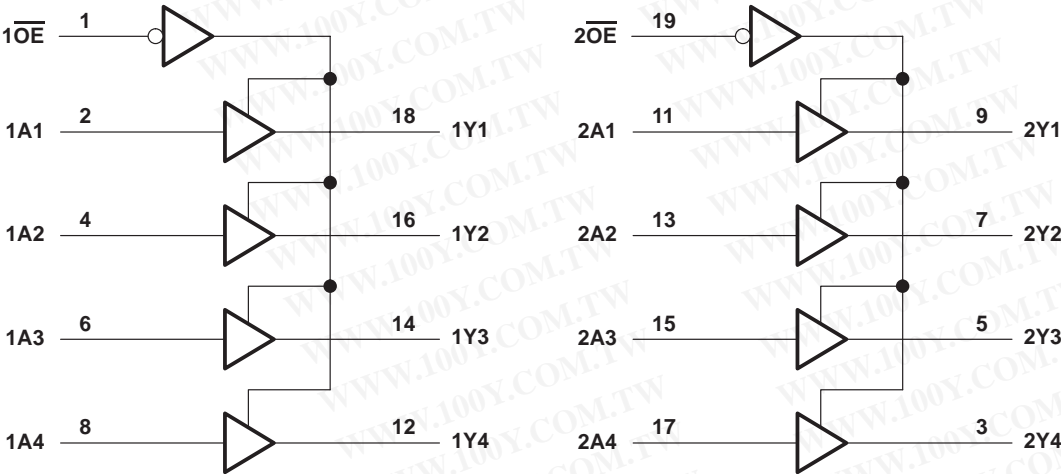
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V

Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V

Voltage range applied to any output in the high-impedance or
  power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V

Output voltage range applied in the high or low state, V_O (see Notes 1 and 2) . . . . . . –0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$) . . . . –20 mA

Output clamp current, I_{OK} ($V_O < 0$) . . . . –50 mA

Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±35 mA

Continuous current through V_{CC} or GND . . . . ±70 mA

Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . 70°C/W

(see Note 3): DGV package . . . . 92°C/W

(see Note 3): DW package . . . . 58°C/W

(see Note 3): NS package . . . . 60°C/W

(see Note 3): PW package . . . . 83°C/W

(see Note 4): RGY package . . . . 37°C/W

Storage temperature range, T_{stg} . . . . –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

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recommended operating conditions (see Note 5)

			SN54LV244A		SN74LV244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−8		−8	
		V_{CC} = 4.5 V to 5.5 V		−16		−16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54LV244A			SN74LV244A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = −50 µA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V
		I_{OH} = −2 mA	2.3 V	2			2			
		I_{OH} = −8 mA	3 V	2.48			2.48			
		I_{OH} = −16 mA	4.5 V	3.8			3.8			
V_{OL}		I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4			0.4	
		I_{OL} = 8 mA	3 V			0.44			0.44	
		I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I		V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	µA
I_{OZ}		V_O = V_{CC} or GND	5.5 V			±5			±5	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
I_{off}		V_I or V_O = 0 to 5.5 V	0			5			5	µA
C_i		V_I = V_{CC} or GND	3.3 V		2.3			2.3		pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		7.5*	12.5*	1*	15*	1	15	ns
t_{en}	$\overline{OE}$	Y			8.9*	14.6*	1*	17*	1	17	
t_{dis}	$\overline{OE}$	Y			9.1*	14.1*	1*	16*	1	16	
t_{pd}	A	Y	C_L = 50 pF		9.5	15.3	1	18	1	18	ns
t_{en}	$\overline{OE}$	Y			10.8	17.8	1	21	1	21	
t_{dis}	$\overline{OE}$	Y			13.4	19.2	1	21	1	21	
$t_{sk(o)}$						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		5.4*	8.4*	1*	10*	1	10	ns
t_{en}	$\overline{OE}$	Y			6.3*	10.6*	1*	12.5*	1	12.5	
t_{dis}	$\overline{OE}$	Y			7.6*	11.7*	1*	13*	1	13	
t_{pd}	A	Y	C_L = 50 pF		6.8	11.9	1	13.5	1	13.5	ns
t_{en}	$\overline{OE}$	Y			7.8	14.1	1	16	1	16	
t_{dis}	$\overline{OE}$	Y			11	16	1	18	1	18	
$t_{sk(o)}$						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y			3.9*	5.5*	1*	6.5*	1	6.5	
t_{en}	$\overline{OE}$	Y	C_L = 15 pF		4.5*	7.3*	1*	8.5*	1	8.5	ns
t_{dis}	$\overline{OE}$	Y			6.5*	12.2*	1*	13.5*	1	13.5	
t_{pd}	A	Y			4.9	7.5	1	8.5	1	8.5	
t_{en}	$\overline{OE}$	Y	C_L = 50 pF		5.6	9.3	1	10.5	1	10.5	ns
t_{dis}	$\overline{OE}$	Y			8.8	14.2	1	15.5	1	15.5	
$t_{sk(o)}$						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 6)

	PARAMETER	SN74LV244A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.55		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.
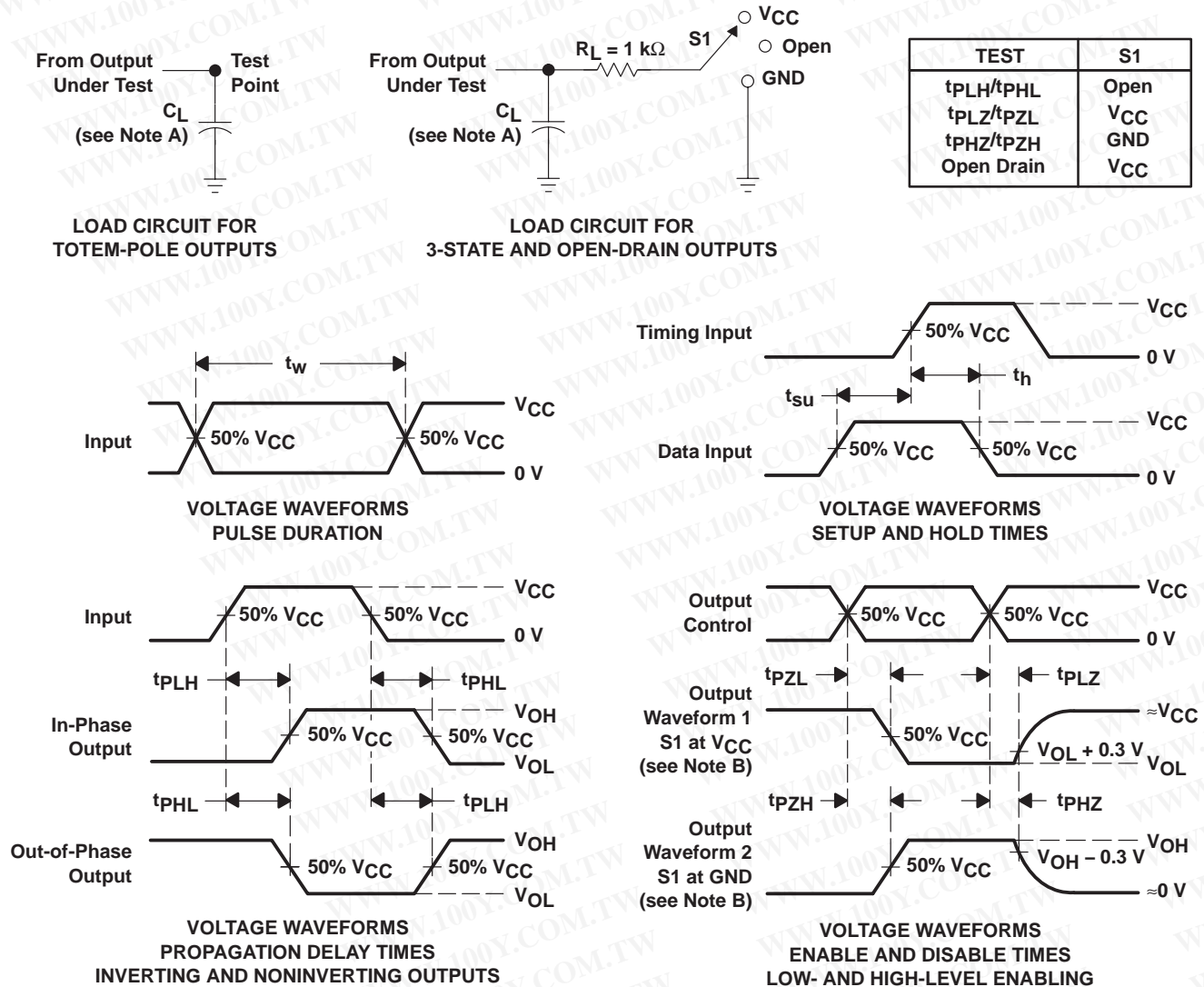
operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	14	pF
			5 V	16	

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LV244ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74LV244ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74LV244APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV244ARGYR	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LV244ARGYRG4	ACTIVE	QFN	RGY	20		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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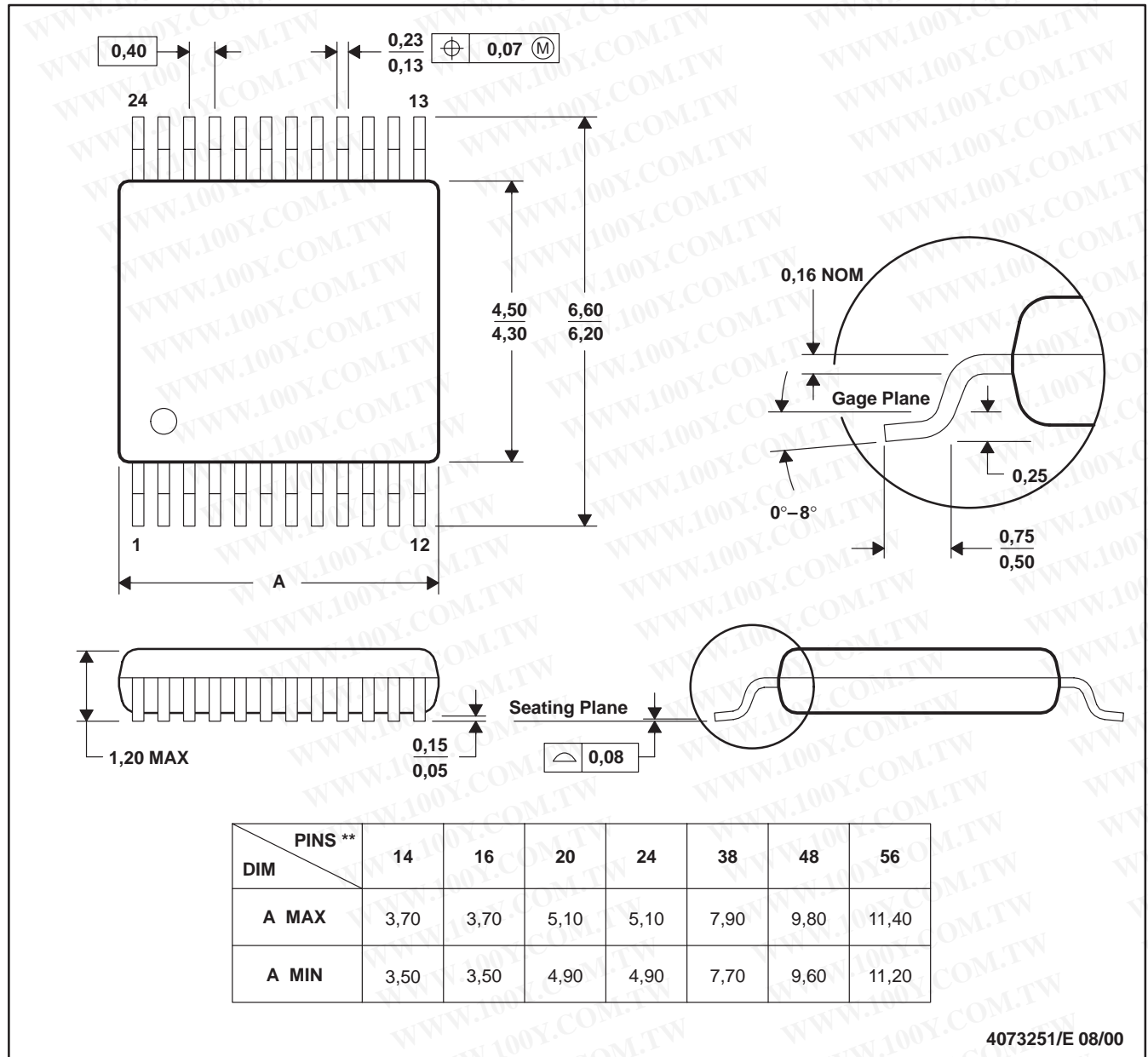
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DGV (R-PDSO-G**)   PLASTIC SMALL-OUTLINE
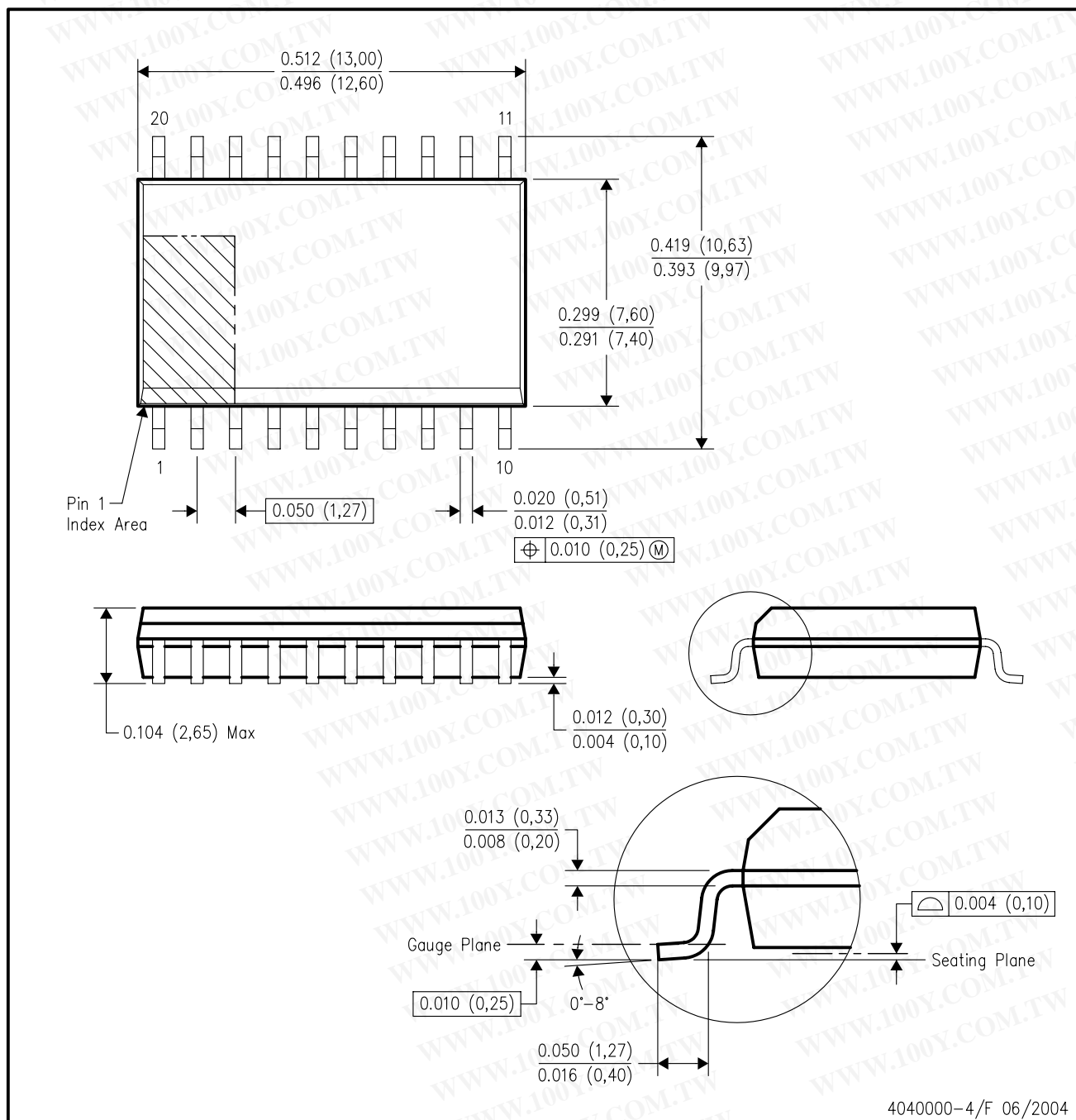
24 PINS SHOWN

0,40   0,23 / 0,13   ⊕ 0,07 Ⓜ

24   13

4,50 / 4,30   6,60 / 6,20

0,16 NOM

Gage Plane

0,25

0°−8°

0,75 / 0,50

1   12

A

1,20 MAX

0,15 / 0,05

Seating Plane

⌒ 0,08

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
    B. This drawing is subject to change without notice.
    C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
    D. Falls within JEDEC: 24/48 Pins – MO-153
                    14/16/20/56 Pins – MO-194

DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040000−4/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS−013 variation AC.

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RGY (R−PQFP−N20) PLASTIC QUAD FLATPACK
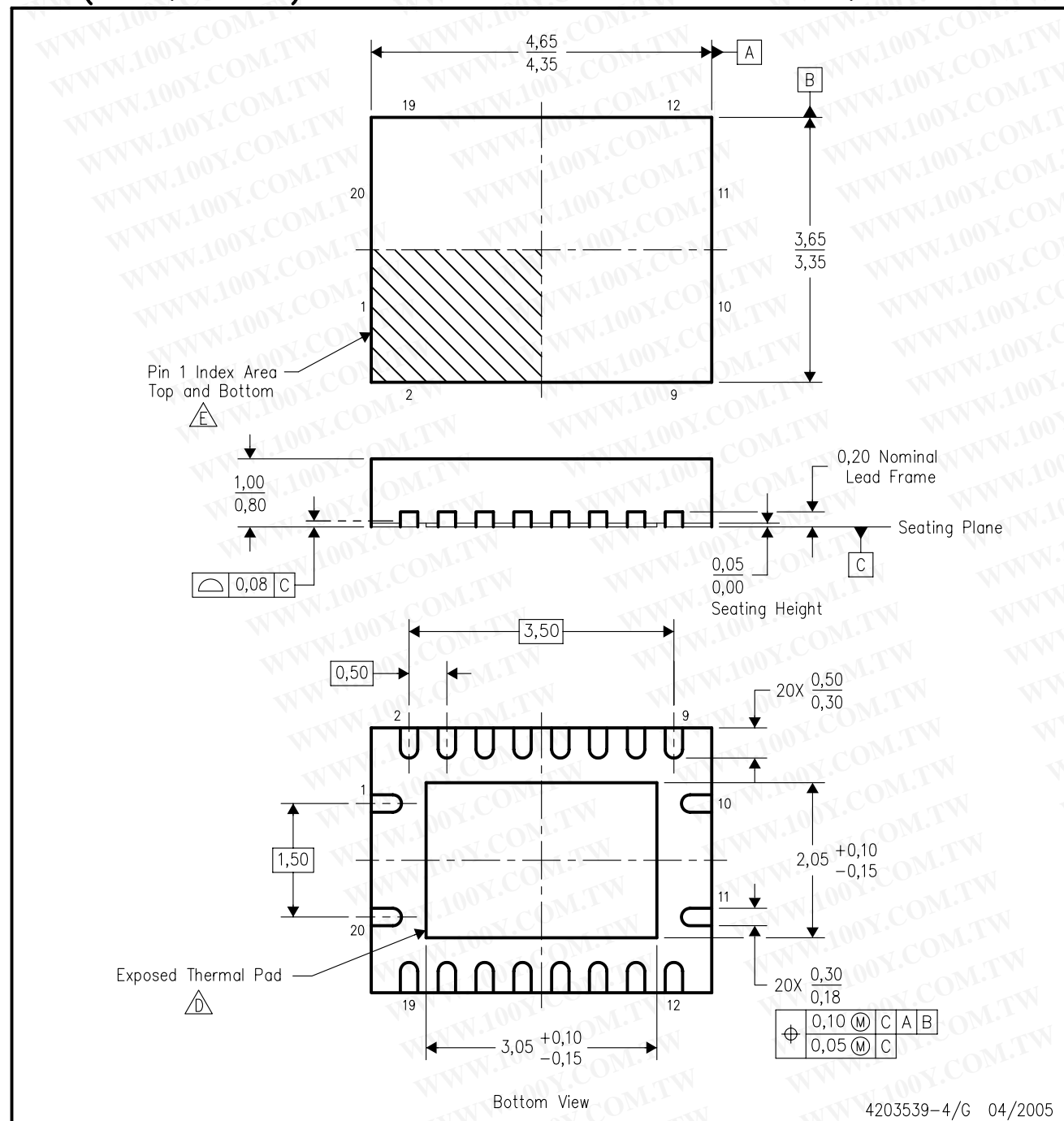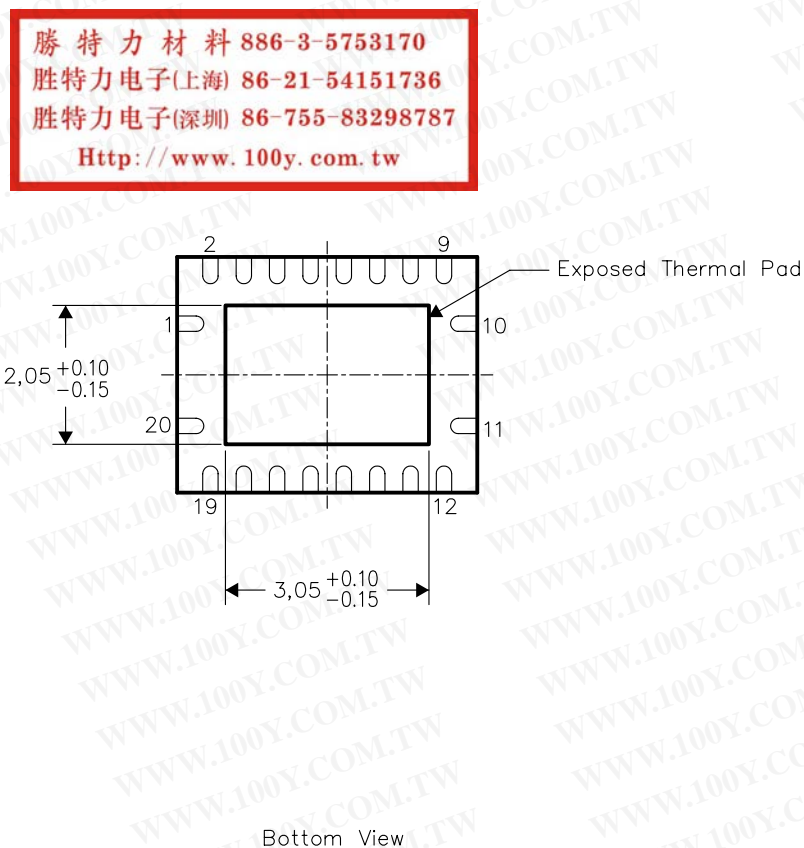

4203539-4/G 04/2005

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
   B. This drawing is subject to change without notice.
   C. QFN (Quad Flatpack No−Lead) package configuration.
   D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
   E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
     The Pin 1 identifiers are either a molded, marked, or metal feature.
   F. Package complies to JEDEC MO−241 variation BC.

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THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No−Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.
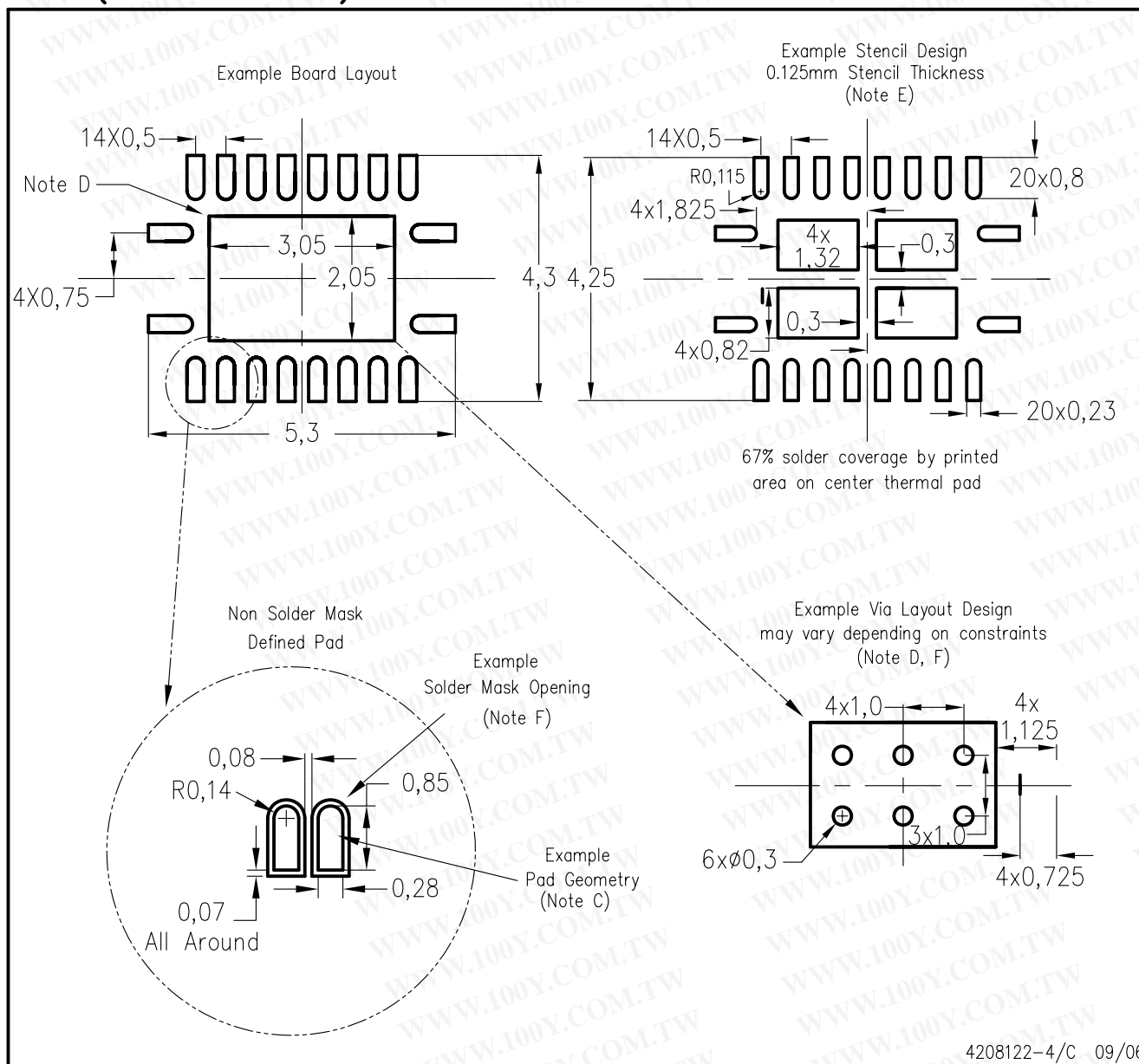
The exposed thermal pad dimensions for this package are shown in the following illustration.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R−PQFP−N20)

Example Board Layout

14X0,5

Note D

3,05

2,05

4X0,75

4,3 4,25

5,3

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

14X0,5

R0,115

4x1,825

4x
1,32

0,3

20x0,8

0,3

4x0,82

20x0,23

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

0,08

R0,14

0,85

0,07

0,28

All Around

Example
Solder Mask Opening
(Note F)

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

4x1,0

4x
1,125

6xØ0,3

3x1,0

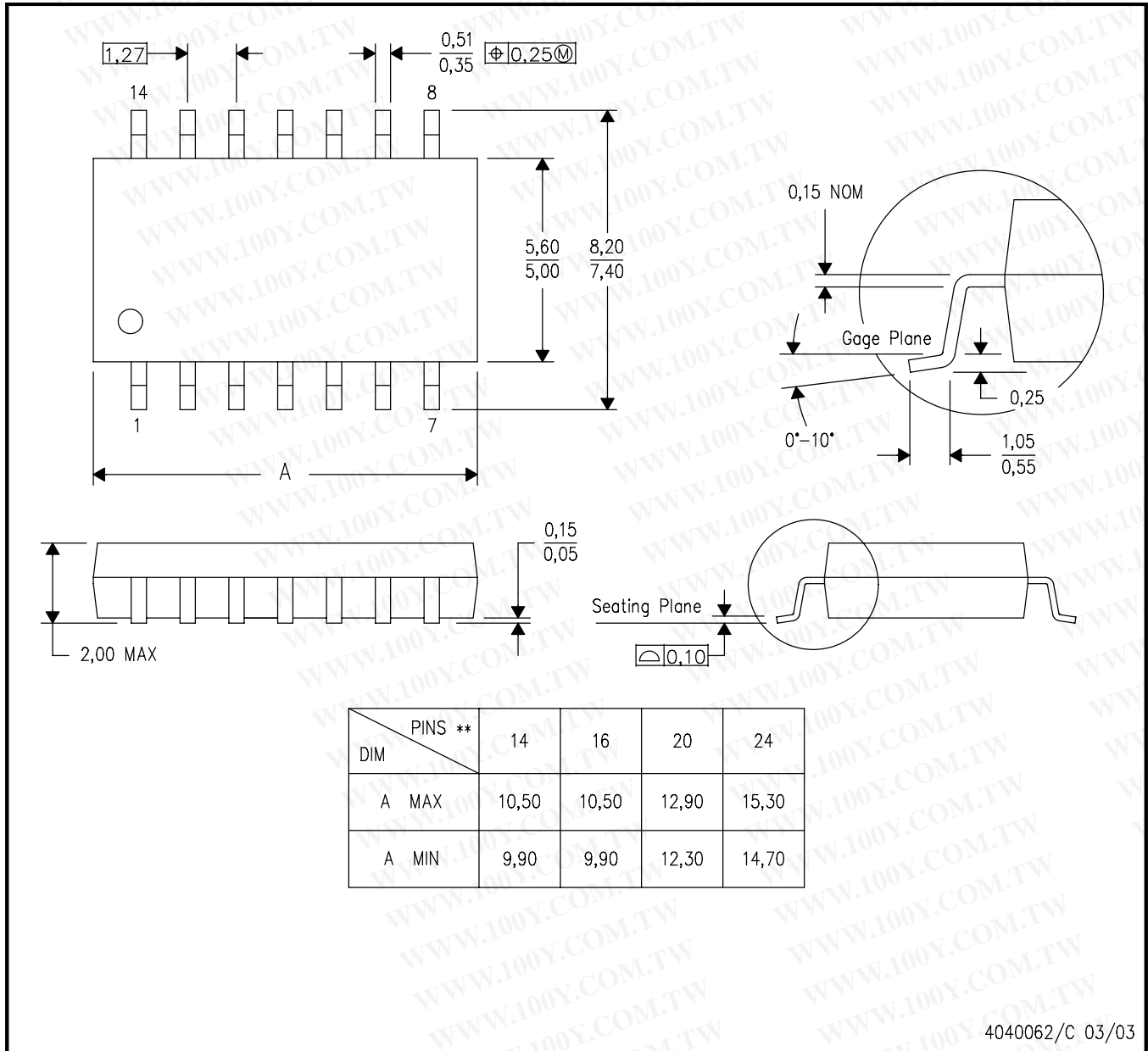4x0,725

4208122−4/C 09/06

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Publication IPC−7351 is recommended for alternate designs.
   D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
       Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets
       for specific thermal information, via requirements, and recommended board layout. These documents are available at
       www.ti.com <http: //www.ti.com>.
   E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
       contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
   F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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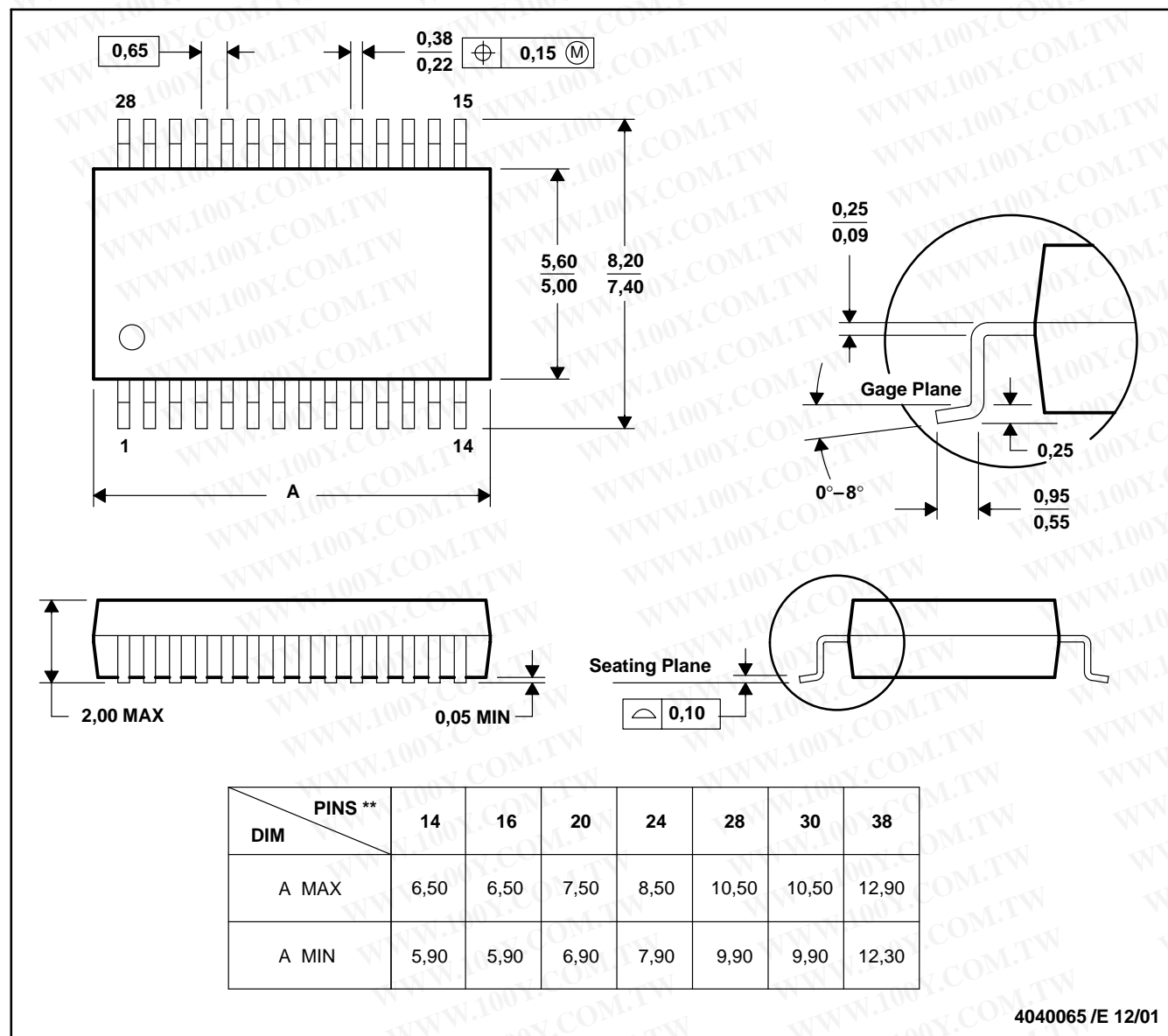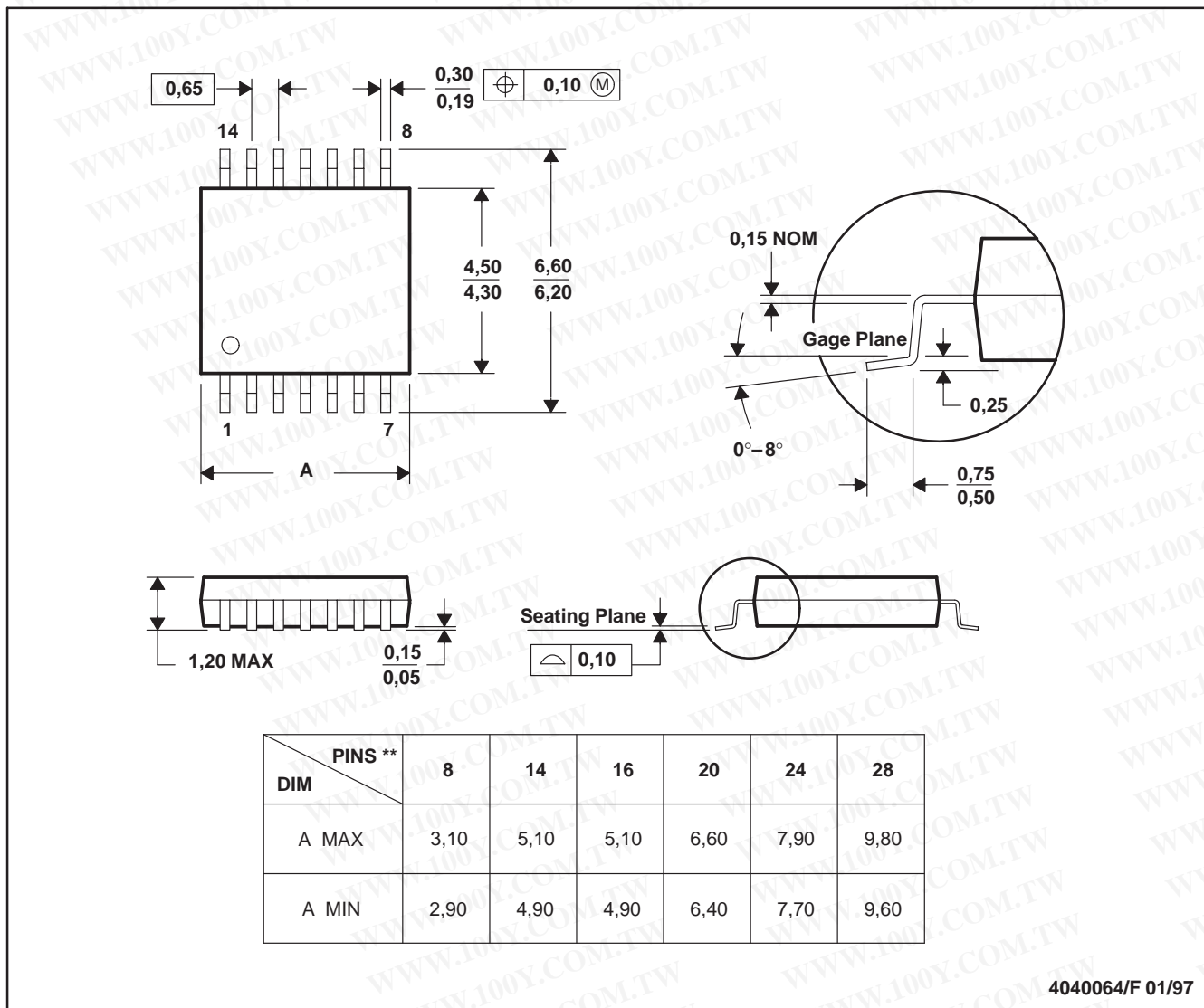|	PINS **	14	16	20	24
DIM					
A	MAX	10,50	10,50	12,90	15,30
A	MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**) **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

0,65

0,38
0,22

0,15 Ⓜ

28   15

5,60
5,00

8,20
7,40

0,25
0,09

Gage Plane

0,25

0°–8°

0,95
0,55

1   14

A

2,00 MAX

0,05 MIN

Seating Plane

0,10

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

PINS **	8	14	16	20	24	28
DIM						
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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