

CD4028B Types

BCD-to-Decimal Decoder

High-Voltage Types (20-Volt Rating)

■ CD4028B types are BCD-to-decimal or binary-to-octal decoders consisting of buffering on all 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7 if D = "0". High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

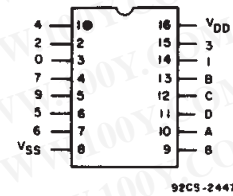
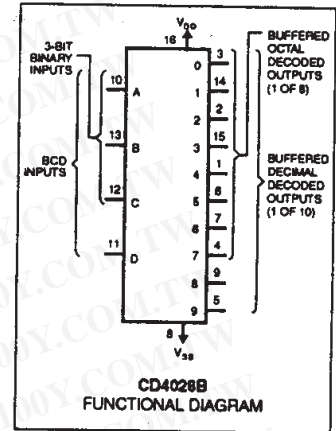
The CD4028B-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- BCD-to-decimal decoding or binary-to-octal decoding
- High decoded output drive capability
- "Positive logic" inputs and outputs. decoded outputs go high on selection
- Medium-speed operation.
 $t_{PHL}, t_{PLH} = 80 \text{ ns (typ.) @ } V_{DD} = 10 \text{ V}$
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
 1 V at $V_{DD} = 5 \text{ V}$
 2 V at $V_{DD} = 10 \text{ V}$
 2.5 V at $V_{DD} = 15 \text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Code conversion
- Indicator-tube decoder
- Address decoding—memory selection control



Top View
TERMINAL DIAGRAM

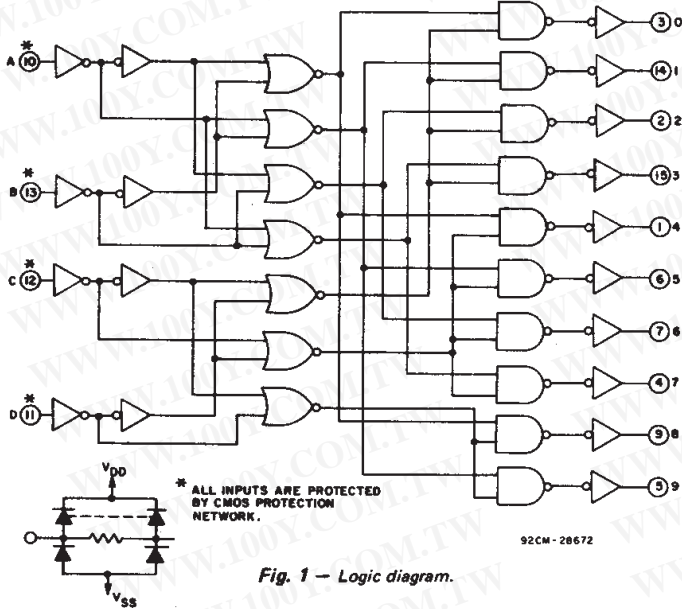


Fig. 1 - Logic diagram.

TABLE I - TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

I = HIGH LEVEL 0 = LOW LEVEL

MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 Voltages referenced to V_{SS} Terminal) -0.5V to +20V
- INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5\text{V}$
- DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{mA}$
- POWER DISSIPATION PER PACKAGE (P_D):
 For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW
 For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW
- OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$
- STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$
- LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max $+265^\circ\text{C}$

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RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55			+25			Max.		
				Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current, I_{DD} Max.	-	0.5	5	5	5	150	150	-	0.04	5	μA	
	-	0.10	10	10	10	300	300	-	0.04	10		
	-	0.15	15	20	20	600	600	-	0.04	20		
	-	0.20	20	100	100	3000	3000	-	0.08	100		
Output Low (Sink) Current I_{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA	
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-		
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-		
Output High (Source) Current, I_{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	1	-	mA	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-		
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-		
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-		
Output Voltage: Low-Level, V_{OL} Max.	-	0.5	5	0.05			-			0	0.05	V
	-	0.10	10	0.05			-			0	0.05	
	-	0.15	15	0.05			-			0	0.05	
Output Voltage: High-Level, V_{OH} Min.	-	0.5	5	4.95			4.95			5	-	V
	-	0.10	10	9.95			9.95			10	-	
	-	0.15	15	14.95			14.95			15	-	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	-	5	1.5			-			1.5	V	
	1.9	-	10	3			-			3		
	1.5, 13.5	-	15	4			-			4		
Input High Voltage, V_{IH} Min.	0.5, 4.5	-	5	3.5			3.5			-	-	V
	1.9	-	10	7			7			-	-	
	1.5, 13.5	-	15	11			11			-	-	
Input Current I_{IN} Max.	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1	μA	

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns, $R_L = 200$ k Ω

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} (V)	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH}	5	175	350	ns
	10	80	160	
	15	60	120	
Transition Time t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	-	5	7.5	pF

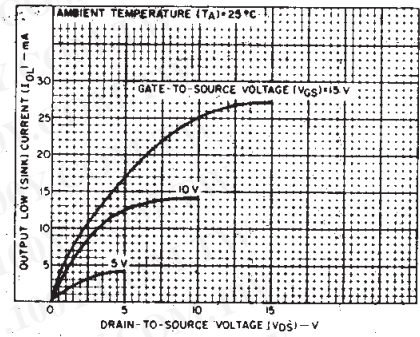


Fig. 2 - Typical output low (sink) current characteristics.

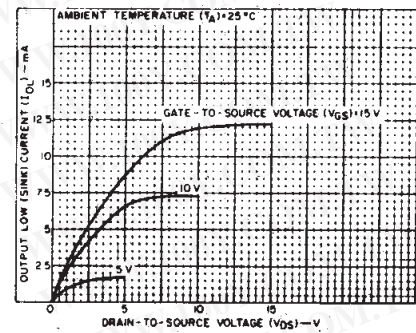


Fig. 3 - Minimum output low (sink) current characteristics.

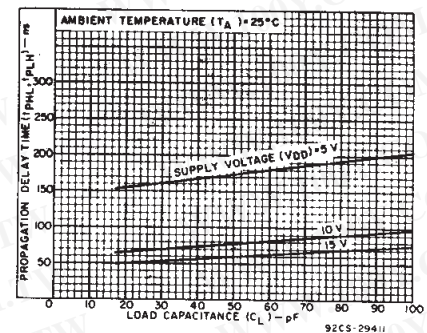


Fig. 4 - Typical propagation delay time as a function of load capacitance.

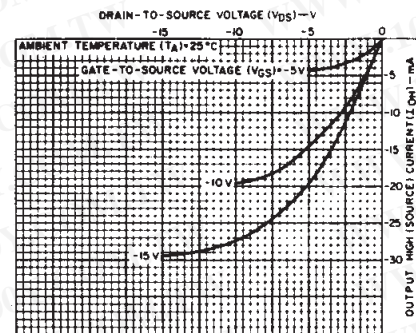


Fig. 5 - Typical output high (source) current characteristics.

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TABLE II - CODE CONVERSION CHART

INPUTS	INPUT CODES					OUTPUT NUMBER
	Hexa-Decimal		Decimal			
	4-BIT BINARY	4-BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN 4-2-2-1	
D C B A	0 0 0 0	0 0			0 0	0 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
	0 0 0 1	1 1			1 1	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	0 0 1 0	2 3		0 2	2 2	0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
	0 0 1 1	3 2	0 3	3 3		0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	0 1 0 0	4 7	1 4	4 4		0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0
	0 1 0 1	5 6	2		3	0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0
	0 1 1 0	6 4	3 1		4	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0
	0 1 1 1	7 5	4 2			0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0
	1 0 0 0	8 15	5			0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0
	1 0 0 1	9 14	6		5	0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
	1 0 1 0	10 12	7 9		6	0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
	1 0 1 1	11 13	8		5	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0
	1 1 0 0	12 8	9 5	6		0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0
	1 1 0 1	13 9	6 7	7		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
	1 1 1 0	14 11	8 8	8	8	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
	1 1 1 1	15 10	7 9	9		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

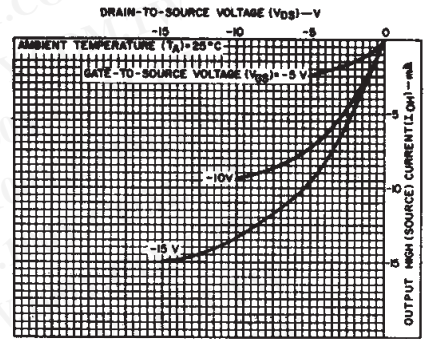


Fig. 6 - Minimum output high (source) current characteristics.

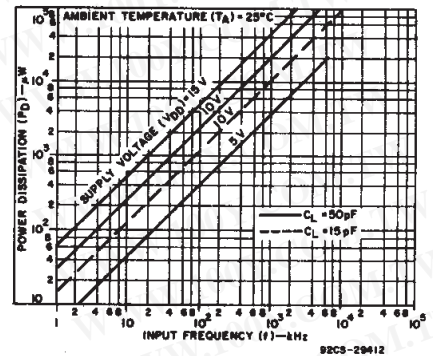


Fig. 7 - Typical dynamic power dissipation as a function of input frequency.

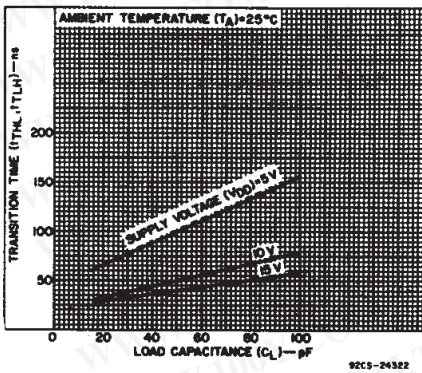


Fig. 8 - Typical transition time as a function of load capacitance.

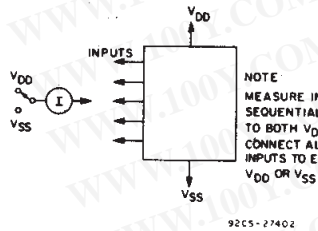


Fig. 9 - Input current test circuit.

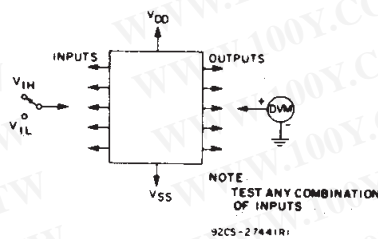


Fig. 11 - Input voltage test circuit.

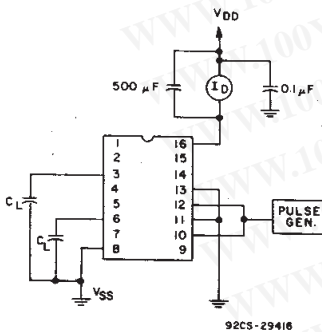


Fig. 10 - Dynamic power dissipation test circuit.

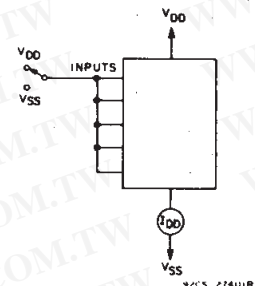


Fig. 12 - Quiescent device current test circuit.

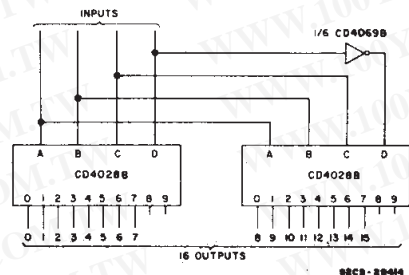
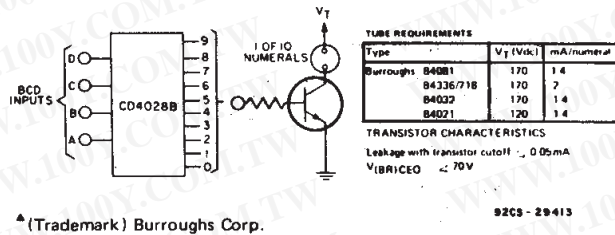


Fig. 13 - Code conversion circuit.

The circuit shown in Fig.13 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028B to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.

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^(Trademark) Burroughs Corp.

Fig. 14 — Neon readout (Nixie Tube[^]) display application.

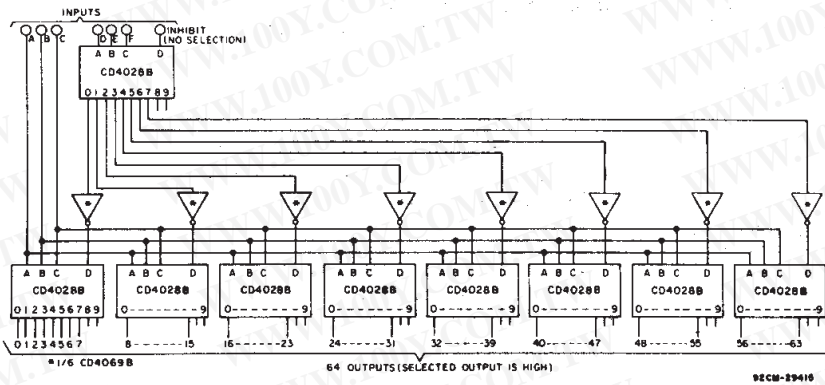
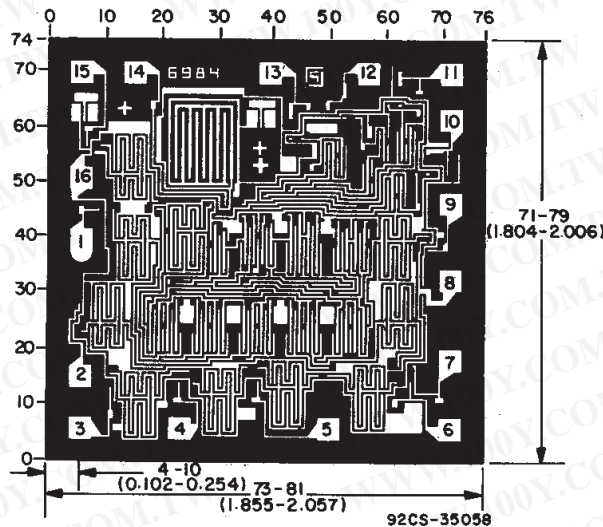


Fig. 15 — 6-bit binary to 1-of-64 address decoder.



CD4028BH DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4028BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4028BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4028BF	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD4028BF3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD4028BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4028BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

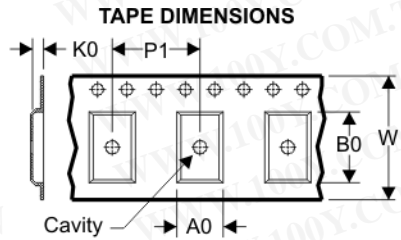
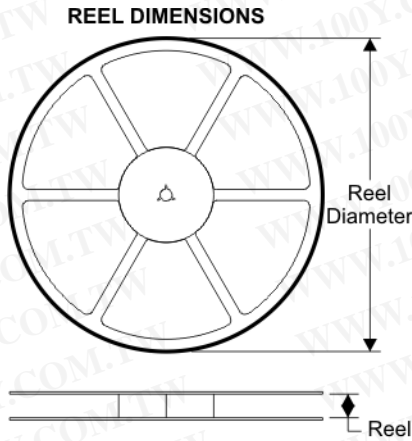
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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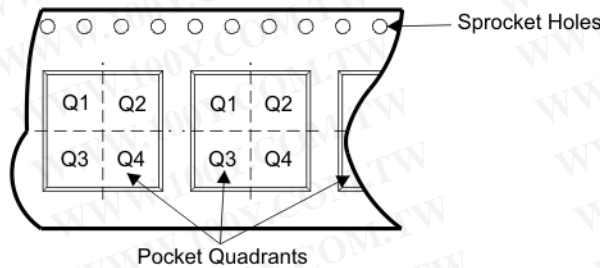
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TAPE AND REEL BOX INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

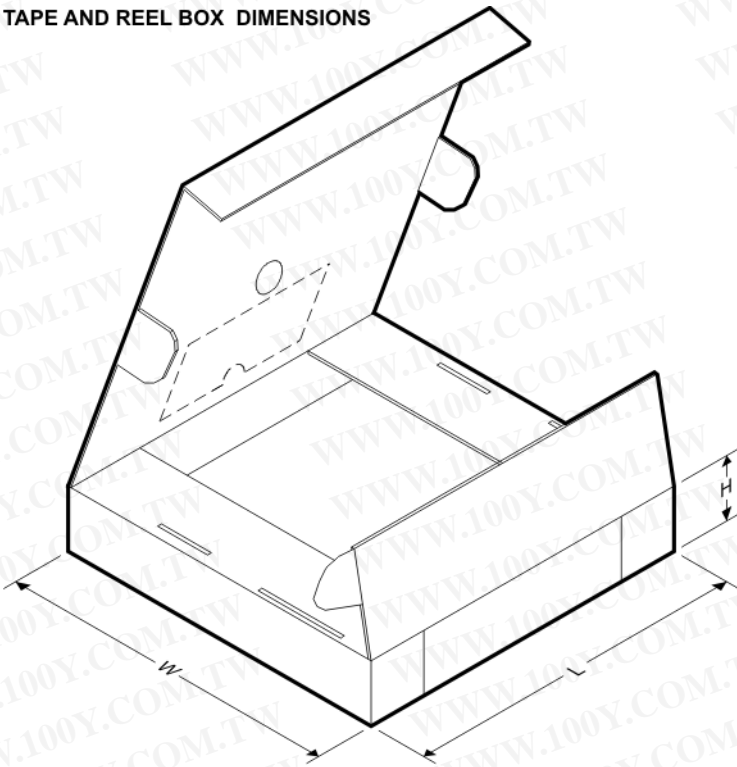
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4028BM96	D	16	SITE 27	330	16	6.5	10.3	2.1	8	16	Q1
CD4028BNSR	NS	16	SITE 41	330	16	8.2	10.5	2.5	12	16	Q1
CD4028BPWR	PW	16	SITE 41	330	12	7.0	5.6	1.6	8	12	Q1

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TAPE AND REEL BOX DIMENSIONS



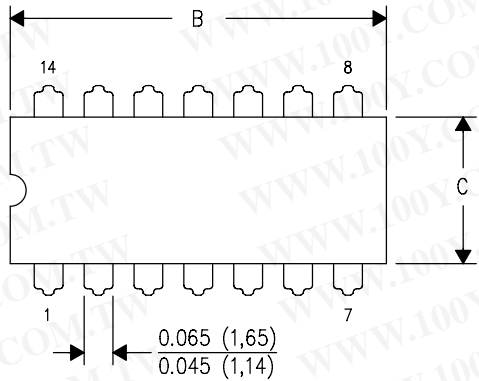
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CD4028BM96	D	16	SITE 27	342.9	336.6	28.58
CD4028BNSR	NS	16	SITE 41	346.0	346.0	33.0
CD4028BPWR	PW	16	SITE 41	346.0	346.0	29.0

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 勝特力电子(深圳) 86-755-83298787
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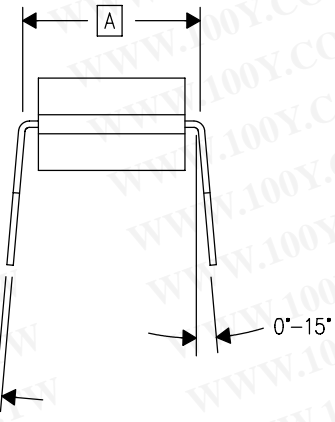
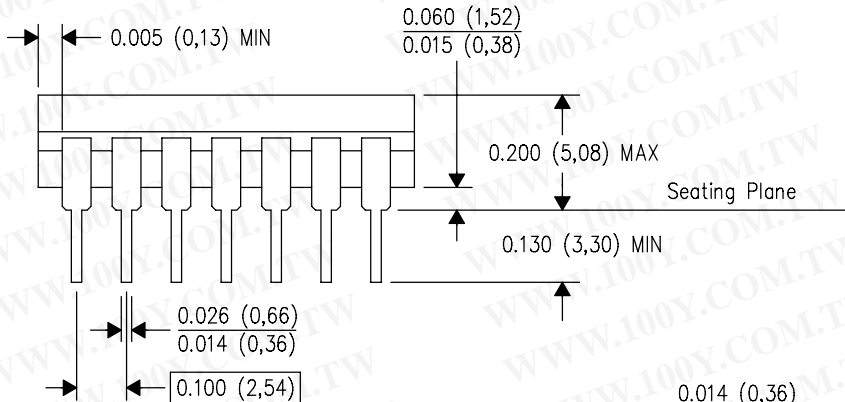
勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
 Http://www.100y.com.tw

J (R-GDIP-T**)
 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



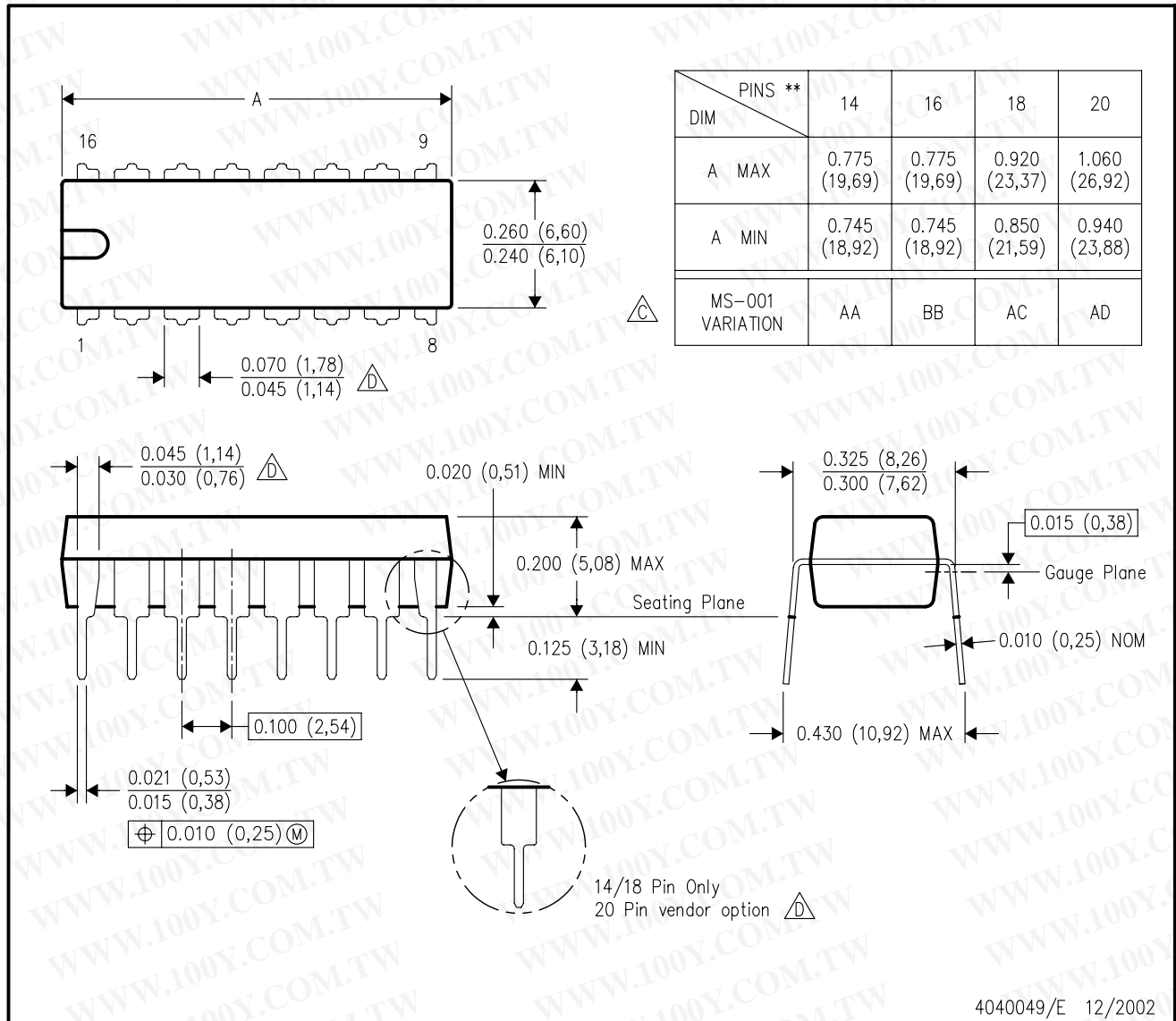
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

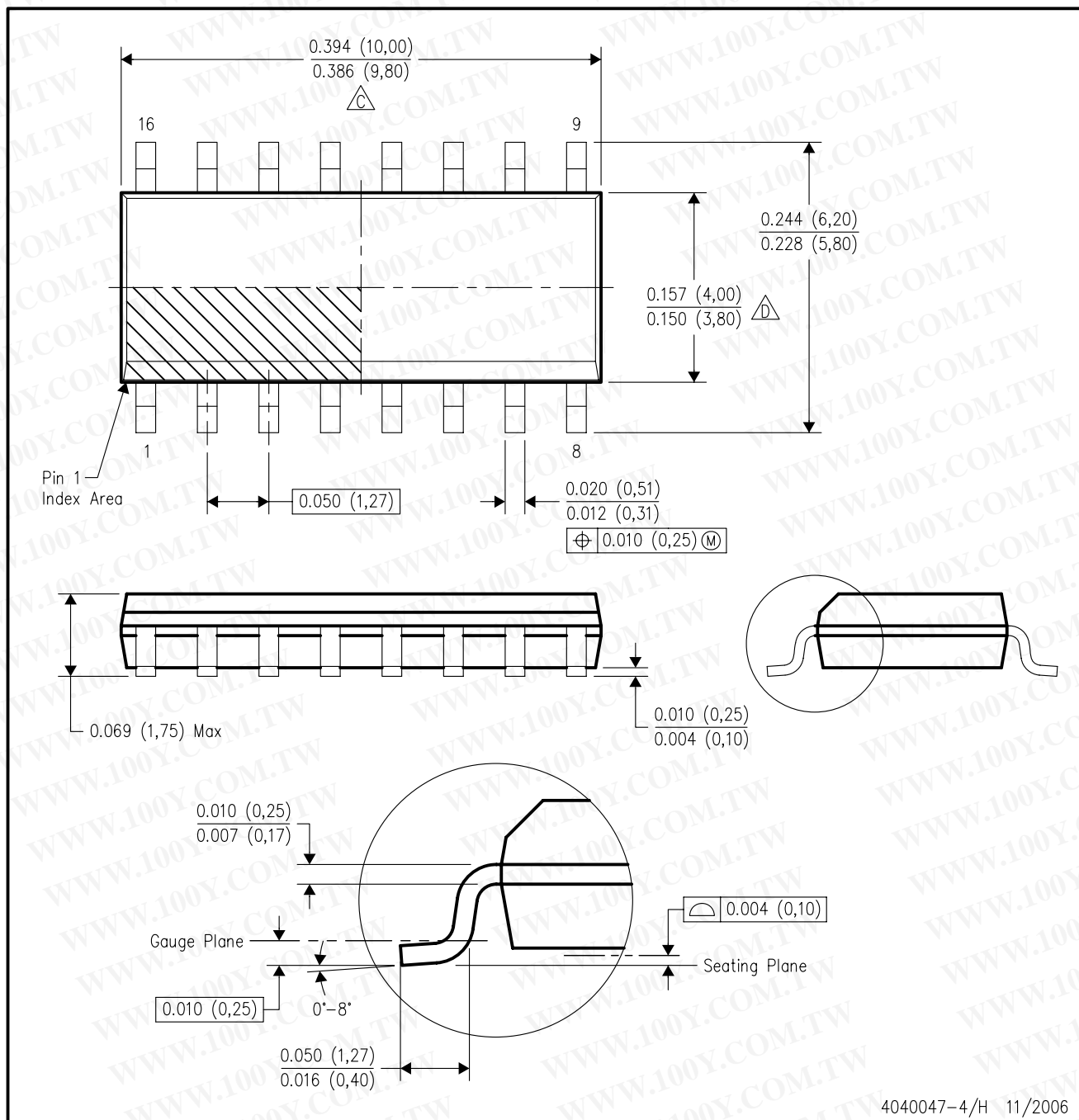


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

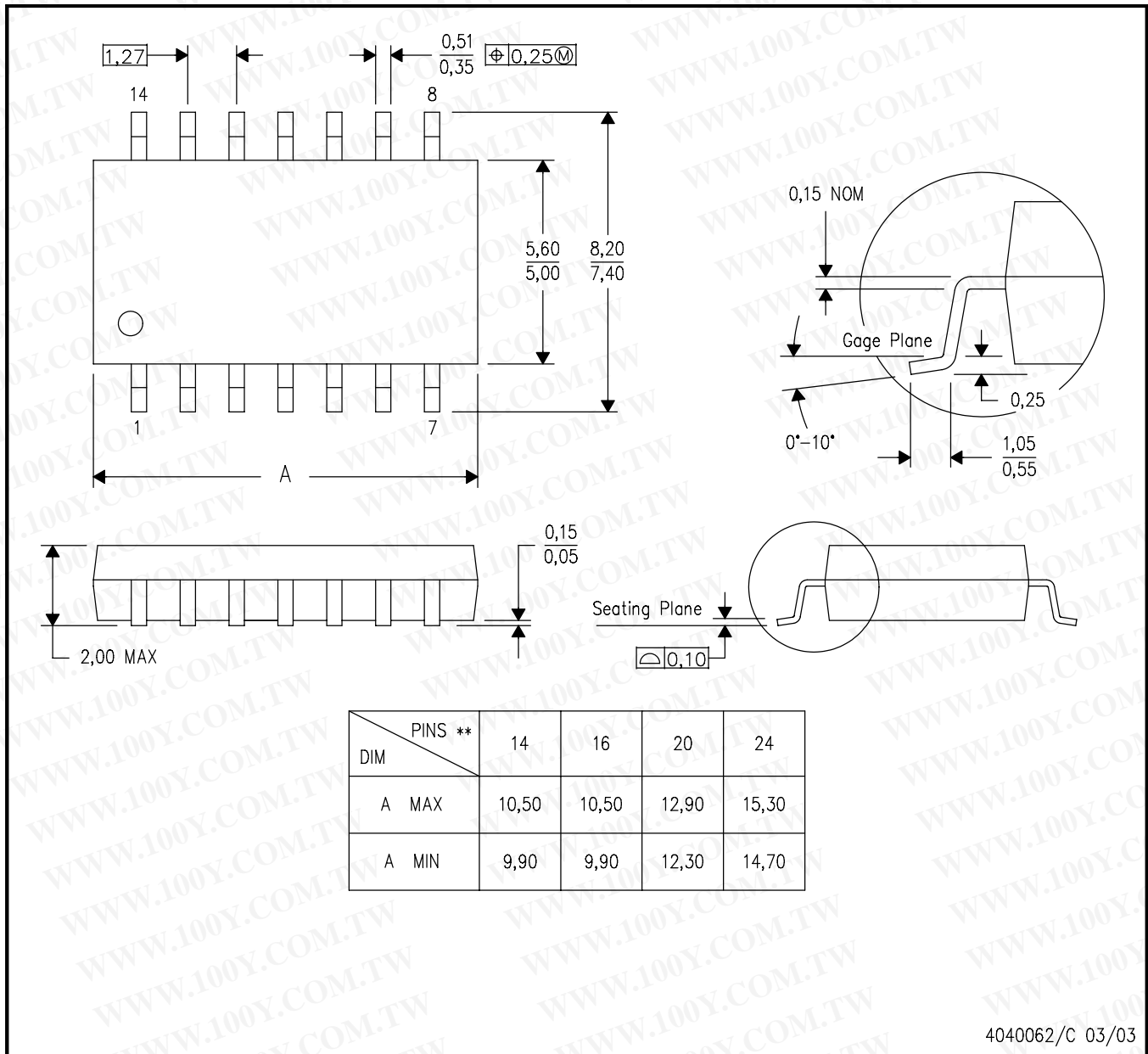
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - \triangle Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - \triangle Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

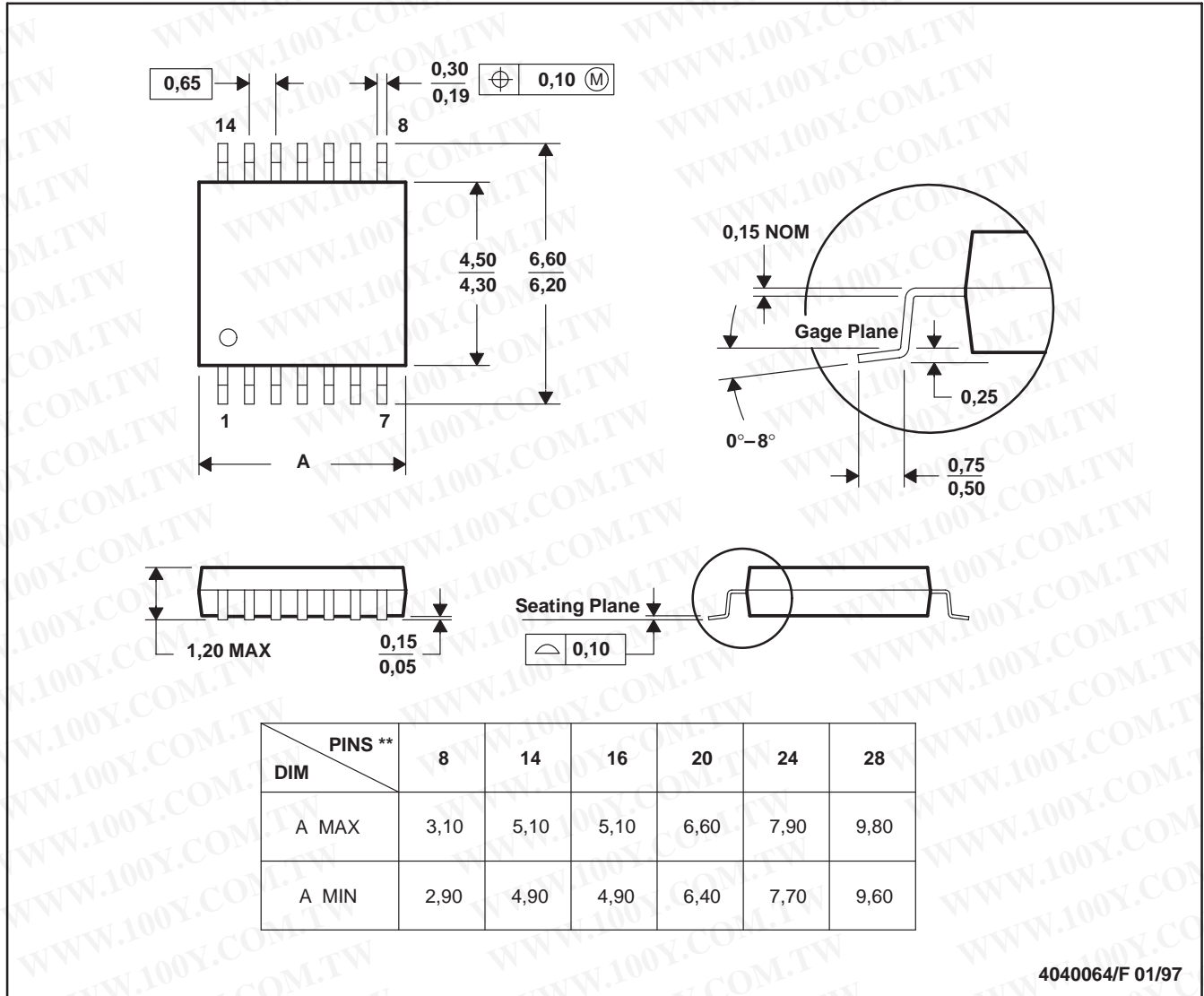


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153