

DATA SHEET

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

TEA6820T; TEA6822T

In Car Entertainment (ICE) car radio

Preliminary specification
Supersedes data of 1996 Oct 18
File under Integrated Circuits, IC01

1997 Feb 12

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TEA6820T; TEA6822T

FEATURES

General

- FM mixer for conversion from FM-IF₁ = 72.2 MHz to FM-IF₂ = 10.7 MHz
- AM mixer for conversion from AM-IF₁ = 10.7 MHz to AM-IF₂ = 450 kHz
- FM-IF gain stage
- Crystal oscillator providing mixer frequencies and references for IF-count and stereo decoder
- FM quadrature demodulator with automatic centre frequency adjustment and THD compensation
- Level, multi-path and noise detectors
- Soft mute
- Stereo noise cancelling and variable de-emphasis
- PLL stereo decoder
- Noise blanker
- AM IF-amplifier and demodulator
- I²C-bus transceiver with interface to enable direct data transfer to radio front-end
- IF-count for AM and FM
- Reference frequency generation for PLL synthesizer.



Stereo decoder

- Adjustment-free PLL VCO
- Pilot depending mono/stereo switching
- Analog control of mono/stereo blend
- Adjacent channel noise suppression (114 kHz)
- Pilot cancelled
- Analog control of de-emphasis
- Integrated low-pass filters for 190 kHz adjacent channel interferences and signal delay for interference absorption circuit.

GENERAL DESCRIPTION

The TEA6820T together with the TEA6810T and the TEA6822T together with the TEA6811T forms an AM/FM electronic tuned car radio in a double conversion receiver concept.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6820T	VSO56	plastic very small outline package; 56 leads; face down	SOT190-2
TEA6822T	VSO56	plastic very small outline package; 56 leads	SOT190-1

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DDA1}	analog supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I _{DDA1}	analog supply current 1 (pin 5)	FM mode	17	21	25	mA
		AM mode	14	17	21	mA
I ₁₉ + I ₂₀	total FM mixer output current		4.8	6.0	7.2	mA
I ₂₂ + I ₂₃	total AM mixer output current		10	12	14	mA
V _{DDA2}	analog supply voltage 2 (pin 28)	note 1	7.0	8.5	10	V
		operating range	8.1	8.5	8.9	V
I _{DDA2}	analog supply current 2 (pin 28)	FM mode	2.4	3.0	3.6	mA
V _{DDA3}	analog supply voltage 3 (+8.5 V; pin 56)	note 1	7.0	8.5	10	V
		operating range	8.1	8.5	8.9	V
I _{DDA3}	analog supply current 3 (pin 56)	FM mode	19	24	28	mA
		AM mode	9.5	12	15	mA
V _{DDD}	digital supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I _{DDD}	digital supply current (pin 52)	note 1	8	10	12	mA
$\frac{S + N}{N}$	signal plus noise-to-noise ratio	FM mode; $\Delta f = 22.5$ kHz at pins 43 and 47	66	75	–	dB
		AM mode; m = 0.3	54	60	–	dB
THD	total harmonic distortion	FM mode; $\Delta f = 75$ kHz	–	0.1	0.35	%
		AM mode	–	1.5	3	%
α_{CS}	channel separation (adjusted)		40	–	–	dB
T _{amb}	operating ambient temperature		–40	–	+85	°C

Note

1. IC is operating; specified parameters may deviate from limits which are valid for operating range.

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BLOCK DIAGRAM

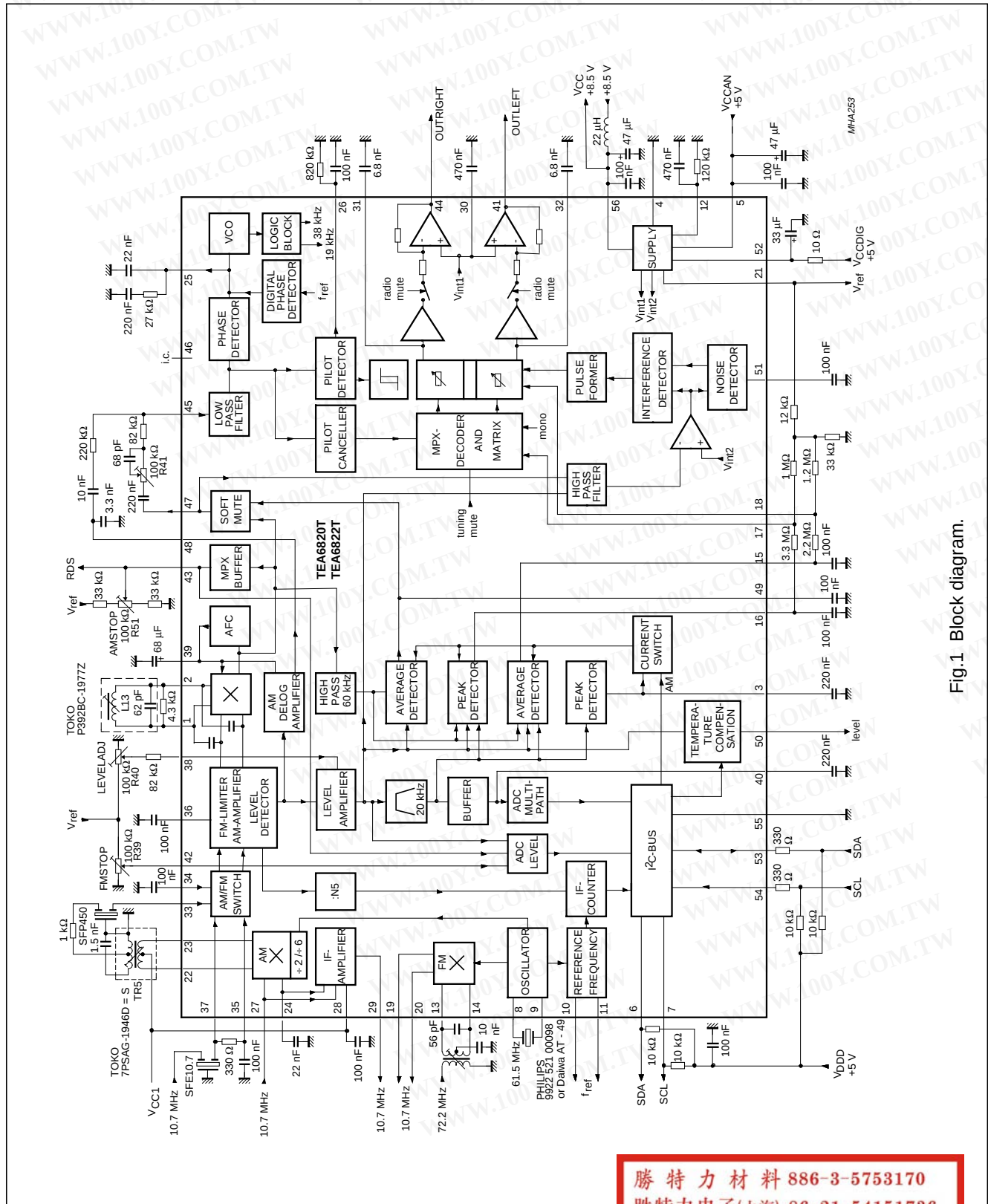


Fig.1 Block diagram.

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PINNING

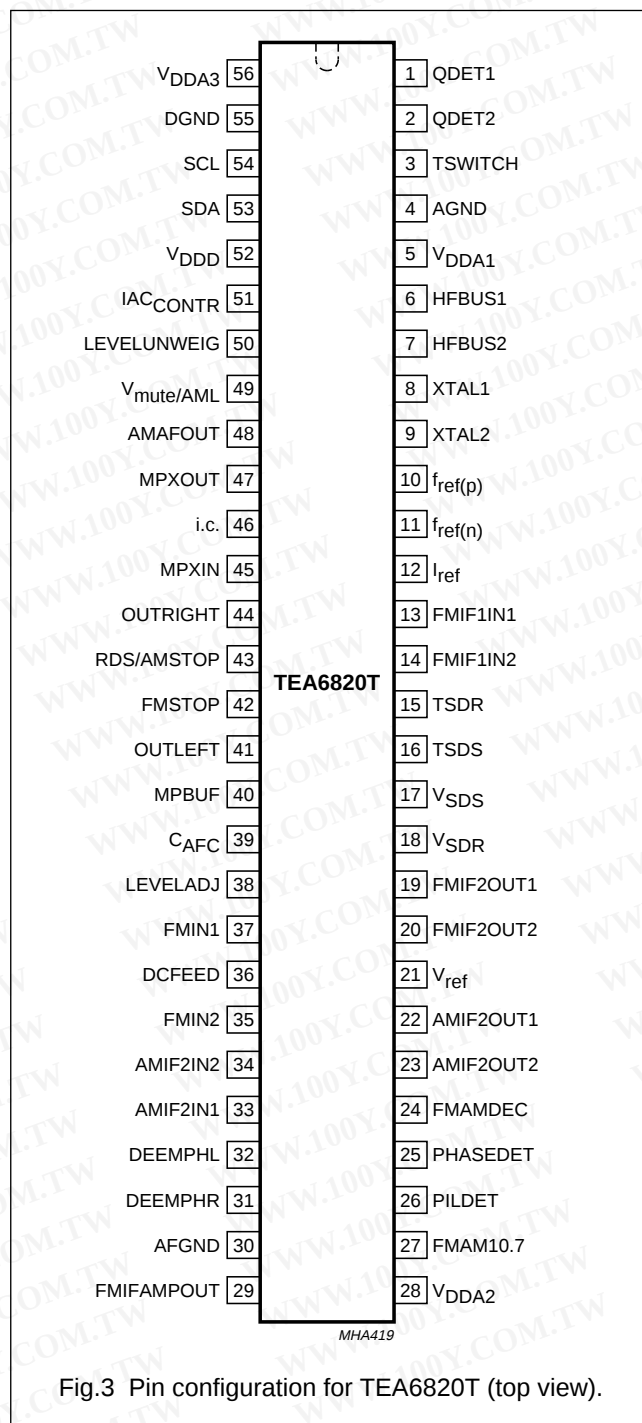
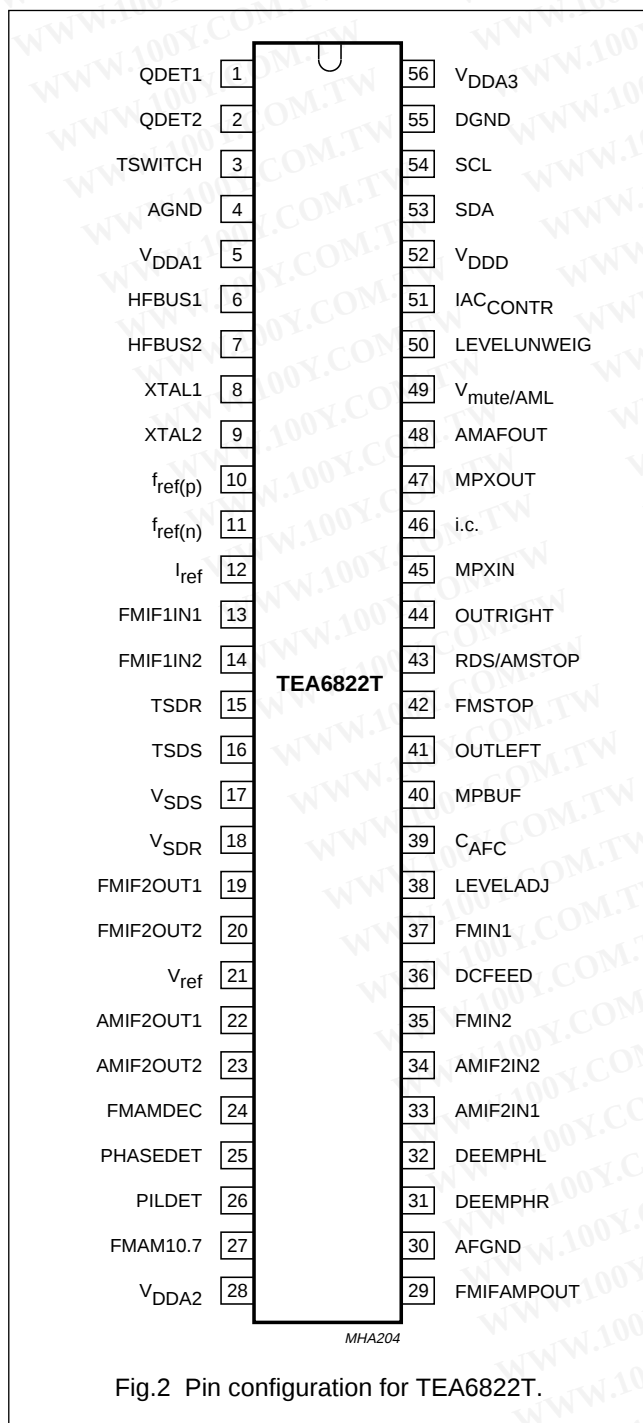
SYMBOL	PIN	DESCRIPTION
QDET1	1	demodulator tank 1
QDET2	2	demodulator tank 2
TSWITCH	3	time switch input
AGND	4	analog ground
V _{DDA1}	5	analog supply voltage 1 (+5 V)
HFBUS1	6	HF bus 1 output; pull-up to +5 V
HFBUS2	7	HF bus 2 output; pull-up to +5 V
XTAL1	8	crystal oscillator 1
XTAL2	9	crystal oscillator 2
f _{ref(p)}	10	PLL reference frequency output (p)
f _{ref(n)}	11	PLL reference frequency output (n)
I _{ref}	12	reference current
FMIF1IN1	13	72 MHz FM-IF input 1
FMIF1IN2	14	72 MHz FM-IF input 2
TSDR	15	time constant for SDR
TSDS	16	time constant for SDS
V _{SDS}	17	SDS control voltage input
V _{SDR}	18	SDR control voltage input
FMIF2OUT1	19	FM mixer output 1
FMIF2OUT2	20	FM mixer output 2
V _{ref}	21	reference voltage output
AMIF2OUT1	22	AM mixer output 1
AMIF2OUT2	23	AM mixer output 2
FMAMDEC	24	FM/AM 10.7 MHz decoupling
PHASEDET	25	phase detector output
PILDET	26	pilot detector output
FMAM10.7	27	FM/AM 10.7 MHz input
V _{DDA2}	28	analog supply voltage 2

SYMBOL	PIN	DESCRIPTION
FMIFAMPOUT	29	FM-IF amplifier output
AFGND	30	AF ground
DEEMPHR	31	de-emphasis capacitor right
DEEMPHL	32	de-emphasis capacitor left
AMIF2IN1	33	AM-IF ₂ input 1
AMIF2IN2	34	AM-IF ₂ input 2
FMIN2	35	FM limiter input
DCFEED	36	DC feed FM limiter
FMIN1	37	FM limiter input
LEVELADJ	38	level adjustment input
C _{AFC}	39	AFC capacitor
MPBUF	40	multi-path buffer time constant
OUTLEFT	41	AF output left
FMSTOP	42	FMSTOP adjustment input
RDS/AMSTOP	43	MPX for RDS/AMSTOP adjustment input
OUTRIGHT	44	AF output right
MPXIN	45	stereo decoder MPX input
i.c.	46	internally connected
MPXOUT	47	FM demodulator MPX output
AMAFOUT	48	AM demodulator AF output
V _{mute/AML}	49	mute voltage/AM level
LEVELUNWEIG	50	unweighted level output
IAC _{CONTR}	51	IAC control voltage
V _{DDD}	52	digital supply voltage
SDA	53	serial data input/output; pull-up to +5 V
SCL	54	serial clock input; pull-up to +5 V
DGND	55	digital ground
V _{DDA3}	56	analog supply voltage 3 (+8.5 V)

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FUNCTIONAL DESCRIPTION

Stereo decoder

By changing the value of the input resistor at pin 12 the MPX input can be adapted to the level of the FM demodulator output (see Fig.16).

A 3rd order low-pass filter ($f_g = 90$ kHz) at the MPX input provides an extra 190 kHz ACI suppression.

An interference gate is connected at the MPX demodulator outputs. For AM the VCO is switched off.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 (pin 5)		-0.3	+6.5	V
V_{DDA2}	analog supply voltage 2 (pin 28)		-0.3	+12	V
V_{DDA3}	analog supply voltage 3 (pin 56)		-0.3	+12	V
V_{DDD}	digital supply voltage (pin 52)		-0.3	+6.5	V
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		-40	+85	°C
V_{es}	electrostatic handling	note 1			
	pins 8 and 9		-100	+100	V
	all other pins		-300	+300	V

Note

1. Charge device model class B: equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

CHARACTERISTICS

$V_{56-4} = V_{28-4} = 8.5$ V; $V_{5-4} = V_{52-55} = 5$ V; $T_{amb} = 25$ °C; $f_{mod} = 1$ kHz; deviation = 22.5 kHz; $R_g = 50$ Ω ; $V_{37-35} = 10$ mV; with de-emphasis = 50 μ s; coil quality = 15; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current consumption						
I_{DDA1}	analog supply current 1 (pin 5)	FM mode	17	21	25	mA
		AM mode	14	17	21	mA
I_{DDA2}	analog supply current 2 (pin 28)	FM mode	2.4	3.0	3.6	mA
I_{DDA3}	analog supply current 3 (pin 56)	FM mode	19	24	28	mA
		AM mode	9.5	12	15	mA
I_{DDD}	digital supply current (pin 52)		8	10	12	mA
$I_{19} + I_{20}$	total FM mixer output current		4.8	6.0	7.2	mA
$I_{22} + I_{23}$	total AM mixer output current	AM mode	10	12	14	mA
FM-IF path; see Fig.4						
$V_{19-20 \max(p-p)}$	maximum output voltage (peak-to-peak value)		12.0	14.0	–	V
$I_{19}; I_{20}$	mixer bias current		2.4	3.0	3.6	mA
	mixer leakage current	in AM position	–	–	2	μ A
$I_{19IF2}/V_{13-14IF1}$	conversion gain		1.65	1.9	2.2	mS
R_i	input resistance (pins 13 to 14)		5	7	–	k Ω
C_i	input capacitance (pins 13 to 14)		–	3	4.5	pF
R_{opt}	optimum generator resistance		–	1.2	–	k Ω
R_o	output resistance (pins 19 to 20)		15	20	–	k Ω
C_o	output capacitance (pins 19 to 4 and pins 20 to 4)		–	12	14	pF
IP3	third order intermodulation		114	124	–	dB μ V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
f_{osc}	oscillator frequency		–	61.5	–	MHz
Δf_{osc}	oscillator frequency spread		–	–	250	Hz
$\Delta f_{osc}/\Delta T$	temperature dependence of oscillator frequency	crystal type PHILIPS 9922 521 00098	–	30×10^{-6}	–	K ⁻¹
R_1	crystal motional resistance		–	–	70	Ω
C_0	crystal shunt capacitance		–	–	5	pF
FM-IF₂ amplifier						
$V_{27-24 \text{ max(rms)}}$	maximum input voltage for 1 dB compression point (RMS value)		80	110	–	mV
$V_{29-4 \text{ max(rms)}}$	maximum output voltage (RMS value)		220	320	–	mV
V_{29-4}/V_{27-24}	amplifier gain	loaded with 330 Ω ; see Fig.5	9	12	15	dB
$\Delta V_{29-4}/V_{27-24}$	gain temperature dependence	$-25^\circ\text{C} < T_{amb} < +50^\circ\text{C}$	–	0.1	–	dB/K
		$+50^\circ\text{C} < T_{amb} < +75^\circ\text{C}$	0	–	–	dB/K
R_i	input resistance (pins 27 to 24)		300	330	360	Ω
C_i	input capacitance (pins 27 to 4)		–	–	5	pF
R_o	output resistance (pin 29)		300	330	360	Ω
C_o	output capacitance (pins 29 to 4)		–	–	5	pF
FM-IF₂ limiter						
$V_{o \text{ 1-2(p-p)}}$	limiter output voltage (peak-to-peak value)		500	700	–	mV
V_{1-2}/V_{37-35}	limiter gain	see Fig.6	–	80	–	dB
C_i	input capacitance (pins 37 to 4)		–	–	5	pF
R_o	output resistance (pins 1 to 2)		–	–	1.0	k Ω
C_o	output capacitance (pins 1 to 2)		10	15	20	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator						
$V_{47-4(rms)}$	MPX output voltage (RMS value)		160	200	240	mV
$V_{43-4(rms)}$	MPX output voltage for RDS (RMS value)		160	200	240	mV
$V_{37-35(rms)}$	start of limiting voltage (RMS value)	$\alpha_{AF} = -3$ dB	–	25	40	μ V
$V_{37-35(rms)}$	input voltage for signal plus noise-to-noise ratio (RMS value)	see Fig.7 for pin 47 (MPXOUT) and Fig.8 for pin 43 (RDS/AMSTOP) $\frac{S+N}{N} = 26$ dB $\frac{S+N}{N} = 46$ dB	– –	30 70	45 100	μ V
ΔV_{43DC}	residual DC-offset voltage	ΔL_{demod} = typical value $10 \mu V < V_{37-35} < 80 \mu V$ $80 \mu V < V_{37-35} < 800$ mV	– –	100 10	1000 30	mV mV
V_{43FM}/V_{43AM}	AM suppression	$\Delta f = 22.5$ kHz; $f_{modAM} = 1$ kHz; $m_{AM} = 30\%$; $V_{37-35} = 3$ to 300 mV	50	60	–	dB
V_{47FM}/V_{47AM}	AM suppression	$V_{37-35} = 1$ to 300 mV	50	60	–	dB
$\Delta V_{43-44AFCdis}$ $/\Delta V_{43-44AFCactive}$	demodulator frequency control voltage (AFC) efficiency at 100 kHz detune from exact tuning		28	32	–	dB
R_o	output resistance (pin 47)		–	–	3	k Ω
	output resistance (pin 43)		–	–	1.5	k Ω
	AF bandwidth (pin 43)		200	–	–	kHz
$\frac{S+N}{N}$	signal plus noise-to-noise ratio		66	75	–	dB
THD	total harmonic distortion	detuning ≤ 50 kHz; $\Delta f = 75$ kHz; $f_{mod} = 1$ kHz without de-emphasis; L_{demod} = typical value pin 43; $V_{37-35} = 300 \mu V$ to 800 mV	–	0.1	0.35	%
		pin 47; $V_{37-35} = 1$ to 800 mV	–	0.1	0.35	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Unweighted voltage level						
V ₅₀₋₄	unweighted voltage level	see Fig.9; V ₃₈ = 2.52 V V ₃₇₋₃₅ ≤ 2.5 μV V ₃₇₋₃₅ = 1.0 mV	1.6 2.7	2.2 3.4	3.0 4.7	V V
ΔV ₅₀₋₄ /ΔV ₃₇₋₃₅	slope of unweighted voltage level	100 μV (RMS) ≤ V ₃₇₋₃₅ < 300 mV temperature compensation off temperature compensation on	0.75 0.6	0.9 0.75	1.05 0.9	V/20 dB V/20 dB
ΔV ₅₀₋₄ /VK	temperature dependence	V ₃₇₋₃₅ = 1 mV temperature compensation off temperature compensation on	— —	5.0 2.0	— —	mV/VK mV/VK
I _{50(max)source}	maximum output source current		0.3	—	—	mA
I _{50(max)sink}	maximum output sink current		–50	—	—	μA
R _{o50}	output resistance		—	—	300	Ω
ADJUSTMENT OF UNWEIGHTED VOLTAGE LEVEL AND V_{mute}/AML; note 1						
ΔV ₅₀	adjusting range voltage	V ₃₇₋₃₅ = 10 mV (RMS)	–1.8	—	+1.8	V
V ₃₈₋₄	internal bias voltage		—	2.6	—	V
ΔV ₅₀₋₄ /ΔV ₃₈₋₄	adjusting gain		—	–0.9	—	—
R _{i38}	input resistance		—	80	—	kΩ
MUTING DEPENDENCE ON ADJUST OF LEVEL UNWEIGHTED VOLTAGE; note 2						
α = V ₄₃ /V ₄₇	start of mute	V ₄₉ /V ₂₁ = 0.625	1	3	7	dB
Δα/ΔV ₄₉	mute slope	α = –6 dB	—	25	—	dB/V
Soft mute, time constant control, mono/stereo blend and high-cut control; see Fig.22						
MUTE VOLTAGE; note 3						
V ₄₉₋₄	mute voltage	V ₃₈ = 2.52 V V ₃₇₋₃₅ < 2.5 μV V ₃₇₋₃₅ = 1.0 mV	1.8 2.7	2.2 3.4	3.2 4.7	V V
ΔV ₄₉₋₄ /ΔV ₃₇₋₃₅	slope of mute voltage	100 μV (RMS) ≤ V ₃₇₋₃₅ < 300 mV	0.75	0.9	1.05	V/20 dB
ΔV ₄₉₋₄ /VK	temperature dependence	V ₃₇₋₃₅ = 1 mV	—	5.0	—	mV/VK

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ATTACK AND DECAY TIME FOR MUTE VOLTAGE						
I ₄₉	charge current	pin 3 connected to GND	–	3.5	–	μA
	discharge current	pin 3 connected to GND	–	–4.0	–	μA
	charge current	pin 3 connected to pin 5	–	150	–	μA
	discharge current	pin 3 connected to pin 5	–	–170	–	μA
Δf	muting activated by 60 kHz FM interference	V ₄₉ < 3 V; V ₃₇₋₃₅ = 3 mV; f _{mod} = 60 kHz				
		pin 3 connected to GND; V ₄₃ /V ₄₇ = 9 dB	–	40	–	kHz
		pin 3 connected to pin 5; V ₄₃ /V ₄₇ = 6 dB	–	40	–	kHz
V ₄₃ /V ₄₇	maximum mute depth by 60 kHz FM interference	pin 3 connected to GND	–	15	–	dB
		pin 3 connected to pin 5	–	10	–	dB
TIME CONSTANT FOR MONO/STEREO BLEND VOLTAGE; note 4						
I ₁₆	charge current	V ₃₇₋₃₅ = 3 mV; pin 3 connected to GND	–	0.6	–	μA
	discharge current	V ₃₇₋₃₅ = 3 mV; pin 3 connected to GND	–	–17	–	μA
	charge current	V ₃₇₋₃₅ = 3 mV; pin 3 connected to pin 5	–	23	–	μA
	discharge current	V ₃₇₋₃₅ = 3 mV; pin 3 connected to pin 5	–	–750	–	μA
m	mono/stereo blend activated by 20 kHz AM interference	V ₁₆ < 2 V; V ₃₇₋₃₅ = 3 mV; R _{L16} > 50 MΩ; f _{mod} = 20 kHz; data byte 2 bit 5 = 0				
		pin 3 connected to GND	–	45	–	%
		pin 3 connected to pin 5	–	45	–	%
		data byte 2 bit 5 = 1				
		pin 3 connected to GND	–	55	–	%
		pin 3 connected to pin 5	–	55	–	%
Δf	mono/stereo blend activated by 60 kHz FM interference	V ₁₆ < 2 V; V ₃₇₋₃₅ = 3 mV; R _{L16} > 50 MΩ; f _{mod} = 60 kHz				
		pin 3 connected to GND	–	50	–	kHz
		pin 3 connected to pin 5	–	50	–	kHz

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TIME CONSTANT FOR HIGH-CUT CONTROL VOLTAGE SDR; note 5						
I ₁₅	charge current	V ₃₇₋₃₅ = 3 mV; pin 3 connected to GND	–	0.6	–	μA
	discharge current	V ₃₇₋₃₅ = 3 mV; pin 3 connected to GND	–	–0.7	–	μA
	charge current	V ₃₇₋₃₅ = 3 mV; pin 3 connected to pin 5	–	41	–	μA
	discharge current	V ₃₇₋₃₅ = 3 mV; pin 3 connected to pin 5	–	–44	–	μA
m	high-cut control activated by 20 kHz AM interference	V ₁₅ < 2 V; V ₃₇₋₃₅ = 3 mV; R _{L15} > 50 MΩ; f _{mod} = 20 kHz pin 3 connected to GND pin 3 connected to pin 5	– –	45 45	– –	% %
Δf	high-cut control activated by 60 kHz FM interference	V ₁₅ < 2 V; V ₃₇₋₃₅ = 3 mV; R _{L15} > 50 MΩ; f _{mod} = 60 kHz pin 3 connected to GND pin 3 connected to pin 5	– –	50 50	– –	kHz kHz
MULTI-PATH DETECTOR						
f _{MP}	multi-path detector band-pass centre frequency		–	20	–	kHz
B _{MP}	band-pass bandwidth		7.0	–	–	kHz
Reference voltage						
V ₂₁₋₄	output voltage	I ₂₁ = –1 mA	4.5	5.1	5.7	V
ΔV ₂₁₋₄	temperature dependence		–	3.3	–	mV/VK
I ₂₁	output current		–	–	1	mA
AM-IF path; see Fig.14 and notes 6 and 7						
V _{22-23 max(p-p)}	maximum output voltage (peak-to-peak value)		12	15	–	V
I ₂₂ , I ₂₃	mixer bias current		5.0	6.0	7.0	mA
	mixer leakage current	in FM position	–	–	2	μA
I _{22IF2} /V _{27-24IF1}	conversion gain		2.2	2.7	3.4	mS
R ₂₇₋₂₄	input resistance		300	330	360	Ω
C ₂₇₋₂₄	input capacitance		–	5	8	pF
R ₂₂₋₂₃	output resistance		10.0	20.0	–	kΩ
C ₂₂₋₂₃	output capacitance		–	5	10	pF
IP3	third order intermodulation		–	137	–	dBμV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM DETECTOR; notes 8 and 9						
$V_{48-4(rms)}$	AF output level (RMS value)	$R_{L48} > 500 \text{ k}\Omega$; $100 \text{ }\mu\text{V} \leq V_{33-34} \leq 300 \text{ mV}$	190	240	290	mV
$V_{33-34(rms)}$	sensitivity voltage (RMS value)	$\frac{S+N}{N} = 26 \text{ dB}$	–	50	75	μV
		$\frac{S+N}{N} = 46 \text{ dB}$	–	200	400	μV
	AM-IF ₂ minimum input voltage (RMS value)	THD $\leq 5\%$; $m = 0.8$	–	–	100	μV
	AM-IF ₂ maximum input voltage (RMS value)	THD $\leq 5\%$; $m = 0.8$	800	–	–	mV
R_{33-34}	IF ₂ input resistance		1.8	2.0	2.2	k Ω
C_{24-23}	IF ₂ input capacitance		–	10	15	pF
R_{048}	output resistance		27	33	39	k Ω
C_{048}	output capacitance		–	–	10	pF
$\frac{S+N}{N}$	signal plus noise-to-noise ratio		54	60	–	dB
THD	total harmonic distortion	$m = 0.8$; $300 \text{ }\mu\text{V} \leq V_{33-34} \leq 200 \text{ mV}$	–	1.5	3.0	%

Notes to the characteristics

- For typical adjusting range see Figs 10 and 13.
- For typical curve see Fig.11.
- The static mute voltage follows the unweighted voltage level as function of FM-IF₂ voltage and level adjustment voltage V_{38-4} . It additionally depends on multi-path level, noise (adjacent channel interferences) and the position of TSWITCH (pin 3). For typical curve for mute voltage dependence see Fig.12.
- The mono/stereo blend voltage is generated as a function of FM-IF₂ voltage, multi-path level, noise and position of TSWITCH.
- The high-cut control voltage is generated as a function of FM-IF₂ voltage, multi-path level, noise and position of TSWITCH.
- $f_{IF1} = 10.7 \text{ MHz}$; $f_{IF2} = 450 \text{ kHz}$ for AM mixer.
- The AM oscillator signal is generated by division of the 61.5 MHz crystal oscillator. Two divider ratios programmable by the I²C-bus: divide by 6 (AM-IF₁ = 10.7 MHz); divide by 2 (AM-IF₁ = 30 MHz).
- For typical AM level curve see Fig.15.
- For AM detector; $f_{AMIF2} = 450 \text{ kHz}$; $f_{mod} = 400 \text{ Hz}$; $m = 30\%$.

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STEREO DECODER CHARACTERISTICS

Input signal ($\Delta f = 75$ kHz) $V_{MPX(p-p)} = 1.7$ V; modulation frequency $f_{mod} = 1$ kHz; de-emphasis time constant $t = 50$ μ s; nominal input resistor (pin 45) $R_i = 168$ k Ω ; $T_{amb} = 25$ $^{\circ}$ C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{44-4(rms)}$; $V_{41-4(rms)}$	AF output voltage (RMS value)		800	900	1000	mV
V_{44-4} ; V_{41-4}	DC output voltage		3.1	3.6	4.1	V
$I_{44(max)}$; $I_{41(max)}$	maximum output current		150	—	—	μ A
V_{44-4}/V_{41-4}	difference of output voltage		−1	—	+1	dB
R_{044} ; R_{041}	output resistor		—	—	600	Ω
R_{Lmin}	minimum load resistor		12	—	—	k Ω
α_{cs}	channel separation (adjusted)		40	—	—	dB
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	$f = 20$ Hz to 15 kHz	74	80	—	dB
THD	total harmonic distortion		—	0.1	0.3	%
	MPX input overdrive margin	THD = 1%	4	—	—	dB
Carrier and harmonic suppression at the output; note 1						
α_{19}	pilot signal	$f = 19$ kHz	—	50	—	dB
α_{38}	subcarrier	$f = 38$ kHz	—	50	—	dB
α_{57}		$f = 57$ kHz	—	50	—	dB
α_{76}		$f = 76$ kHz	—	60	—	dB
α_2	intermodulation	$f_{mod} = 10$ kHz; $f_{spur} = 1$ kHz	—	60	—	dB
α_3		$f_{mod} = 13$ kHz; $f_{spur} = 1$ kHz	—	58	—	dB
α_{57}	traffic radio (ARI)	$f = 57$ kHz	—	70	—	dB
α_{67}	subsidiary communications authorization	$f = 67$ kHz	70	—	—	dB
α_{114}	adjacent channel frequency	$f = 114$ kHz	—	80	—	dB
α_{190}		$f = 190$ kHz	—	70	—	dB
RR	ripple rejection at output	$f_r = 100$ Hz; $V_r = 100$ mV _{eff}	—	30	—	dB
Mono/stereo control						
$V_{i(pil)}$	pilot threshold voltage	stereo on	—	24	30	mV
		mono on	8	20	—	mV
$\Delta V_{i(pil)}$	switch hysteresis $V_{i on}/V_{i off}$		—	2	—	dB
External mono/stereo control; note 2						
$V_{17} - 0.765V_{21}$	control voltage channel separation	see Fig.17	—	—	—	—
		$\alpha = 6$ dB	—	−110	—	mV
		$\alpha = 16$ dB	—	−40	—	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Muting functions (mute via I²C-bus)						
$\Delta V_{44}, \Delta V_{41}$	DC offset voltage	tune mute	-50	-	+50	mV
		radio mute (in combination with tune mute)	-400	-	+400	mV
α_{mute}	tune mute		60	-	-	dB
	radio mute (in combination with tune mute)		80	-	-	dB
High-cut control; see Fig.18						
$V_{18} - 0.765V_{21}$	control voltage	note 3				
		$t_{\text{de-emph}} = 50 \mu\text{s}$	0	-	-	mV
		$t_{\text{de-emph}} = 80 \mu\text{s}$	-300	-	-	mV
$t_{\text{de-emph}}$	control range of de-emphasis		50	-	80	μs
Voltage controlled oscillator; note 4						
f_{osc}	oscillator frequency range		225	228	231	kHz
Noise blanker						
INTERFERENCE DETECTION FULLY INTERNAL FROM LEVEL DETECTOR						
t_{sup}	interference suppression time		40	50	-	μs
TRIGGER THRESHOLD CONTROL						
$I_{51 \text{ charge}}$	charge current (into +4 V)		-	45	-	μA
$I_{51 \text{ discharge}}$	discharge current (from +8.5 V)		-	-900	-	μA
TRIGGER SENSITIVITY MEASUREMENT WITH PULSED MODULATION OF FM-IF ₂ ; see Figs 19 and 20						
$V_{37-35(p)}$	trigger sensitivity for test signal 1 (peak value)	$V_{38} = 2.52 \text{ V}$; note 5	-	-	0.8	mV
		$V_{38} = 2.52 \text{ V}$; note 6	100	-	-	mV
	trigger sensitivity for test signal 2 (peak value)	$V_{38} = 2.52 \text{ V}$; note 6	5.0	-	-	mV
		$V_{38} = 2.52 \text{ V}$; note 6	100	-	-	mV
V_{51}	trigger threshold variation with frequency modulation of FM-IF ₂ and $f_{\text{mod}} = 15 \text{ kHz}$ (pin 51)	$V_{37-35} = 100 \text{ mV}$; $\Delta f = 0 \text{ kHz}$	-	6.4	-	V
ΔV_{51}		$V_{37-35} = 100 \text{ mV}$; $\Delta f = 75 \text{ kHz}$	-	520	-	mV
I_{offset}	gate input offset current at pins 31 and 32 during suppression pulse duration		-	20	50	nA

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Notes to the stereo decoder characteristics

1. The following equations give the values for the carrier and harmonic suppression at the output:

$$\alpha_2 = \frac{V_0(\text{signal}) (\text{at } 1 \text{ kHz})}{V_0(\text{spurious}) (\text{at } 1 \text{ kHz})} f_s = (2 \times 10 \text{ kHz}) - 19 \text{ kHz}$$

$$\alpha_3 = \frac{V_0(\text{signal}) (\text{at } 1 \text{ kHz})}{V_0(\text{spurious}) (\text{at } 1 \text{ kHz})} f_s = (3 \times 13 \text{ kHz}) - 38 \text{ kHz}$$

$$\alpha_{57}(\text{ARI}) = \frac{V_0(\text{signal}) (\text{at } 1 \text{ kHz})}{V_0(\text{spurious}) (\text{at } 1 \text{ kHz} \pm 23 \text{ Hz})}$$

$$\alpha_{67} = \frac{V_0(\text{signal}) (\text{at } 1 \text{ kHz})}{V_0(\text{spurious}) (\text{at } 9 \text{ kHz})} f_s = (2 \times 38 \text{ kHz}) - 67 \text{ kHz}$$

$$\alpha_{114} = \frac{V_0(\text{signal}) (\text{at } 1 \text{ kHz})}{V_0(\text{spurious}) (\text{at } 4 \text{ kHz})} f_s = 110 \text{ kHz} - (3 \times 38 \text{ kHz})$$

$$\alpha_{190} = \frac{V_0(\text{signal}) (\text{at } 1 \text{ kHz})}{V_0(\text{spurious}) (\text{at } 4 \text{ kHz})} f_s = 186 \text{ kHz} - (5 \times 38 \text{ kHz})$$

2. The stereo decoder can be set to mono via the I²C-bus. Pilot presence indication via the I²C-bus.
3. The nominal de-emphasis value can be changed to 75 μs with C₃₁; C₃₂ = 10 nF.
4. The VCO is adjusted by means of a digital auxiliary PLL.
5. Noise blanker does not trigger.
6. Noise blanker triggers.

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CHARACTERISTICS FOR ANALOG-TO-DIGITAL CONVERTERS (ADCs) FOR LEVEL AND MULTI-PATH VOLTAGES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADC for FM level information; note 1						
ΔV_{37-35}	analog-to-digital conversion step size		2	4	8	dB/step
ΔV_{37-35}	analog-to-digital conversion level range		43	56	69	dB
FM STOP						
ΔV_{stop}	variation of stop level as function of V_{42-4}		—	16	—	dB/V
ADC for AM level information; note 2						
ΔV_{33-34}	analog-to-digital conversion step size		2	4	8	dB/step
ΔV_{33-34}	analog-to-digital conversion level range		43	56	69	dB
AM STOP						
ΔV_{stop}	variation of stop level as function of V_{43-4}		—	16	—	dB/V
ADC for multi-path information; note 3						
m	multi-path conversion	step 0	—	—	5	%
		step 1	—	15	—	%
		step 2	—	22	—	%
		step 3	—	28	—	%
		step 4	—	34	—	%
		step 5	—	40	—	%
		step 6	—	46	—	%
		step 7	—	52	60	%

Notes

1. The FM level information V_{50-3} is analog-to-digital converted with 4 bits.
2. The AM level information V_{49-4} is analog-to-digital converted with 4 bits.
3. The multi-path information V_{40-4} is analog-to-digital converted with 3 bits covering an IF_2 amplitude modulation range $m \leq 0.6$; $f_{\text{mod}} = 20 \text{ kHz}$.

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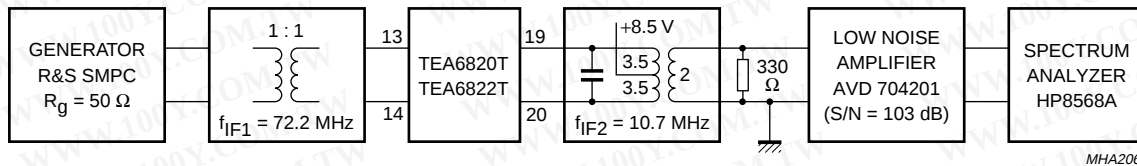


Fig.4 Test circuit FM mixer.

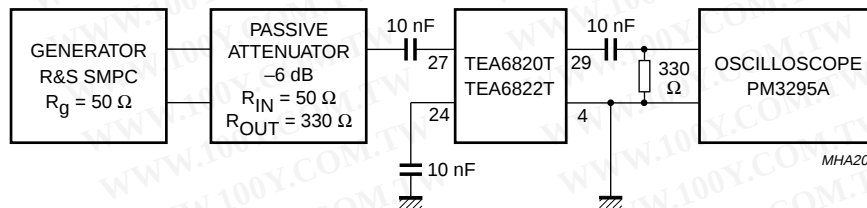


Fig.5 Test circuit IF-amplifier.

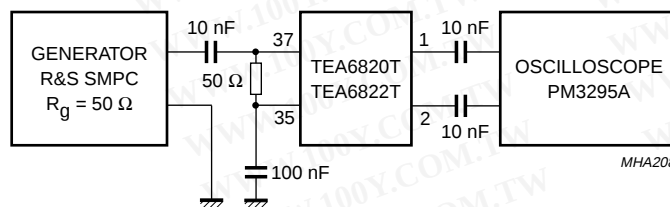
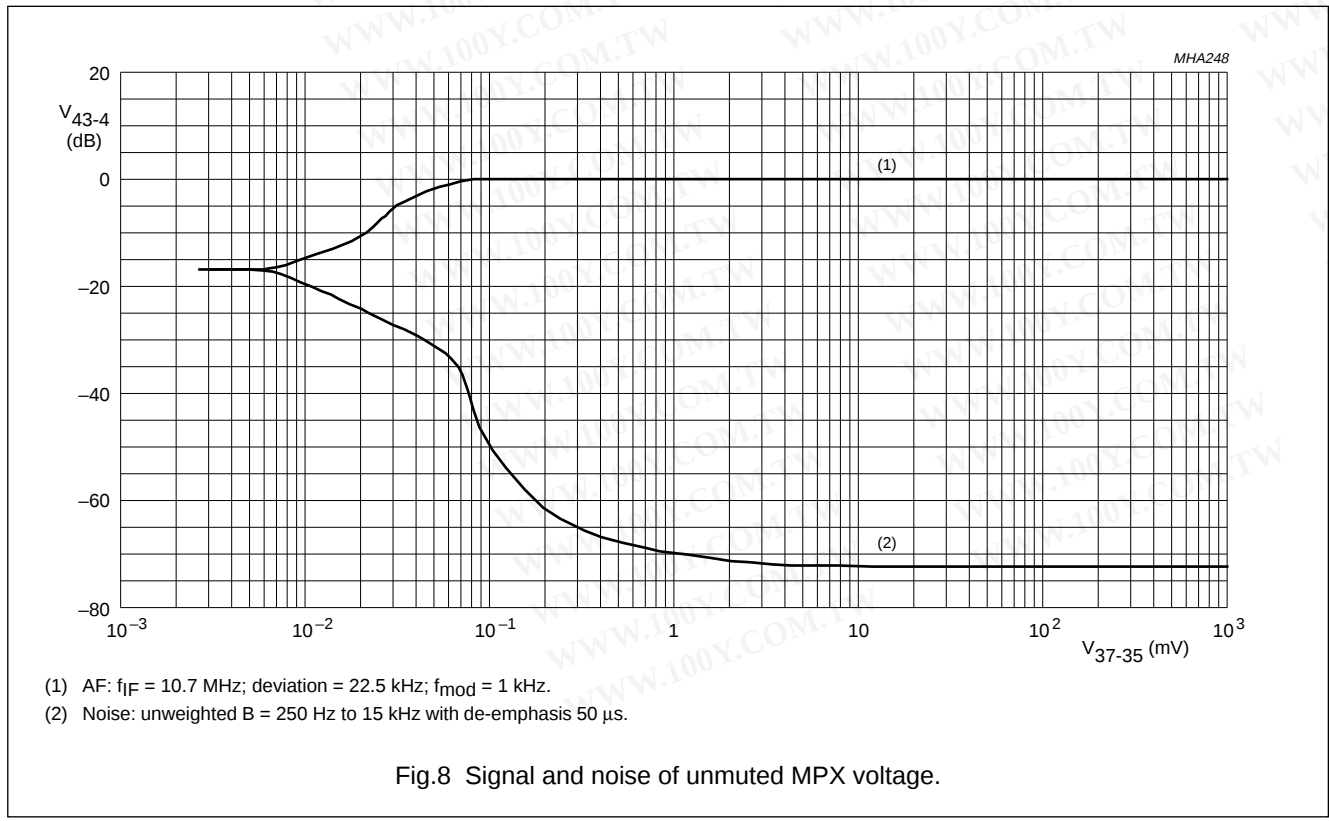
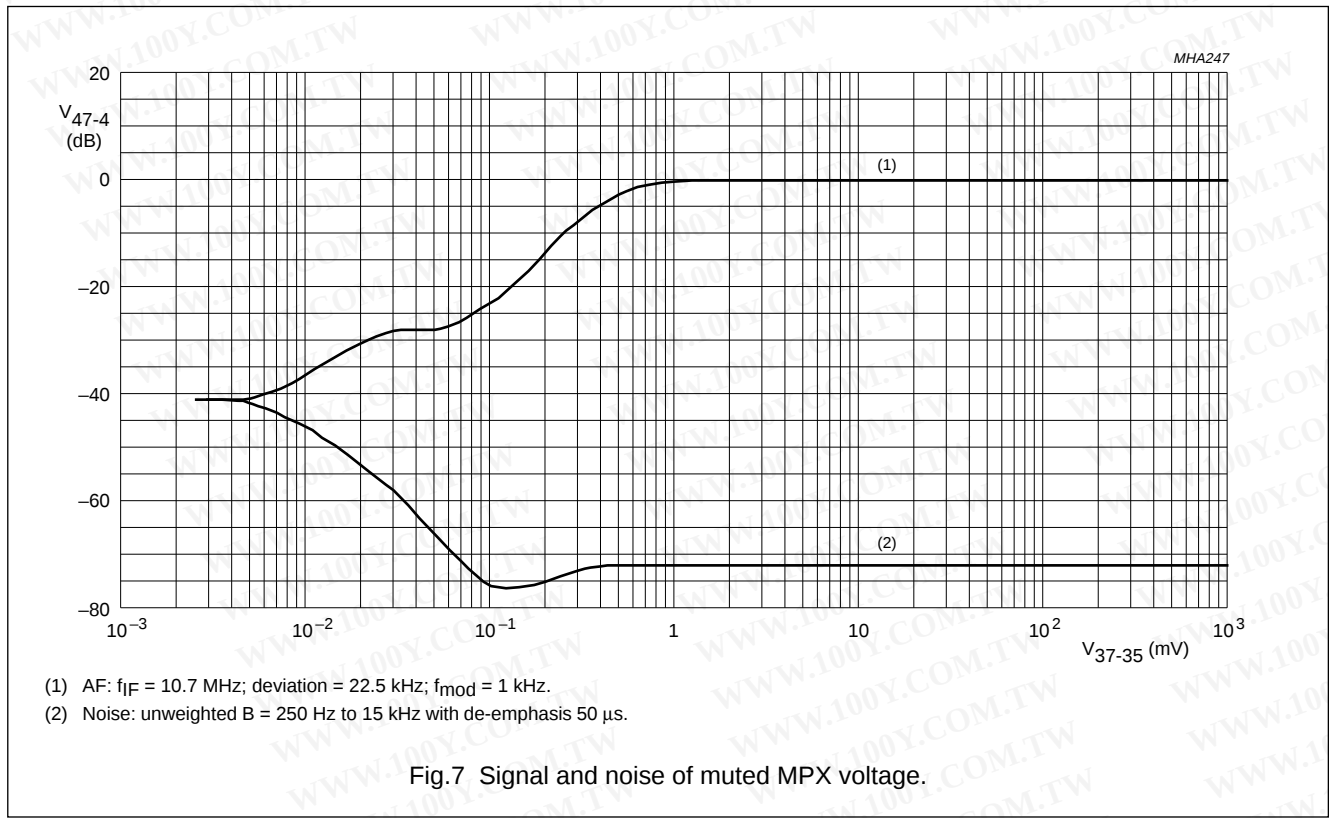


Fig.6 Test circuit limiter gain.

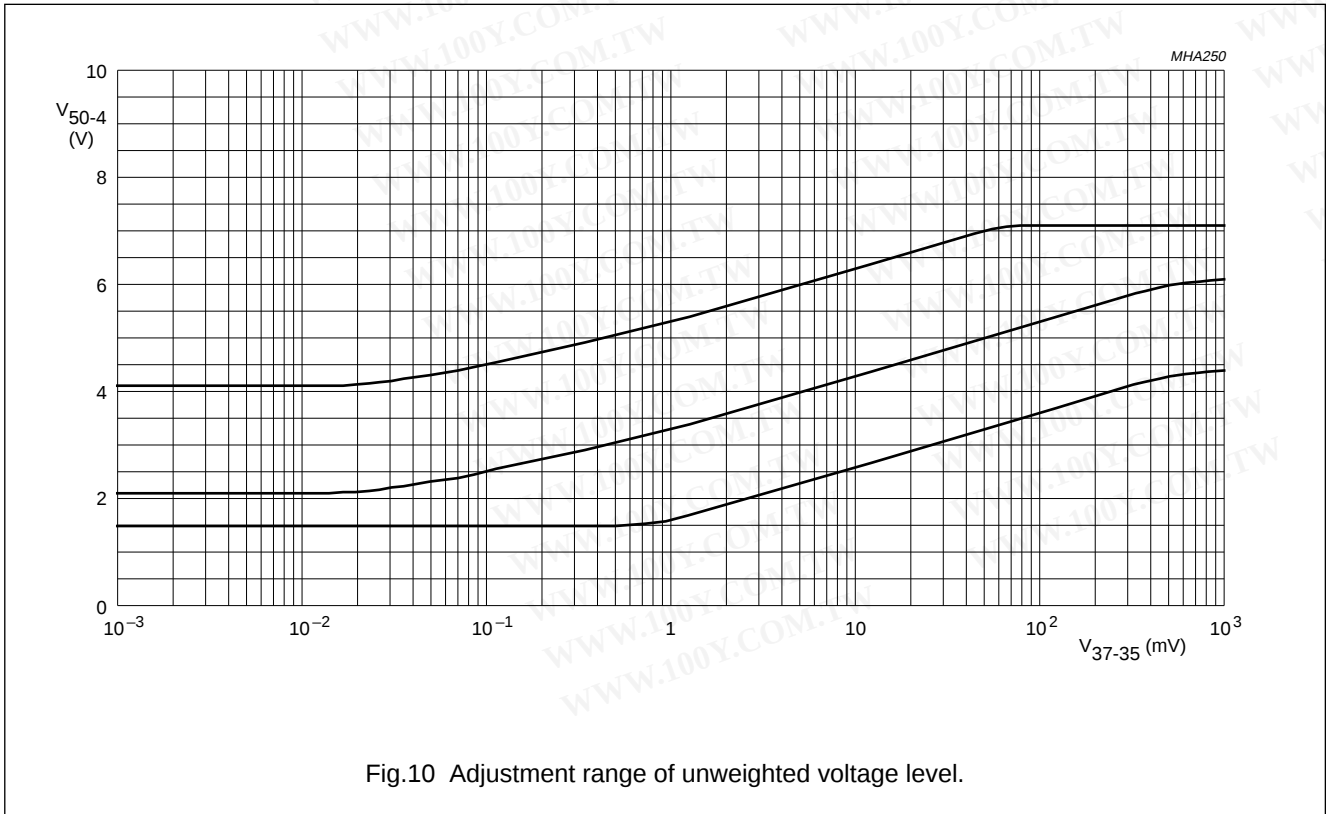
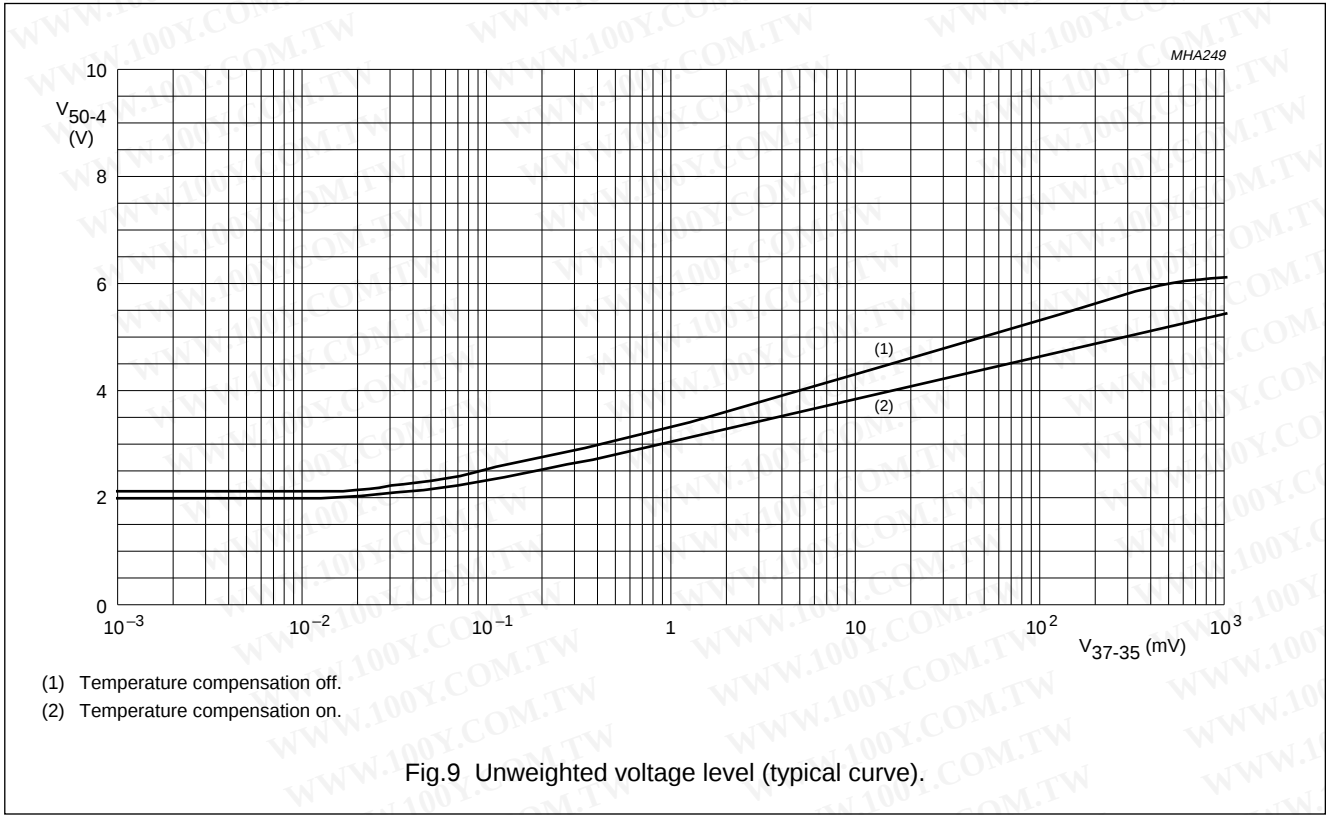
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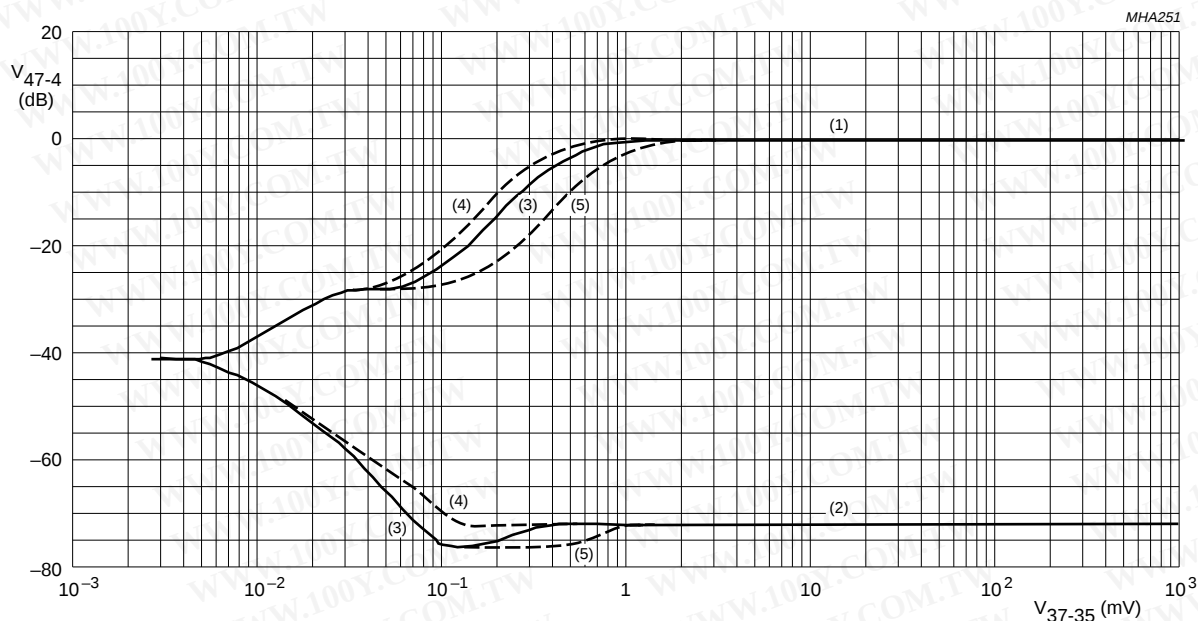
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- (1) AF: $f_{IF} = 10.7$ MHz; deviation = 22.5 kHz; $f_{mod} = 1$ kHz.
- (2) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50 μ s.
- (3) Level adjustment set to α_3 dB at 0.6 mV.
- (4) Level adjustment set to α_3 dB at 0.4 mV.
- (5) Level adjustment set to α_3 dB at 1 mV.

Fig.11 Muting dependence of unweighted voltage level (typical curve).

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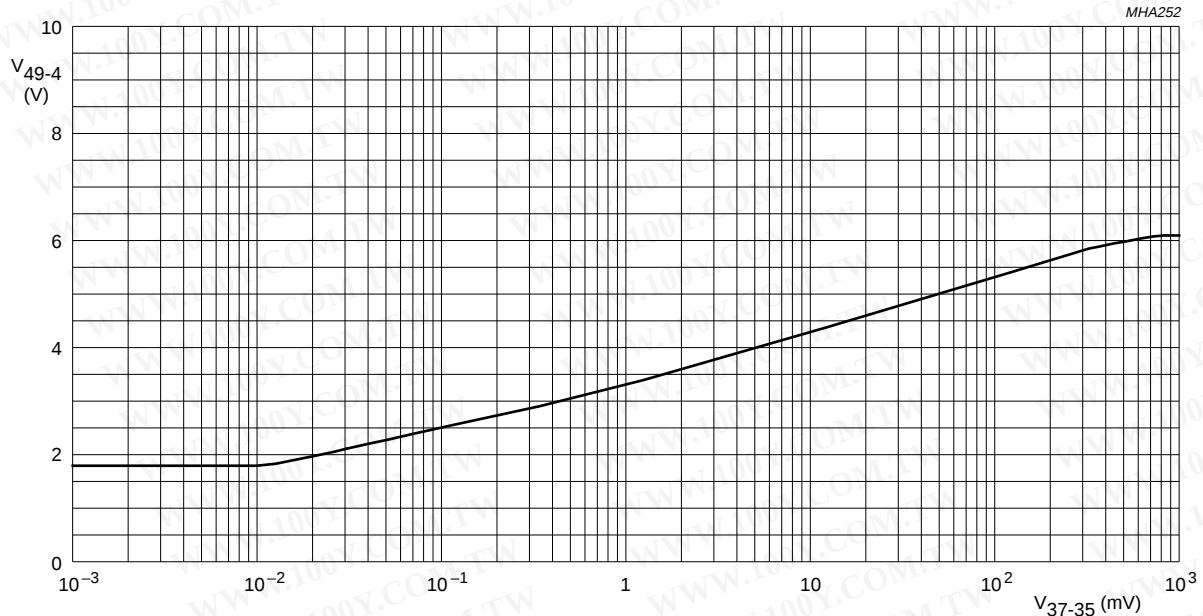
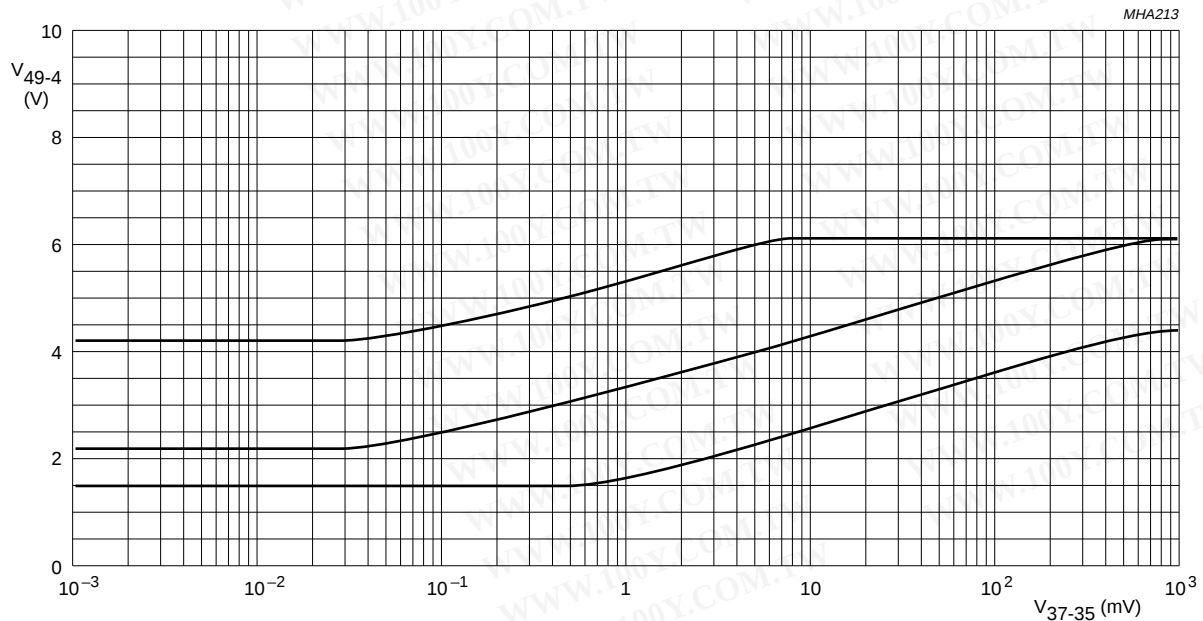
Fig.12 Typical mute voltage as function of FM-IF₂ voltage.

Fig.13 Adjustment range mute voltage.

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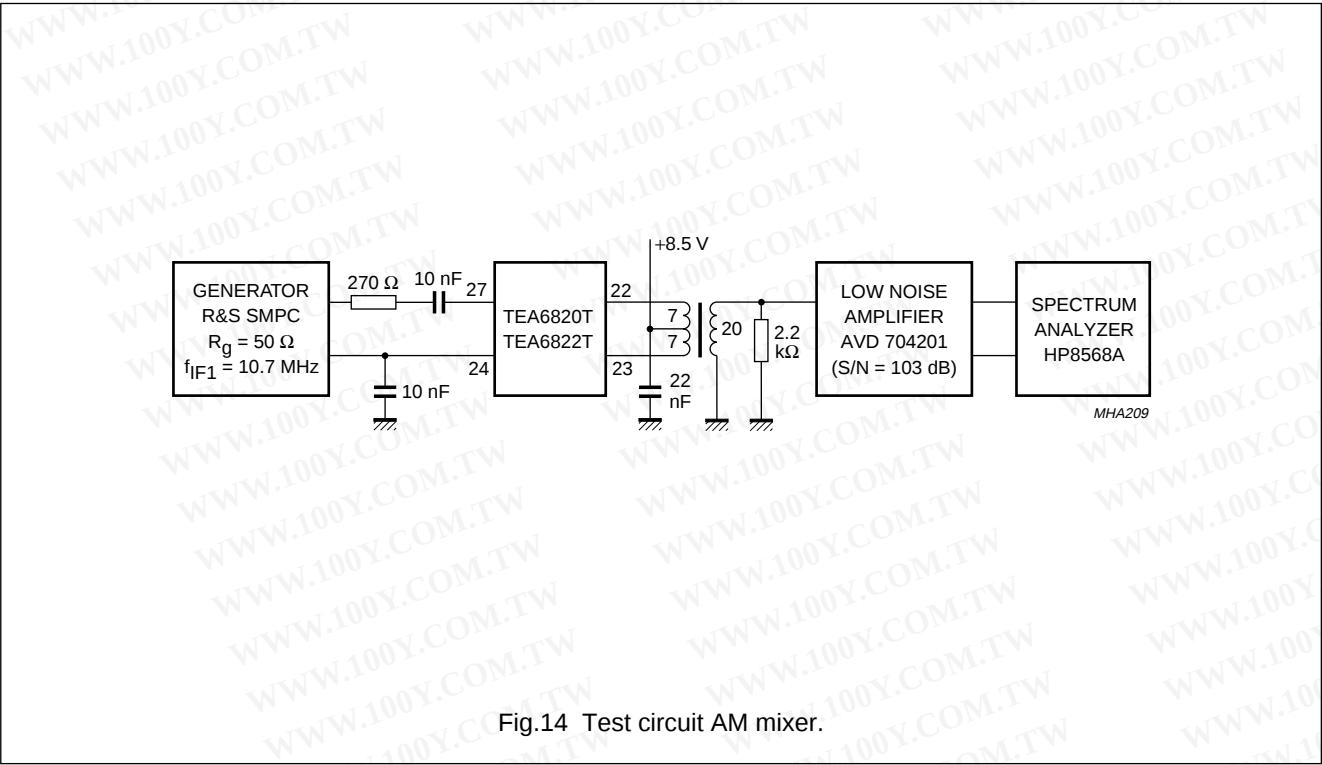


Fig.14 Test circuit AM mixer.

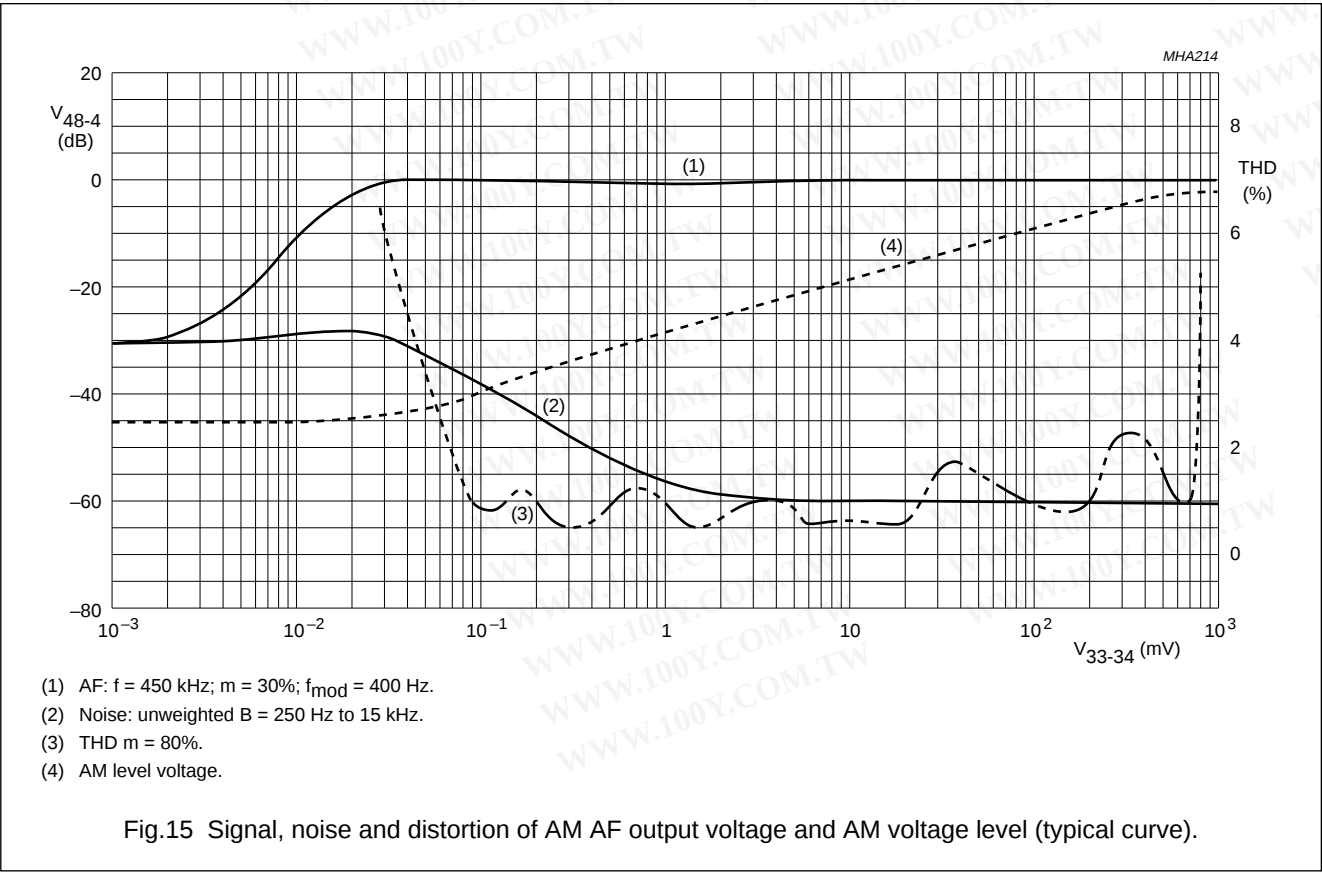
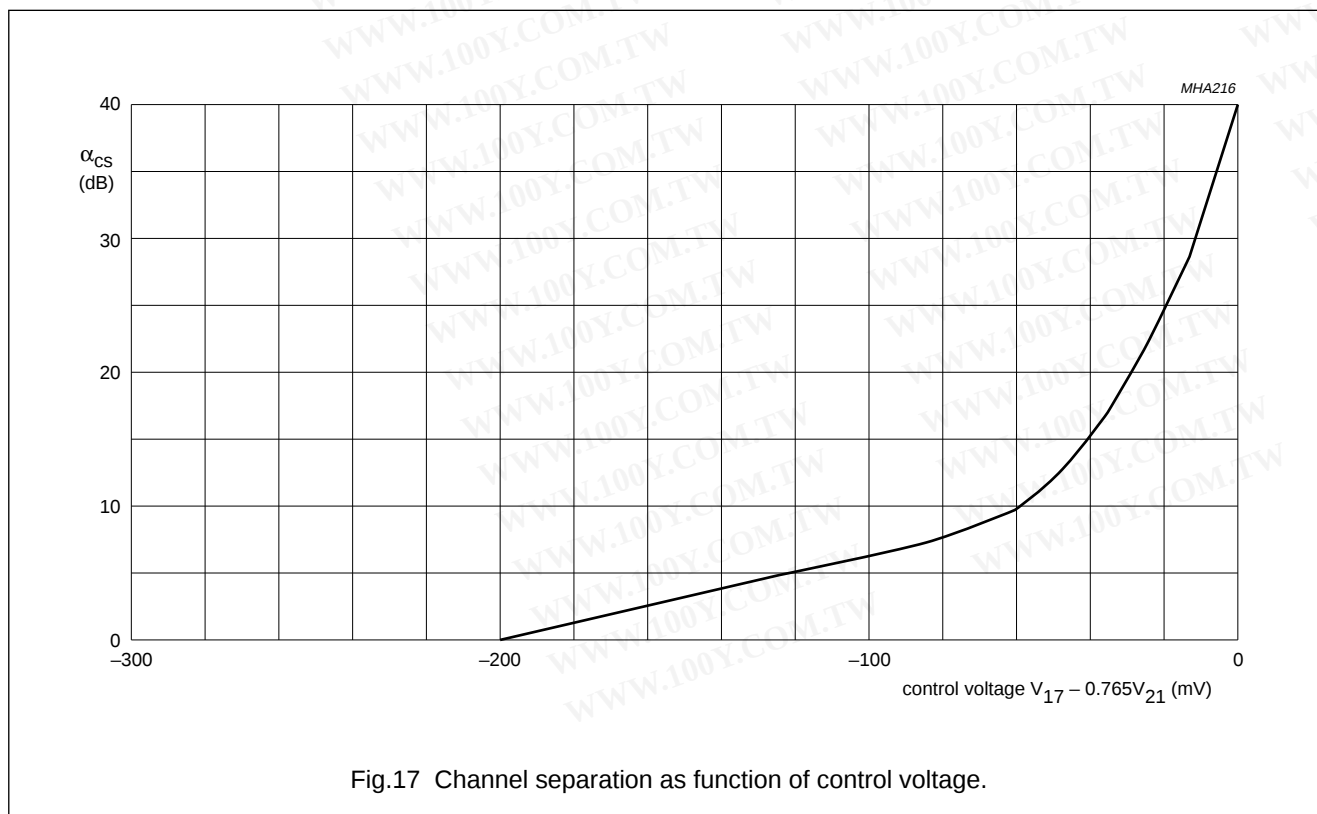
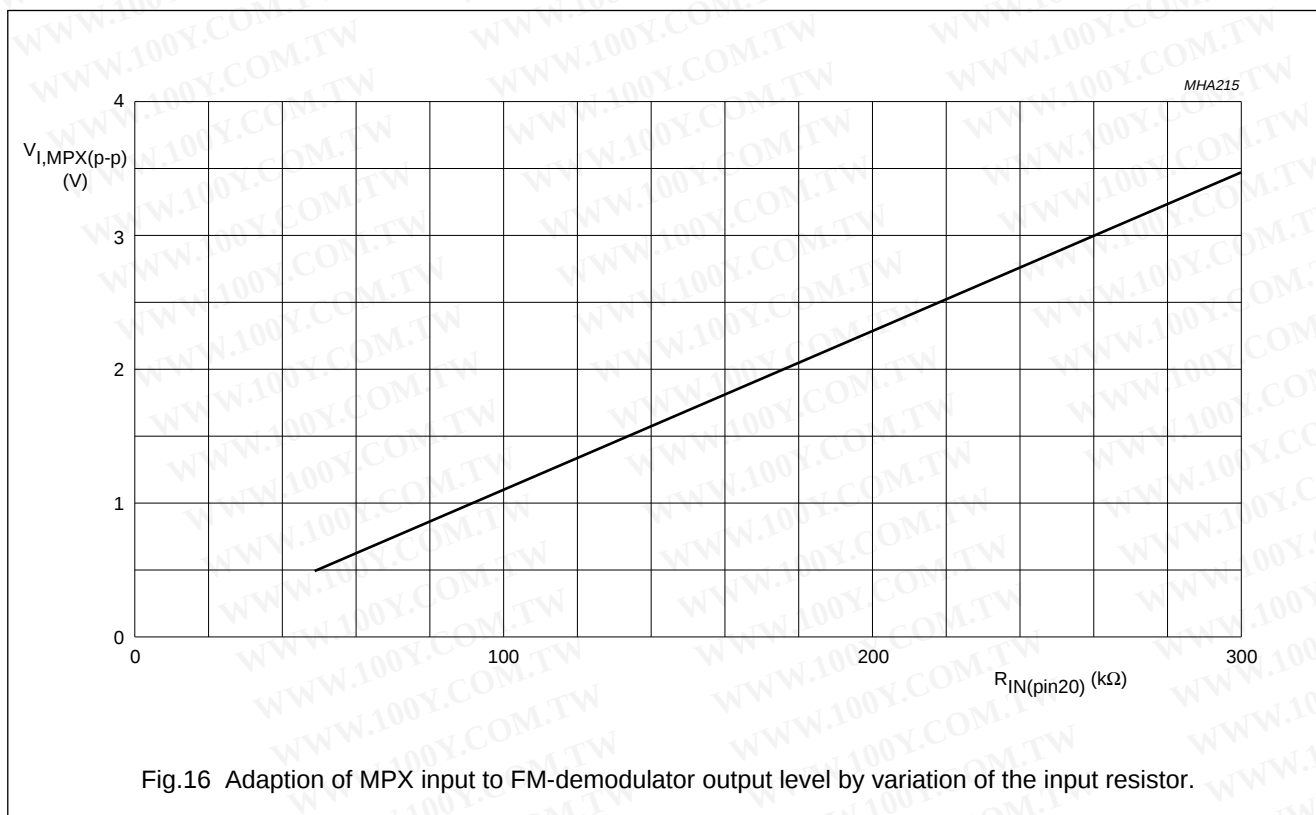


Fig.15 Signal, noise and distortion of AM AF output voltage and AM voltage level (typical curve).

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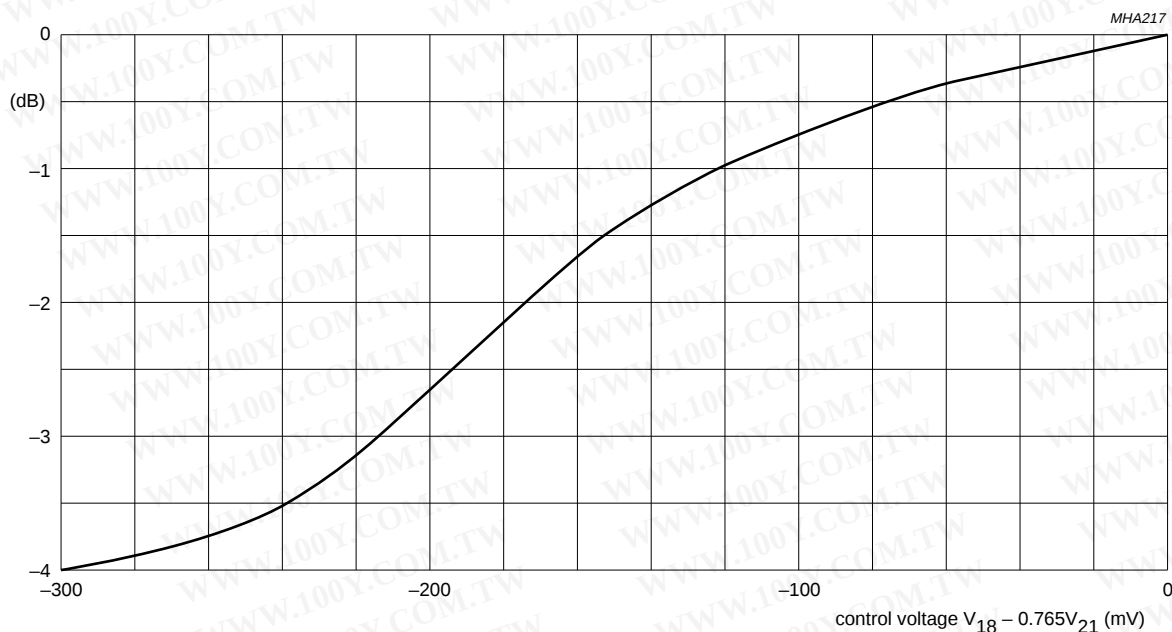


Fig.18 High-cut with $f_{\text{mod}} = 10$ kHz as function of control voltage.

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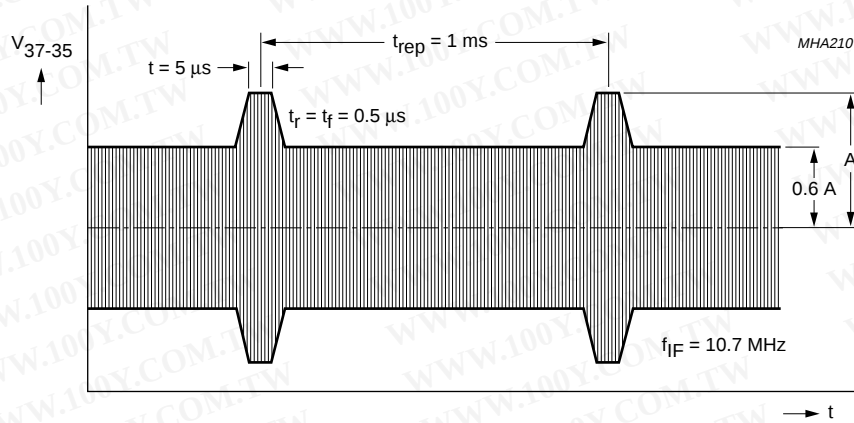


Fig.19 Test signal 1 for interference detection from level detector.

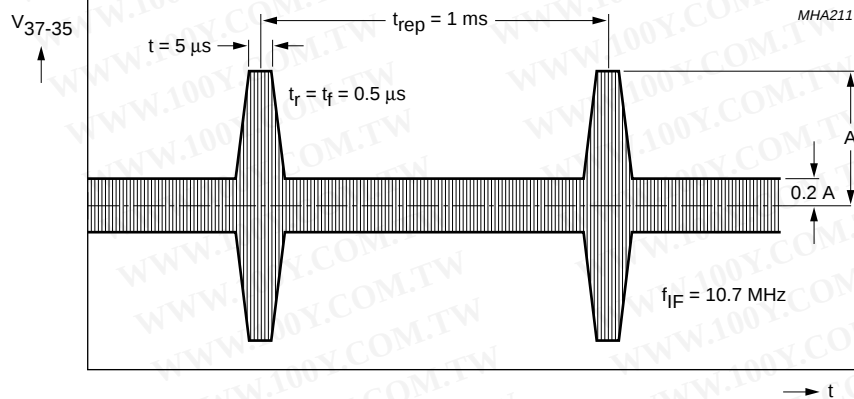


Fig.20 Test signal 2 for interference detection from level detector.

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I²C-BUS AND I²C-BUS CONTROLLED FUNCTIONS

I²C-bus specification

The standard I²C-bus specification is expanded by the following definitions.

Structure of the I²C-bus logic: slave transceiver with auto increment and expansion to switch a direct transfer of all transmissions to an output for the radio front-end IC (TEA6810T respectively TEA6811T).

Subaddresses are not used.

DATA TRANSFER FOR THE TEA6820T AND THE TEA6822T

Data sequence:

- Address
- Byte 1
- Byte 2.

The data transfer maybe in this order only. The transfer direction of the data bytes is defined by the LSB of the address.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte was not completed, this byte is lost and the previous information is available.

DATA TRANSFER TO AN OUTPUT OF THE FRONT-END IC

A data bit in the transceiver of the TEA6820T or TEA6822T enables or disables a direct transfer of all transmissions to an interface stage for the front-end IC.

For a transmission to the front-end IC the address and the data format of the front-end IC has to be used.

Remark: the pull-up resistors for the front-end interface (pins 6 and 7) should not be connected to the 5 V supply voltage of the front-end IC, otherwise a bus pull-down (pin 53) can occur during switching off the front-end supply when the interface stage is enabled.

DATA TRANSFER TO THE IF IC

Data transfer to the IF IC (TEA6820T or TEA6822T) is independent of the state of interface stage for the front-end IC.

Table 1 Structure of the I²C-bus

DESCRIPTION	SPECIFICATION
Bus address of the TEA6820T and the TEA6822T	1100001X
Subaddress	not used
Hardware (pin) programmable address bits	not available
Default settings by power-on reset	data byte 1 bits 4 to 7 are set to logic '0'; all other bits are random

Table 2 Data to be received by the IC for data byte 1

BIT	DESCRIPTION	RESULT
0	switch for mono	bit 0 = 1
	switch for stereo	bit 0 = 0
1	LSB reference frequency for synthesizer	
2	reference frequency for synthesizer	
3	MSB reference frequency for synthesizer	
4	tuning mute off	bit 4 = 1
	tuning mute on	bit 4 = 0
5	SDS/SDR hold off	bit 5 = 1
	SDS/SDR hold on	bit 5 = 0
6	radio mute off	bit 6 = 1
	radio mute on	bit 6 = 0
7	I ² C-bus to front-end ENABLED	bit 7 = 1
	I ² C-bus to front-end DISABLED	bit 7 = 0

Table 3 Reference frequency setting in data byte 1; see Table 1

BIT 3	BIT 2	BIT 1	FREQUENCY SETTING
0	0	0	3 kHz
0	0	1	5 kHz
0	1	0	10 kHz
0	1	1	15 kHz
1	0	0	25 kHz
1	0	1	50 kHz
1	1	0	not defined
1	1	1	not defined

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Table 4 Data to be received by the IC for data byte 2

BIT	DESCRIPTION	RESULT
0	AM/FM; AM mode	bit 0 = 0
	AM/FM; FM mode	bit 0 = 1
1	divider for AM mixer; divide by 2	bit 1 = 0
	divider for AM mixer; divide by 6	bit 1 = 1
2	measure time IF-count; 40 ms	bit 2 = 0
	measure time IF-count; 4 ms	bit 2 = 1
3	SDR off	bit 3 = 0
	SDR on	bit 3 = 1
4	IF-prescaler division rate; divide by 200	bit 4 = 0
	IF-prescaler division rate; divide by 25	bit 4 = 1
5	sensitivity unchanged	bit 5 = 0
	multi-path sensitivity switch; less sensitivity by an offset of $\Delta m = 10\%$	bit 5 = 1
6	temperature compensation of unweighted voltage level; temperature coefficient as specified in Chapter "Characteristics"	
	temperature compensation off	bit 6 = 0
	temperature compensation on	bit 6 = 1
7	not used	

Table 5 Data to be transmitted by the IC for data byte 1; note 1

BIT	DESCRIPTION
0	bit 1 level information
1	bit 2 level information
2	MSB (bit 3) level information
3	LSB multi-path information
4	multi-path information
5	MSB multi-path information
6	stereo pilot presence; bit 6 = 1
7	LSB (bit 0) level information

Note

- The analog-to-digital conversion for multi-path and level will be done during a transmission of any address to the I²C-bus.

Table 6 Data to be transmitted by the IC for data byte 2

BIT	DESCRIPTION
0	LSB of the IF-counter
1	IF-counter
2	IF-counter
3	IF-counter
4	IF-counter
5	IF-counter
6	IF-counter
7	MSB of the IF-counter

REFERENCED FREQUENCY GENERATION

Table 7 Division ratios

DIVISION RATIO	REFERENCE FREQUENCY (kHz) ⁽¹⁾
20500	3
12300	5
6150	10
4100	15
2460	25
1230	50

Note

- All specified frequencies are valid for a crystal oscillator frequency of 61.5 MHz.

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Table 8 Output signal of reference frequency divider

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{10-11(p-p)}$	differential output voltage (peak-to-peak value)	0.3	0.4	0.5	V
$V_{10-4(p-p)}$; $V_{11-4(p-p)}$	single-ended output voltage (peak-to-peak value)	0.15	0.2	0.3	V
C_{10-4} ; C_{11-4}	output capacitance	–	–	4	pF
R_{10-52} ; R_{11-52}	output resistance	800	1000	1200	Ω

IF COUNTER

Table 9 IF counter sensitivity

SYMBOL	PARAMETER	CONDITIONS	MIN.	UNIT
V_{33-34}	IF counter sensitivity	AM mode; $m = 0$	200	μV
V_{37-35}	IF counter sensitivity	FM mode	200	μV

AM counting windows are 4 or 40 ms. FM counting windows are 4 or 40 ms. AM counting resolution is 250 or 25 Hz. FM counting resolution is 5 kHz, 625 Hz, 50 kHz or 6.25 kHz. AM IF-prescaler is divisible by 1. FM IF-prescaler is divisible by 25 or 200.

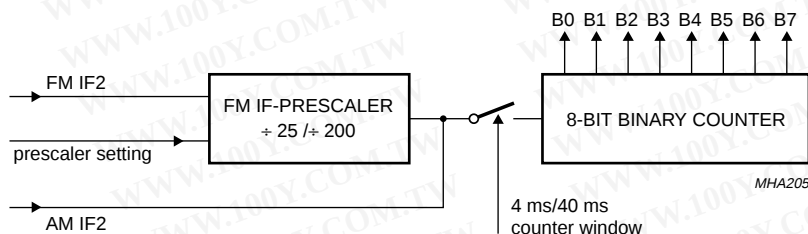


Fig.21 IF counter structure.

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IF counter read out

IF counter read out as a function of FM or AM position, counter window and prescaler setting

FM/AM	PRESCALER RATIO	WINDOW (ms)	f_{IF} (kHz)	READ OUT	RESOLUTION (Hz/count)	RANGE (kHz)	
						MIN.	MAX.
FM	200	4	10700	D6H	50000	4300	17050
FM	200	40	10700	5CH	5000	10065	11335
FM	25	4	10700	B0H	6250	9906.25	11493.75
FM ⁽¹⁾	25	40	10700	E0H	625	10620.63	10779.38
AM	1	4	450	08H	250	418.25	481.75
AM ⁽¹⁾	1	40	450	50H	25	446.83	453.18

Note

1. In position FM with a prescaler ratio of 25, counter window of 40 ms and in position AM with 40 ms counter window ambiguous counting results within the IF filter bandwidth are obtained. The counting range is 127 counts above and 127 counts below the nominal IF of 10.7 MHz for FM and 450 kHz for AM.

The IF count windows are valid for a crystal oscillator frequency of 61.5 MHz.

The FM/AM switching is carried out by bit 0 of byte 2 of the received data of the IC.

The IF counter operates continuously.

The IF counter and window-counter will be reset when the I²C-bus logic detects the address of the IC. This disables changes in the latches for the IF count, while reading this value. If the transmission to the front-end IC is disabled after the synthesizer loop of the TEA6810T/TEA6811T front-end IC has locked for a new frequency, the IF-count will be available after the set measuring time.

The IF counter starts at 0. The IF counter output are the **8 least significant bits** of the counting result.

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INTERNAL CIRCUITRY

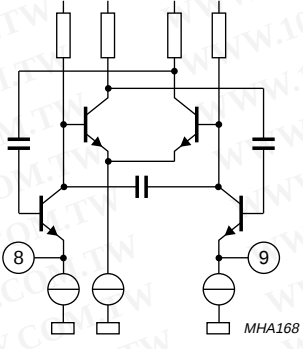
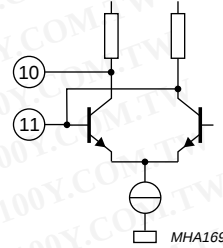
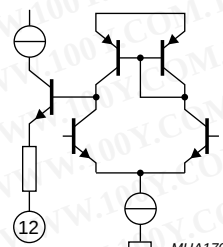
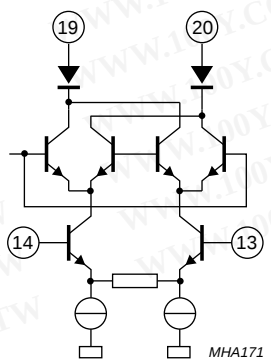
Table 10 Equivalent pin circuits and pin voltages

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
1	QDET1	4.0	4.0	
2	QDET2	4.0	4.0	
3	TSWITCH	open	0.4 to 0.6	
4	AGND	—	—	
5	V _{DDA1}	5.0	5.0	
6	HFBUS1	5.0	5.0	
7	HFBUS2	5.0	5.0	

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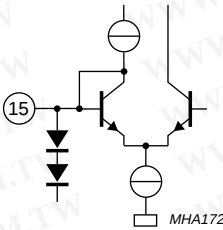
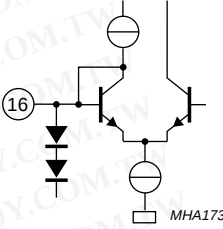
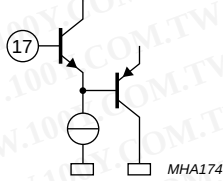
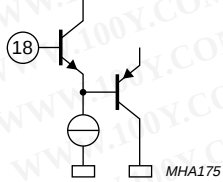
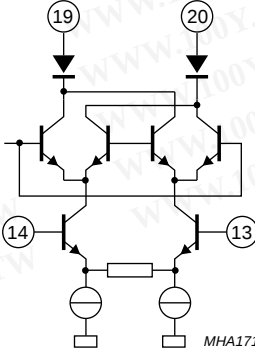
TEA6820T; TEA6822T

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
8	XTAL1	4.1	4.1	
9	XTAL2	4.1	4.1	
10	$f_{ref(p)}$	4.9	4.9	
11	$f_{ref(n)}$	4.9	4.9	
12	I_{ref}	4.3	4.3	
13	FMIF1IN1	2.3	2.3	
14	FMIF1IN2	2.3	2.3	

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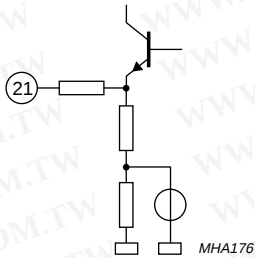
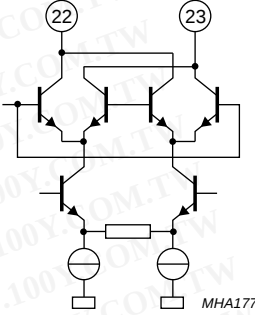
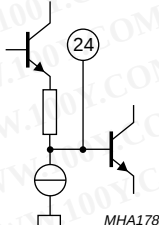
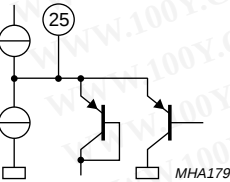
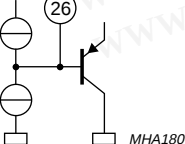
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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
15	TSDR	0.7 to 5.5	0.7 to 5.5	
16	TSDS	0.7 to 5.5	0.7 to 5.5	
17	V _{SDS}	3.0 to 5.5	3.0 to 5.5	
18	V _{SDR}	3.0 to 5.5	3.0 to 5.5	
19	FMIF2OUT1	8.5	8.5	
20	FMIF2OUT2	8.5	8.5	

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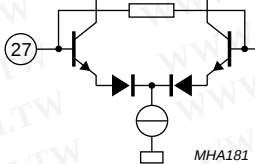
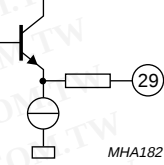
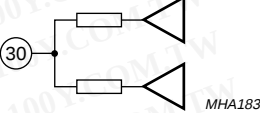
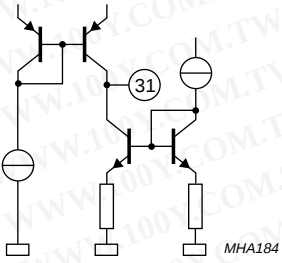
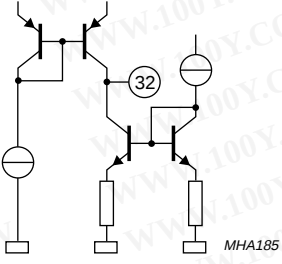
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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
21	V_{ref}	5.1	5.1	 MHA176
22	AMIF2OUT1	8.5	8.5	 MHA177
23	AMIF2OUT2	8.5	8.5	
24	FMAMDEC	3.0	2.5	 MHA178
25	PHASEDET	2.8 to 7.0	2.8 to 7.2	 MHA179
26	PILDET	0.4	0.4 to 7.0	 MHA180

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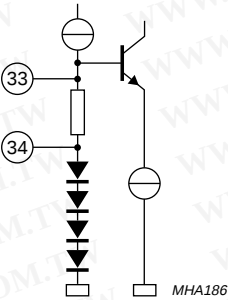
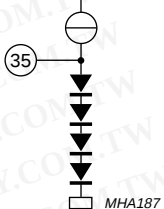
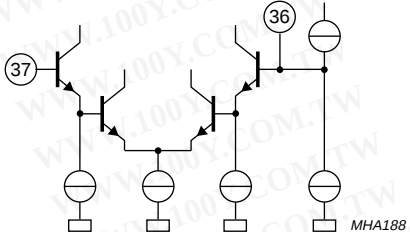
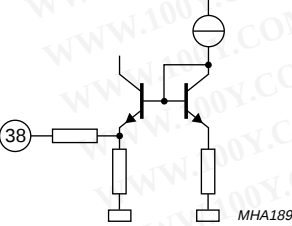
TEA6820T; TEA6822T

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
27	FMAM10.7	3.0	2.5	
28	V _{DDA2}	8.5	8.5	
29	FMIFAMPOUT	6.0	6.0	
30	AFGND	3.6	3.6	
31	DEEMPHR	2.3	2.3	
32	DEEMPHL	2.3	2.3	

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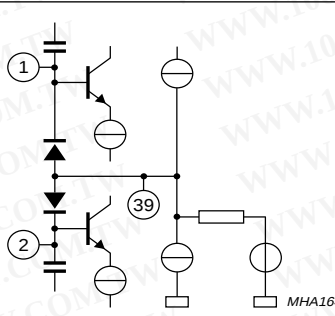
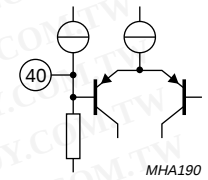
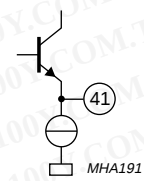
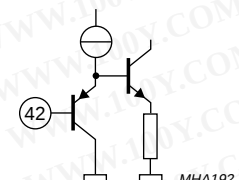
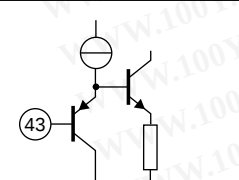
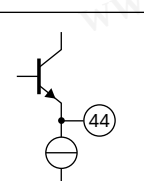
TEA6820T; TEA6822T

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
33	AMIF2IN1	2.7	0.7	
34	AMIF2IN2	2.7	0.7	
35	FMIN2	0.7	2.7	
36	DCFEED	2.7	2.7	
37	FMIN1	0.7	2.7	
38	LEVELADJ	2.6	2.6	

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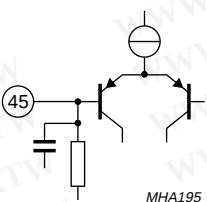
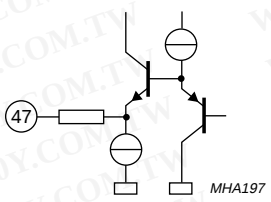
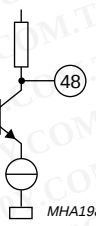
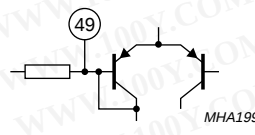
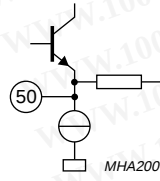
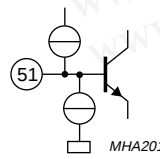
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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
39	C _{AFC}	1.0 to 2.2	1.0 to 7.0	
40	MPBUF	0.7 to 6.0	0.7 to 6.0	
41	OUTLEFT	3.6	3.6	
42	FMSTOP	0 to 5.2	0 to 5.2	
43	RDS/AMSTOP	0 to 5.2	3.0	
44	OUTRIGHT	3.6	3.6	

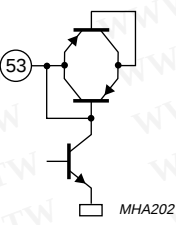
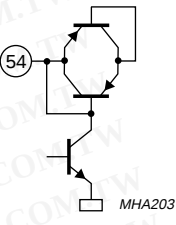
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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
45	MPXIN	2.8	2.8	 MHA195
46	i.c.	—	—	
47	MPXOUT	0	3.0	 MHA197
48	AMAFOUT	3.7	4.8	 MHA198
49	V _{mute} /AML	1.0 to 5.5	1.0 to 5.5	 MHA199
50	LEVELUNWEIG	1.0 to 7.0	1.0 to 7.0	 MHA200
51	IAC _{CONTR}	0	6.0	 MHA201
52	V _{DDD}	5.0	5.0	

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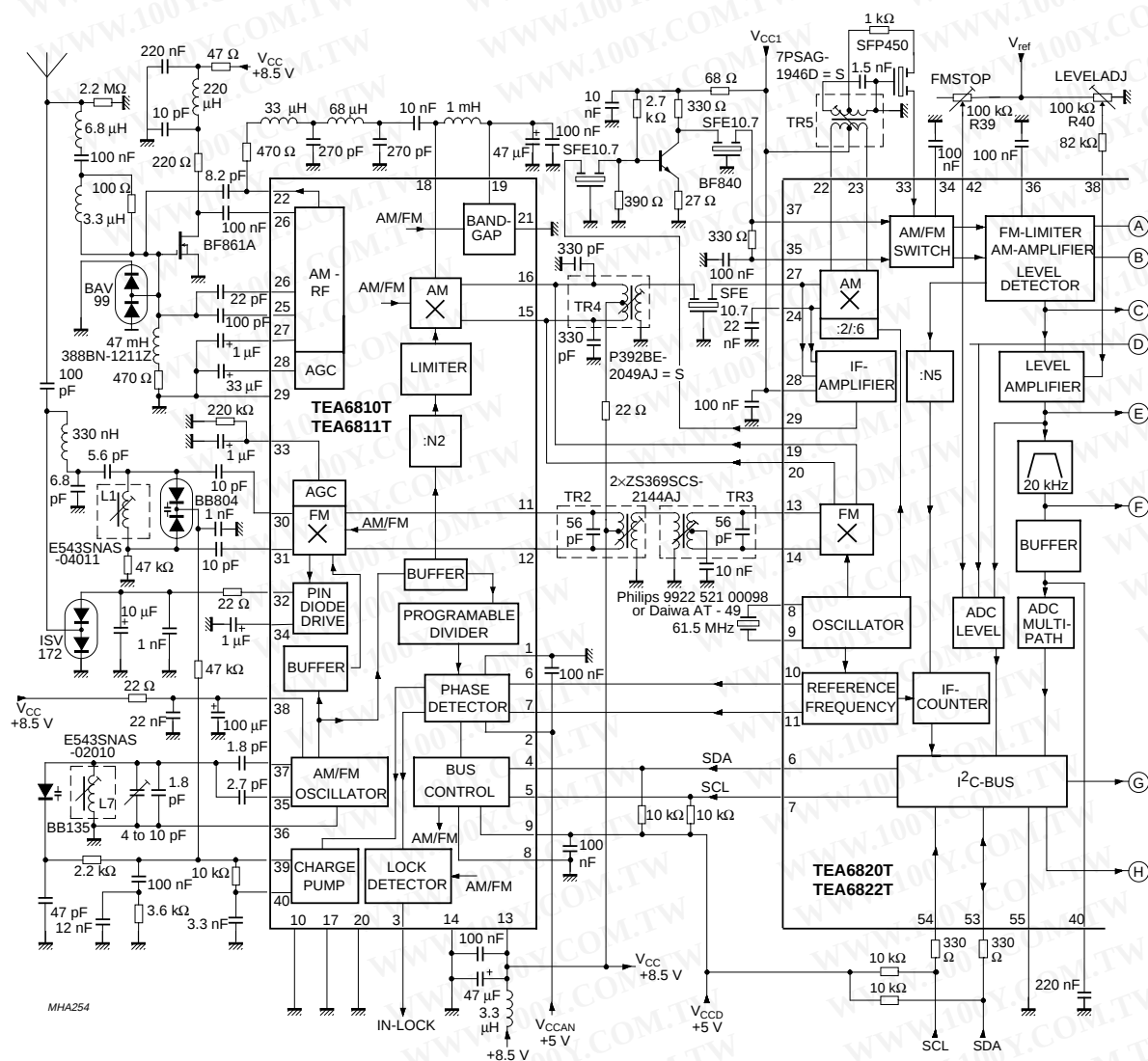
PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
53	SDA	5.0	5.0	
54	SCL	5.0	5.0	
55	DGND	0	0	
56	V _{DDA3}	8.5	8.5	

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TEA6820T; TEA6822T

APPLICATION INFORMATION



Time constant control: slow or fast attack and decay time constants for soft mute, mono/stereo and high-cut control can be chosen by connecting pin 3 to GND or pin 21.

Fig.22 ICE application diagram (continued in Fig.23).

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TEA6820T; TEA6822T

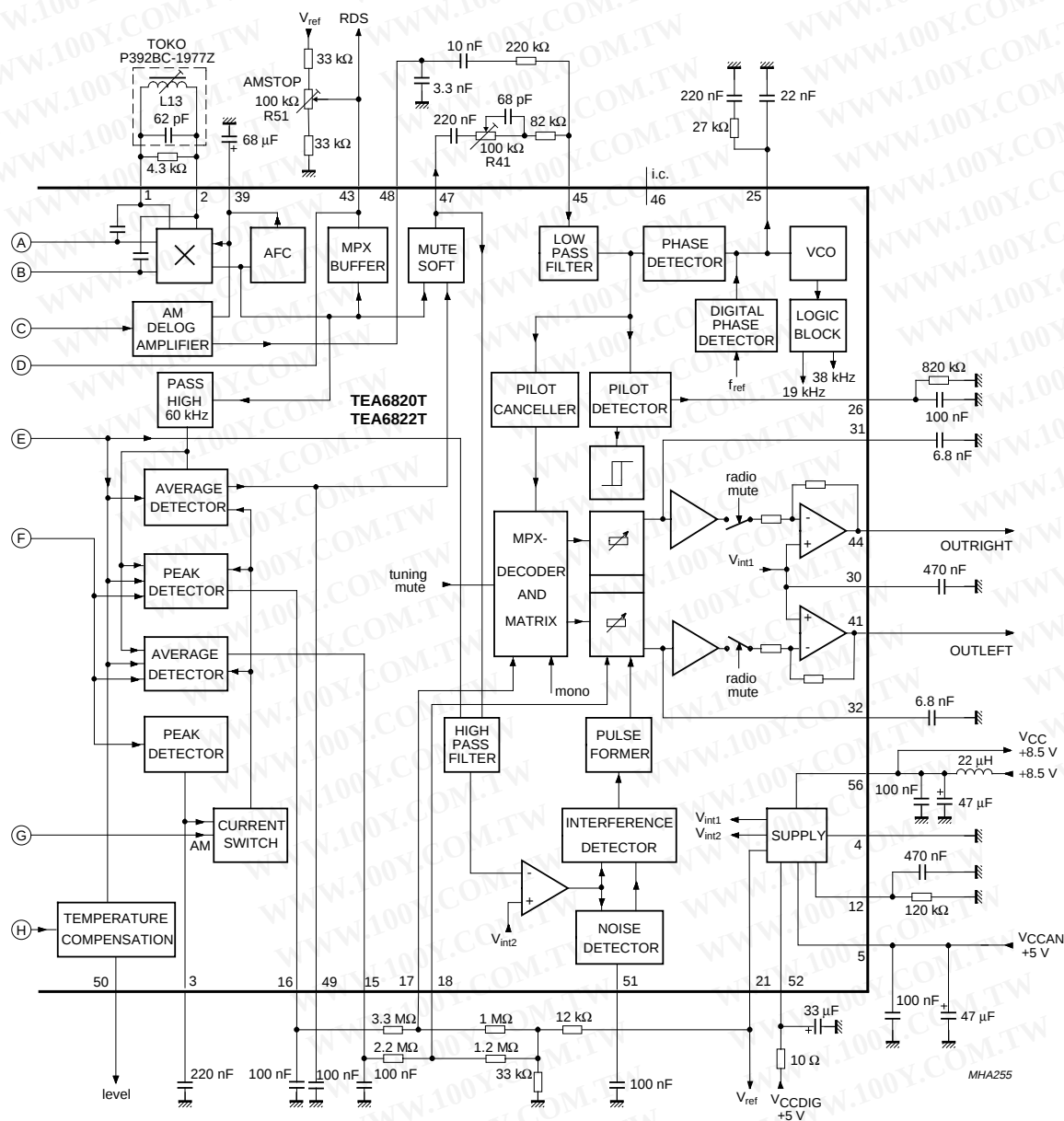


Fig.23 ICE application diagram (continued from Fig.22).

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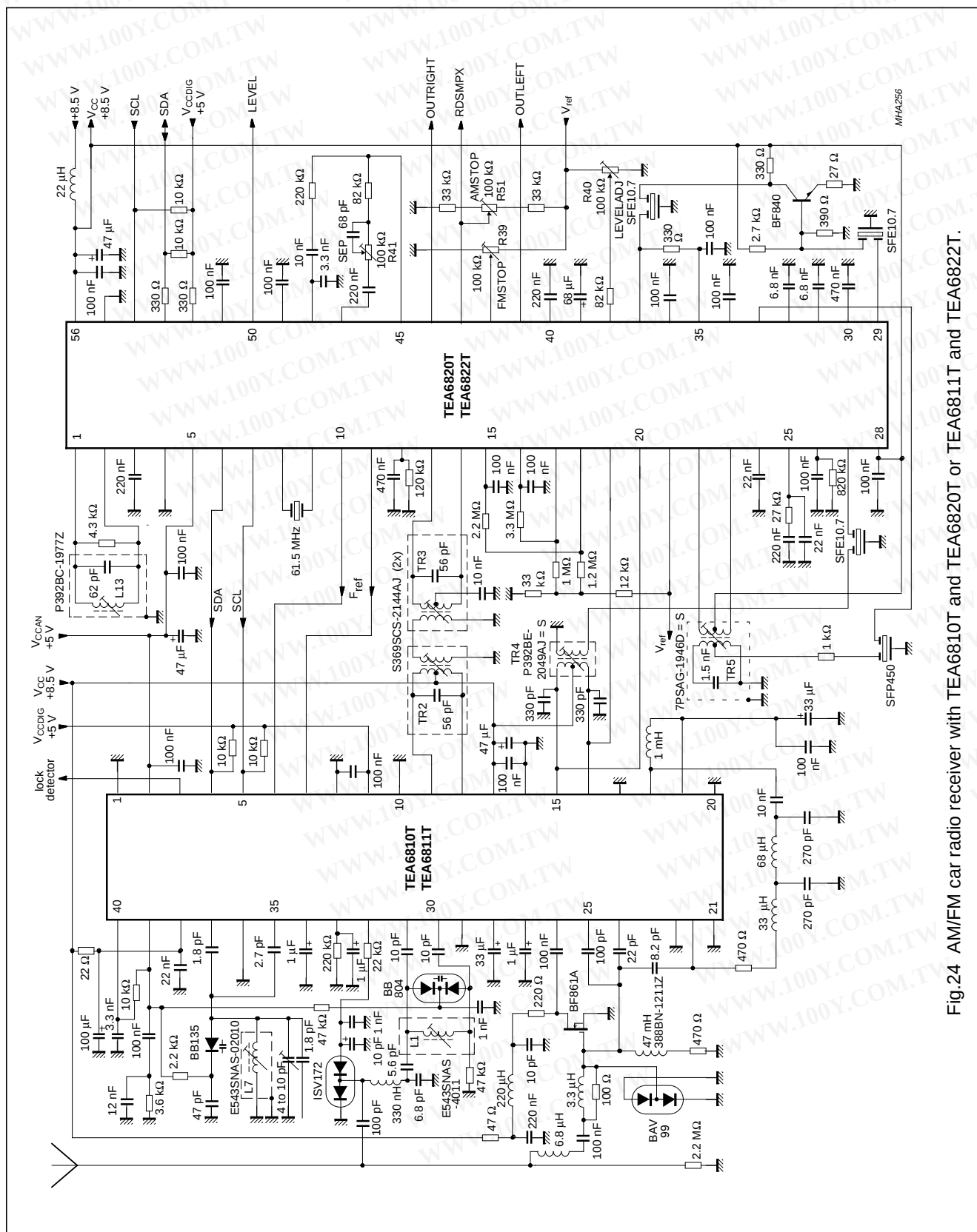


Fig.24 AM/FM car radio receiver with TEA6810T and TEA6820T or TEA6822T.

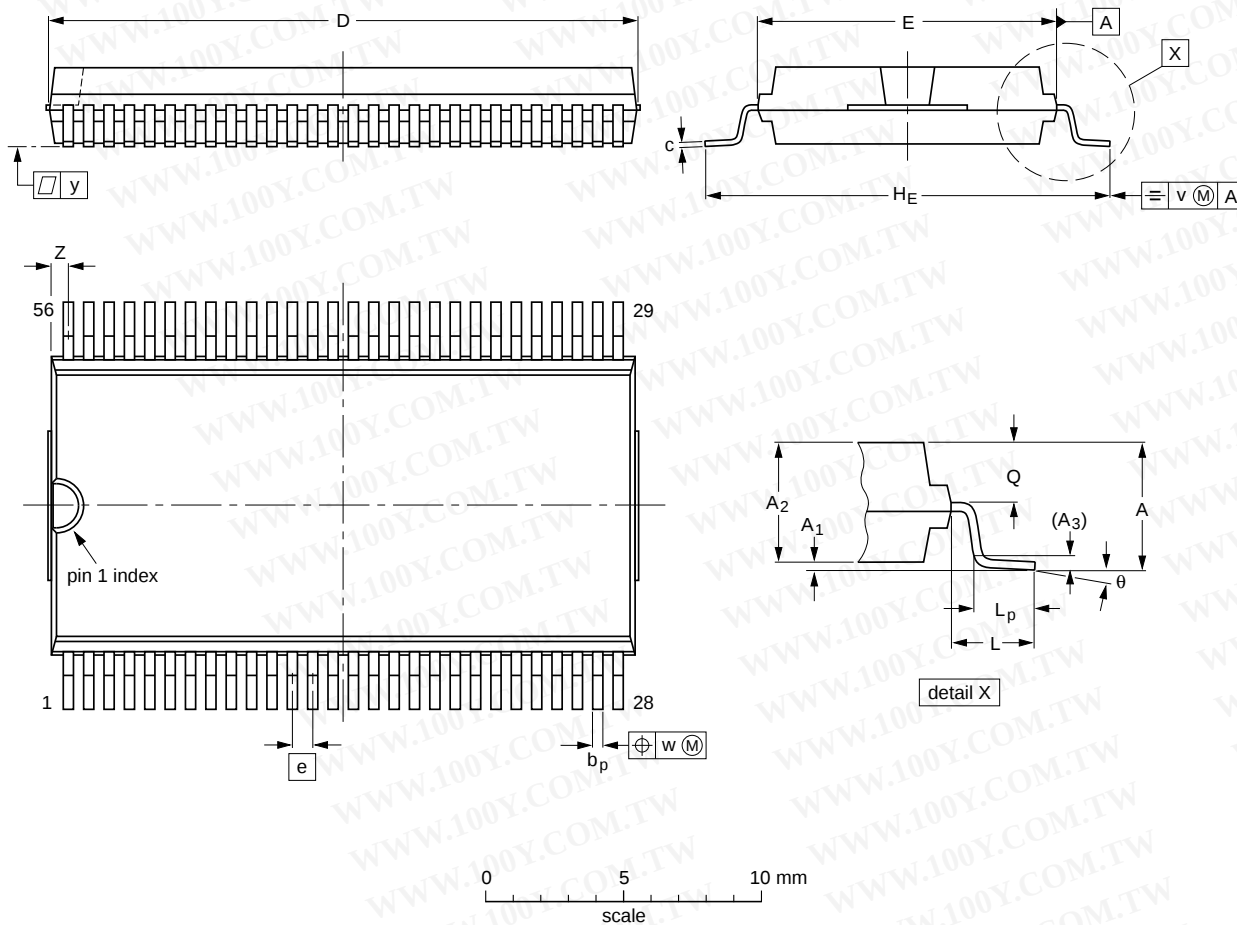
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PACKAGE OUTLINES

VSO56: plastic very small outline package; 56 leads

SOT190-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.03	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

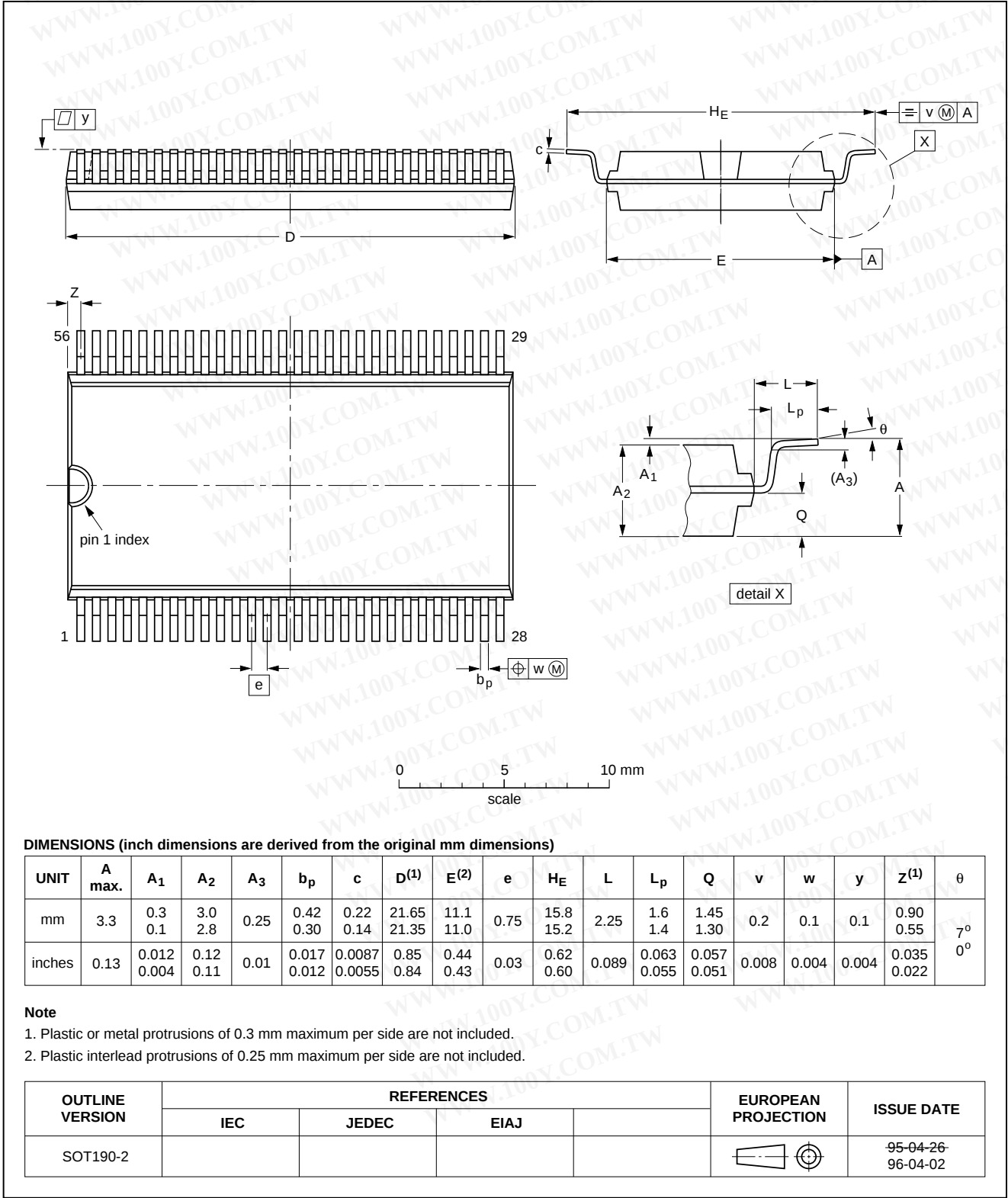
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						92-11-17 96-04-02

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VSO56: plastic very small outline package; 56 leads; face down

SOT190-2



In Car Entertainment (ICE) car radio

TEA6820T; TEA6822T

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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TEA6820T; TEA6822T

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale

PURCHASE OF PHILIPS I²C COMPONENTS

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