SERIAL E^2PROM

TC89101P, TC89102P

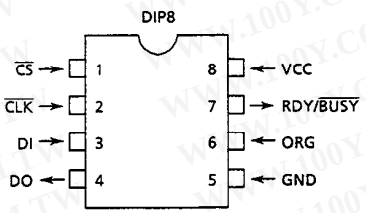
The TC89101P is a 1024-bit serial E²PROM. The TC89102P is a 2048-bit serial E²PROM. These are fabricated with floating gate CMOS technology.

PART No.	CAPACITY	ORGANIZATION	PACKAGE
TC89101P	1024-bit	128 x 8-bit or 64 x 16-bit	DIP8
TC89102P	2048-bit	256 x 8-bit or 128 x 16-bit	

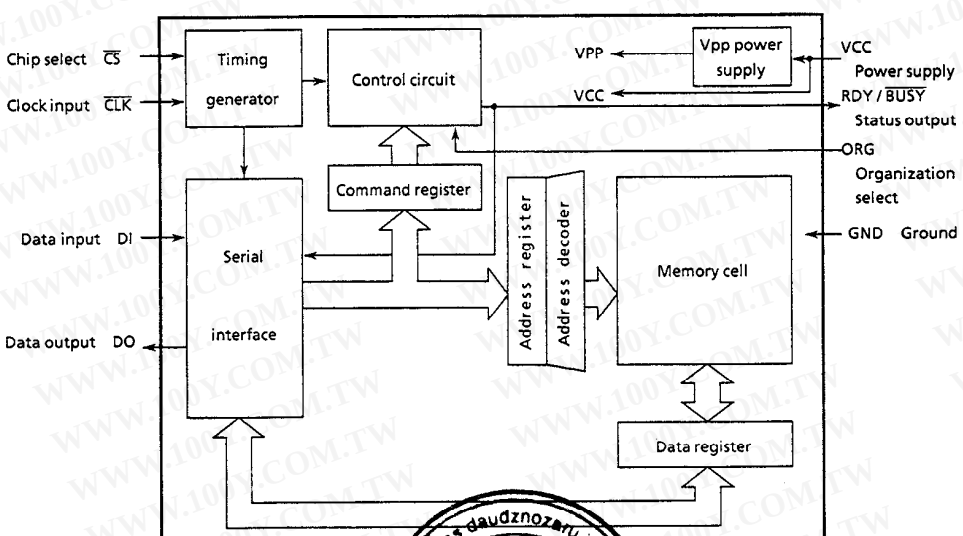
FEATURES

- ◆Single 5 V Supply
- ◆Low Power Dissipations
- ◆Serial Interface
- ◆Self timed Program cycle (Built-in Timer)
- ◆Ready / Busy status signal
- ◆Erase / Write Enable and Disable by software
- ◆Erase / Write Disable for low power supply
- ◆Program and Chip Erase
- ◆User Selectable Organization 8-bit or 16-bit

PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input / Output	FUNCTIONS
$\overline{CS}$	Input	Chip select Chip is enabled when $\overline{CS}$ is at "L" level. Set $\overline{CS}$ to "H" level before executing instructions.
$\overline{CLK}$	Input	Clock input The DI data is latched at the rising edge of $\overline{CLK}$. The data is output from DO at the falling edge of $\overline{CLK}$. $\overline{CLK}$ is enabled when $\overline{CS}$ is at "L" level.
DI	Input	Serial data input The address, command and data input pin.
DO	Output	Serial data output The data output pin.
ORG	Input	Organization select The 16-bit organization is selected when ORG is "H" level. The 8-bit organization is selected when ORG is "L" level.
RDY / $\overline{BUSY}$	Output	Status output "L" level is output during program or chip erase operation. "H" level is output when program or chip erase operation is completed.
VCC	Power supply	+ 5 V
GND		0 V (GND)

OPERATIONAL DESCRIPTION

1. INSTRUCTION SET

(1) TC89101

Instruction	Address		Command	Data	
	128 x 8-bit	64 x 16-bit	C0C1 C2 C3	128 x 8-bit	64 x 16-bit
Read	A0 to A6, 0	A0 to A5, 00	1 0 0 0 0 0 0 0		
Program	A0 to A6, 0	A0 to A5, 00	0 1 1 0 0 0 0 0	D0 to D7	D0 to D15
Chip Erase	* * * * * * * *	* * * * * * * *	0 0 1 1 0 0 0 0		
Busy Monitor	* * * * * * * *	* * * * * * * *	1 0 1 1 0 0 0 0		
E/W Enable	* * * * * * * *	* * * * * * * *	1 0 0 1 0 0 0 0		
E/W Disable	* * * * * * * *	* * * * * * * *	1 1 0 1 0 0 0 0		

*: don't care

(2) TC89102

Instruction	Address		Command	Data	
	256×8-bit	128×16-bit	C0C1 C2 C3	256×8-bit	128×16-bit
Read	A0 to A7	A0 to A6, 0	1 0 0 0 0 0 0 0		
Program	A0 to A7	A0 to A6, 0	0 1 1 0 0 0 0 0	D0 to D7	D0 to D15
Chip Erase	********	********	0 0 1 1 0 0 0 0		
Busy Monitor	********	********	1 0 1 1 0 0 0 0		
E/W Enable	********	********	1 0 0 1 0 0 0 0		
E/W Disable	********	********	1 1 0 1 0 0 0 0		

*: don't care

2. OPERATION METHOD

Set $\overline{CS}$ and $\overline{CLK}$ to "H" level before executing instruction. $\overline{CS}$ changes to "L" level, then $\overline{CLK}$ is enabled and operates as the sync signal for serial I/O. The DI data is latched at the rising edge of $\overline{CLK}$. The data is output from DO at the falling edge of $\overline{CLK}$.

Execute instruction only when RDY/$\overline{BUSY}$ status signal is "H" level. However Busy Monitor instruction can be executed whenever.

Uses only commands which are included in the Instruction Set listed above.

(1) **Read**

Executing Read instruction reads out the memory data at the specified address and outputs it serially from DO.

(2) **Program**

Executing Program instruction automatically starts internal rewriting of the memory data at the specified address with the input data.

After Program instruction is input, $\overline{CS}$ can be set to "H" level ever while the internal rewriting process is operating.

(3) **Chip Erase**

Executing Chip Erase instruction automatically Starts internal erasing of the memory data at all address.

After Chip Erase instruction is input, $\overline{CS}$ can be set to "H" level even while the internal erasing process is operating.

(4) **Busy Monitor**

Executing Busy Monitor instruction outputs the RDY/$\overline{BUSY}$ status signal from DO.

"L" level is output during Program or Chip Erase operation. "H" level is output when Program or Chip Erase operation is completed.

The RDY/$\overline{BUSY}$ status signal is output until $\overline{CS}$ is switched to "H" level.

(5) **E/W Enable**

Executing E/W Enable instruction sets E/W enable mode and enables Program and Chip Erase instructions.

(6) **E/W Disable**

Executing E/W Disable instruction sets the E/W disable mode and disables both the Program and Chip Erase instructions. Once E/W disable mode is set, E/W disable mode is held until E/W Enable instruction is executed.

3. CAUTIONS WHEN TURNING THE POWER ON AND OFF

(1) After turning the power on, wait 1ms for warm-up before executing instruction.

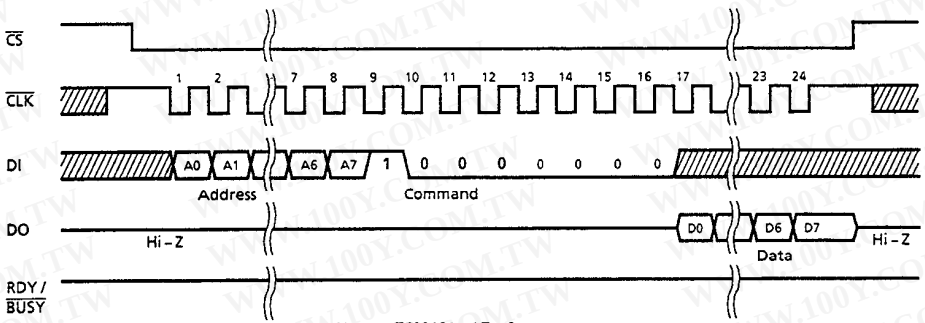
(2) After turning the power on, set either the E/W enable mode or E/W disable mode.

(3) If the power supply voltage is lower the approximately 3.5 V, E/W Disable instruction is automatically executed internally.

4. TIMING DIAGRAMS

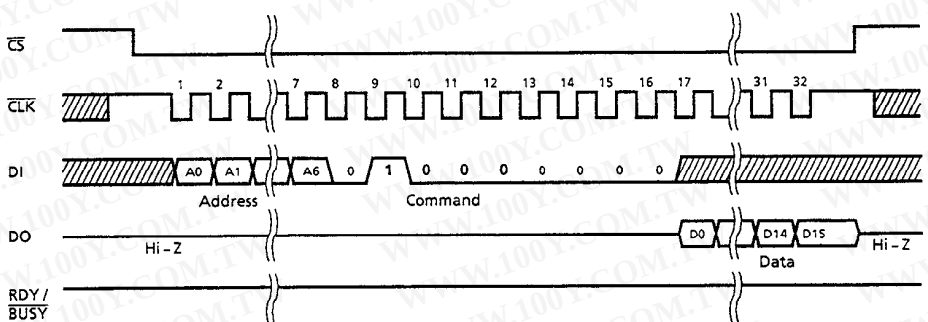
(1) Read

256×8



Note: TC89101; A7 = 0

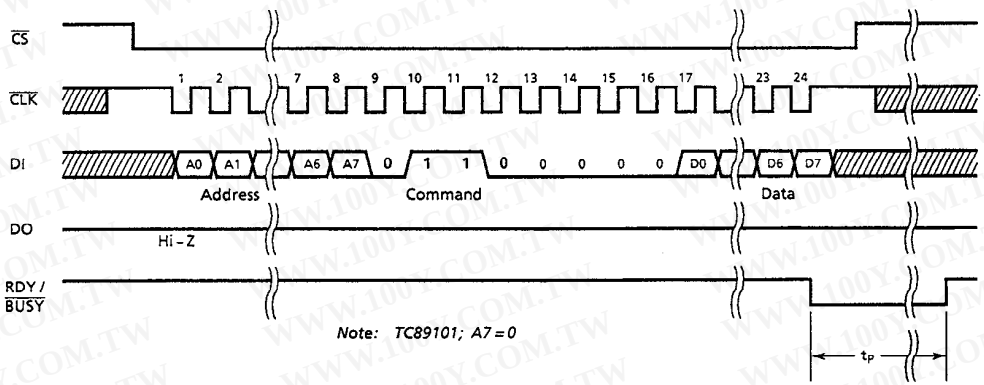
128×16



Note: TC89101; A6 = 0

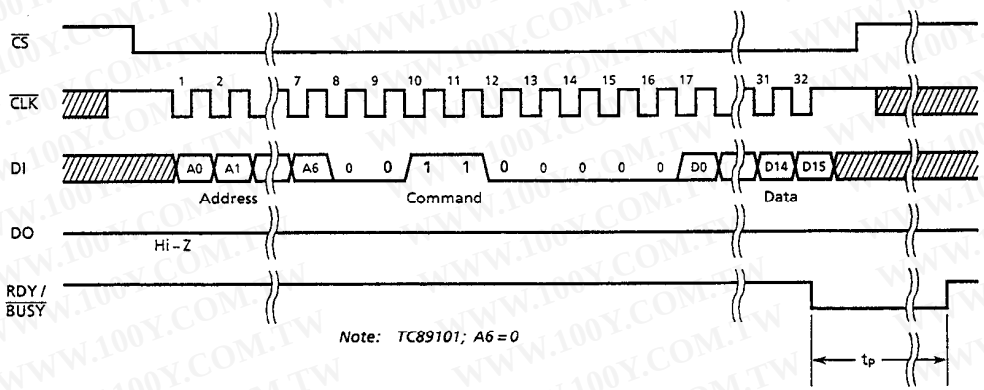
(2) Program

256×8



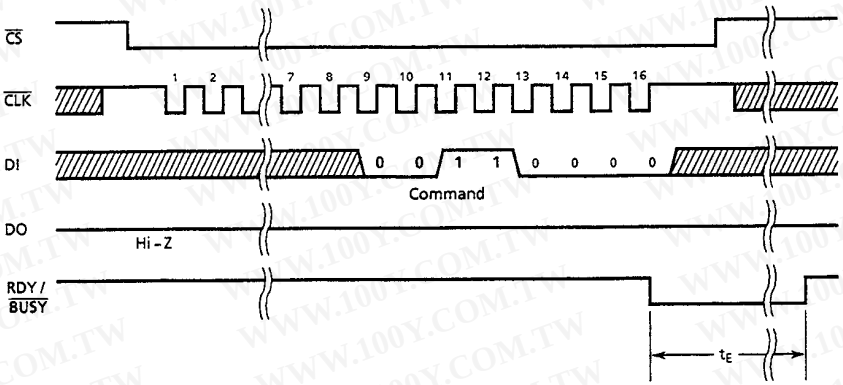
Note: TC89101; A7 = 0

128×16

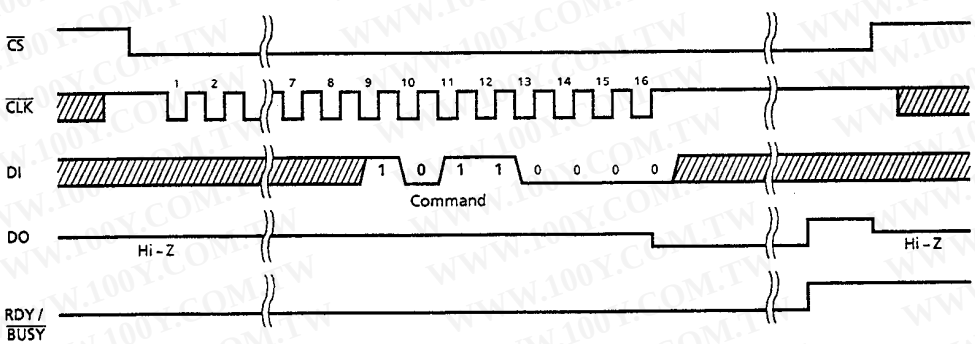


Note: TC89101; A6 = 0

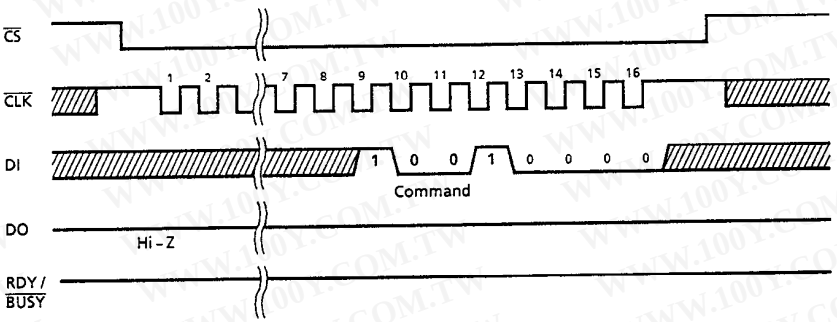
(3) Chip Erase



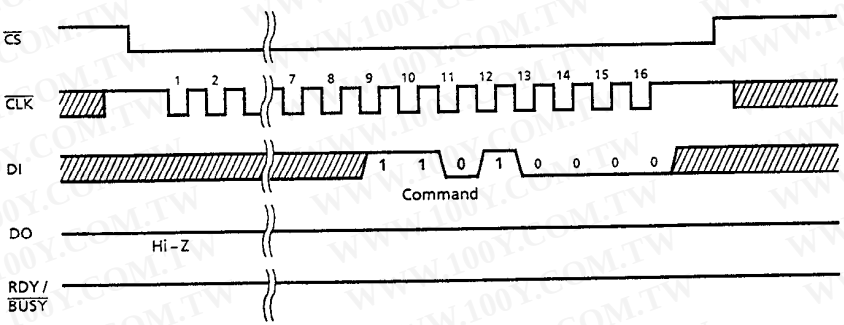
(4) Busy Monitor



(5) E/W Enable



(6) E/W Disable



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (GND = 0 V)

PARAMETER	SYMBOL	RATINGS	UNITS
Supply Voltage	V_{CC}	− 0.3 to 7	V
Input Voltage	V_{IN}	− 0.3 to V_{CC} + 0.3	V
Output Voltage	V_{OUT}	− 0.3 to V_{CC} + 0.3	V
Power Dissipation	PD	600	mW
Soldering Temperature (time)	Tsld	260 (10 s)	°C
Storage Temperature	Tstg	− 55 to 125	°C
Operating Temperature	Topr	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS (GND = 0 V, Topr = 0 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNITS
Supply Voltage	V_{CC}			4.5	5.5	V
Input Low Voltage	V_{IL}		V_{CC} = 4.5 V	0	0.8	V
Input High Voltage	V_{IH1}	$\overline{CS}$, DI, ORG	V_{CC} = 5.5 V	2.0	V_{CC}	V
	V_{IH2}	$\overline{CLK}$		3.0		
Clock Frequency	f_{CLK}			0	1	MHz

D.C. CHARACTERISTICS (GND = 0 V, Topr = 0 to 70 °C)

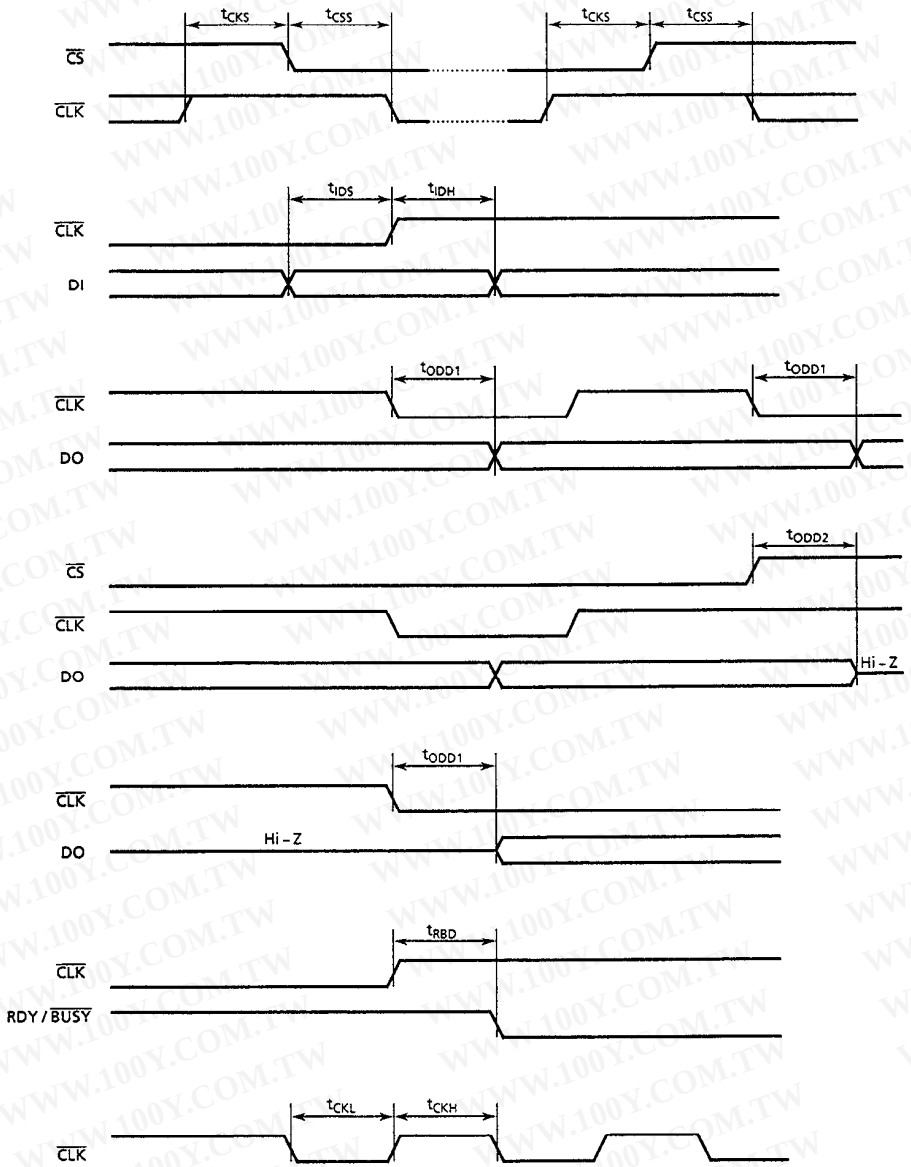
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNITS
Input Current	I_{LI}		−	−	± 10	μA
Output Leakage Current	I_{LO}		−	−	± 10	μA
Output High Voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = − 400 μA	2.4	−	−	V
Output Low Voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 2.1 mA	−	−	0.4	V
Supply Current	I_{CCO}		−	−	2	mA
	I_{CCP}	During Program or Chip Erase	−	−	10	mA
	I_{CCS}	$\overline{CS}$ = 1 (Except Program or Chip Erase operation)	−	−	100	μA

A.C. CHARACTERISTICS (GND = 0 V, V_{CC} = 4.5 to 5.5 V, Topr = 0 to 70 °C)

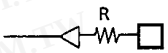
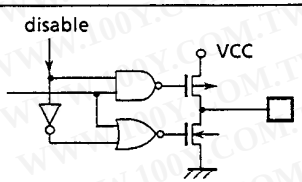
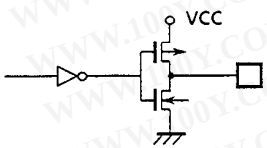
PARAMETER	SYMBOL	Min.	Max.	UNITS
$\overline{CLK}$ Frequency	f_{CLK}	0	1	MHz
$\overline{CLK}$ Low Time	t_{CKL}	400	–	ns
$\overline{CLK}$ High Time	t_{CKH}	400	–	ns
$\overline{CLK}$ Input Setup Time	t_{CKS}	250	–	ns
$\overline{CS}$ Input Setup Time	t_{CSS}	250	–	ns
DO Output Delay Time (Note)	t_{ODD1}	–	250	ns
	t_{ODD2}	–	500	ns
RDY/$\overline{BUSY}$ Output Delay Time	t_{RBD}	–	250	ns
DI Input Setup Time	t_{IDS}	250	–	ns
DI Input Hold Time	t_{IDH}	250	–	ns
Chip Erase Time	t_E	–	20	ms
Program Time	t_P	–	20	ms
Erase/Write Cycle	N_{EW}	10^4	–	cycles
Data Retention Time	t_{RET}	10	–	years

Note: C_L = 100 pF, V_{OH} / V_{OL} = 2.0 V / 0.8 V

A.C. CHARACTERISTICS TIMING DIAGRAMS



INPUT / OUTPUT CIRCUITRY

PIN NAME	I/O	CIRCUITRY	REMARKS
$\overline{CS}$ DI ORG	Input		
$\overline{CLK}$	Input		Hysteresis input
DO	Output		Initial "Hi-Z"
RDY / $\overline{BUSY}$	Output		Initial "High"