

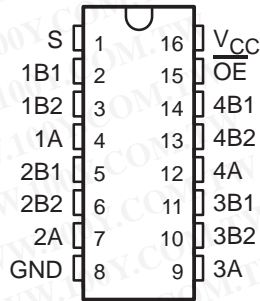
# SN74CBT3257 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS017M – MAY 1995 – REVISED JANUARY 2004

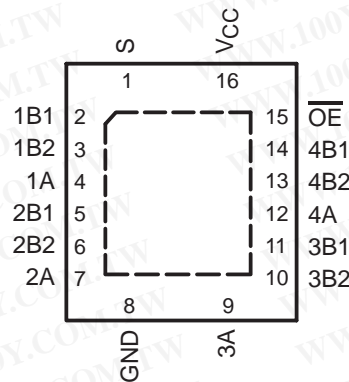
- 5-Ω Switch Connection Between Two Ports

- TTL-Compatible Input Levels

D, DB, DBQ, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



## description/ordering information

The SN74CBT3257 is a 4-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Output-enable ( $\overline{\text{OE}}$ ) and select-control (S) inputs select the appropriate B1 and B2 outputs for the A-input data.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74CBT3257RGYR	CU257
	SOIC – D	Tube	SN74CBT3257D	CBT3257
		Tape and reel	SN74CBT3257DR	
	SSOP – DB	Tape and reel	SN74CBT3257DBR	CU257
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3257DBQR	CU257
	TSSOP – PW	Tube	SN74CBT3257PW	CU257
Tape and reel		SN74CBT3257PWR		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INPUTS		FUNCTION
$\overline{\text{OE}}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

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TEXAS  
INSTRUMENTS

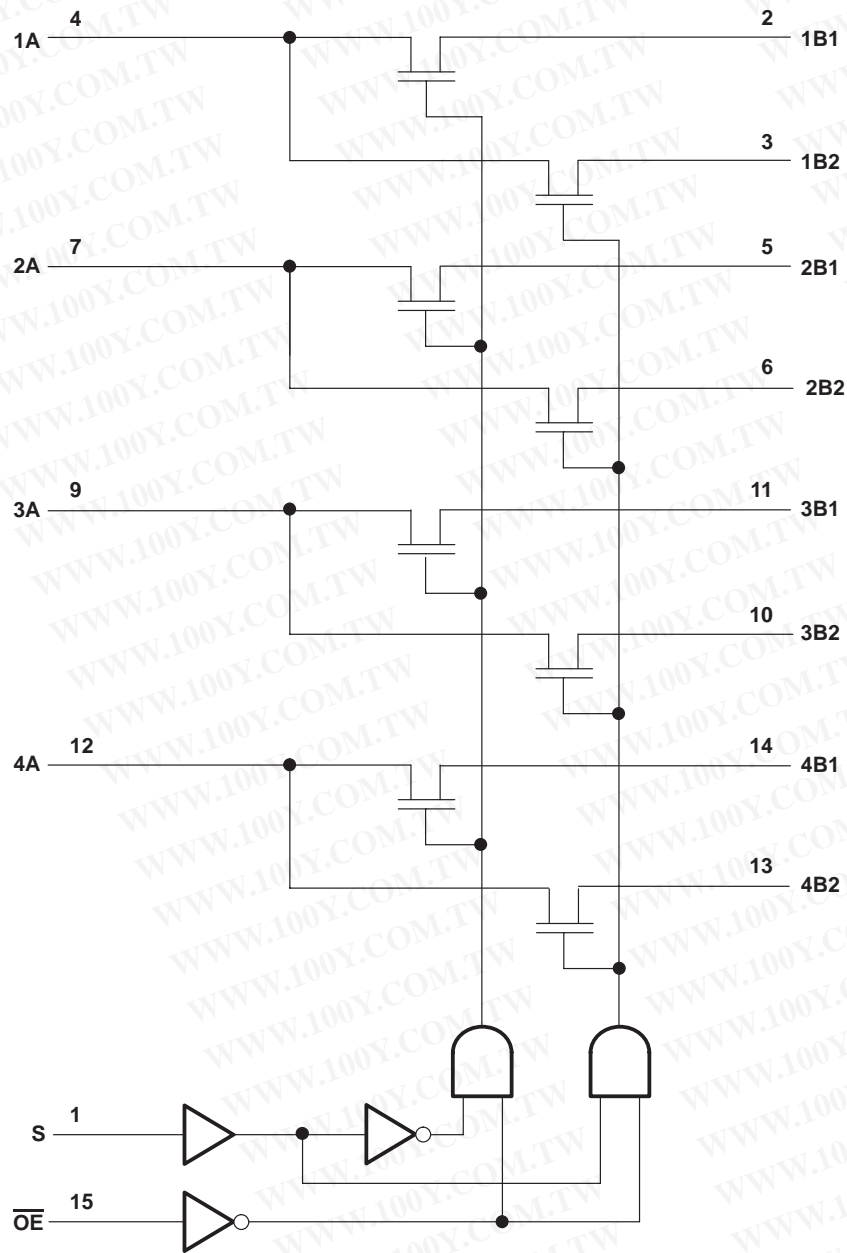
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# SN74CBT3257 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

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## logic diagram (positive logic)



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_K$ ( $V_{I/O} < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
(see Note 2): DB package	82°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): PW package	108°C/W
(see Note 3): RGY package	39°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

**recommended operating conditions (see Note 4)**

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
$I_I$	$V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND			±1	µA
$I_{CC}$	$V_{CC} = 5.5$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND			3	µA
$\Delta I_{CC}$ §	Control inputs $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2.5	mA
$C_i$	Control inputs $V_I = 3$ V or 0			3.5	pF
$C_{iO(OFF)}$	A port $V_O = 3$ V or 0, $\overline{OE} = V_{CC}$			6.5	pF
	B port			4	
$r_{on}$ ¶	$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V	$V_I = 2.4$ V,	$I_I = 15$ mA	14	20
	$V_{CC} = 4.5$ V	$V_I = 0$	$I_I = 64$ mA	5	7
			$I_I = 30$ mA	5	7
		$V_I = 2.4$ V,	$I_I = 15$ mA	10	15

‡ All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

# SN74CBT3257

## 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

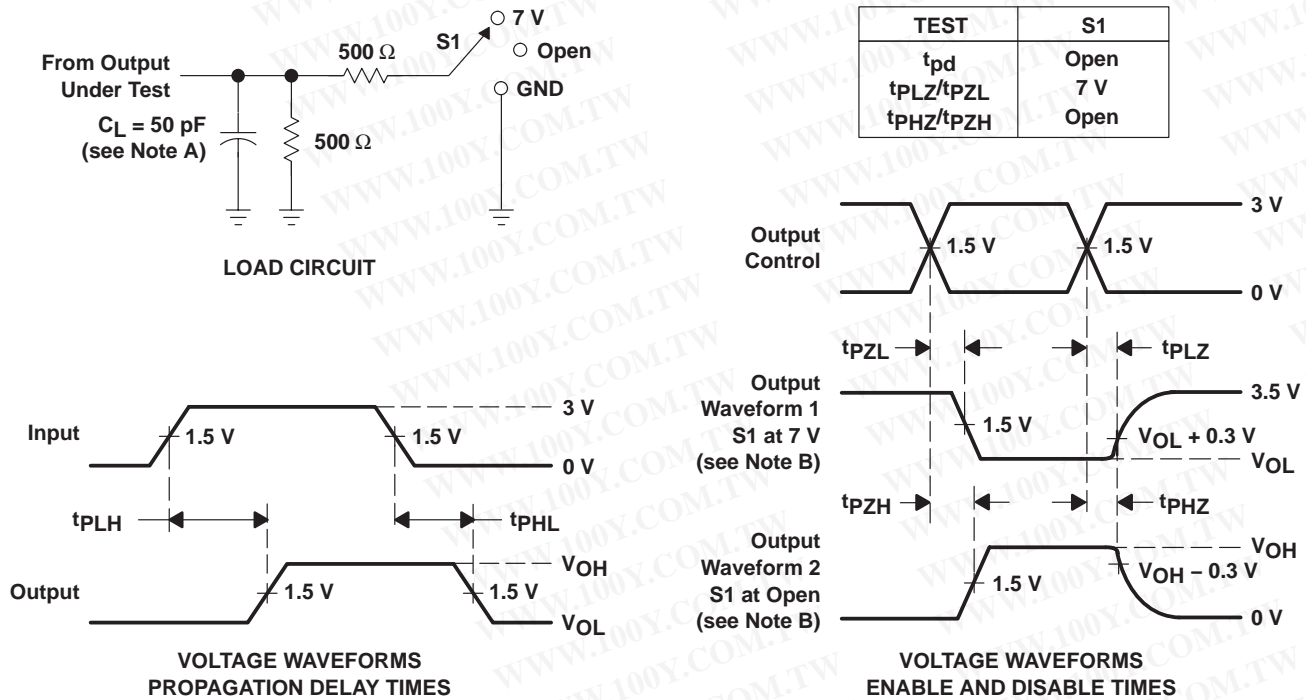
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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V $\pm 0.5$ V		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\dagger$	A or B	B or A	0.35		0.25		ns
$t_{pd}$	S	A	5.5		1.6	5	ns
$t_{en}$	S	B	5.7		1.6	5.2	ns
	$\overline{OE}$	A or B	5.6		1.8	5.1	
$t_{dis}$	S	B	5.2		1	5	ns
	$\overline{OE}$	A or B	5.5		2.2	5.5	

$^\dagger$  The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74CBT3257D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257DBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI
SN74CBT3257DBQR	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBT3257DBQRE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBT3257DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257PWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
SN74CBT3257PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3257RGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

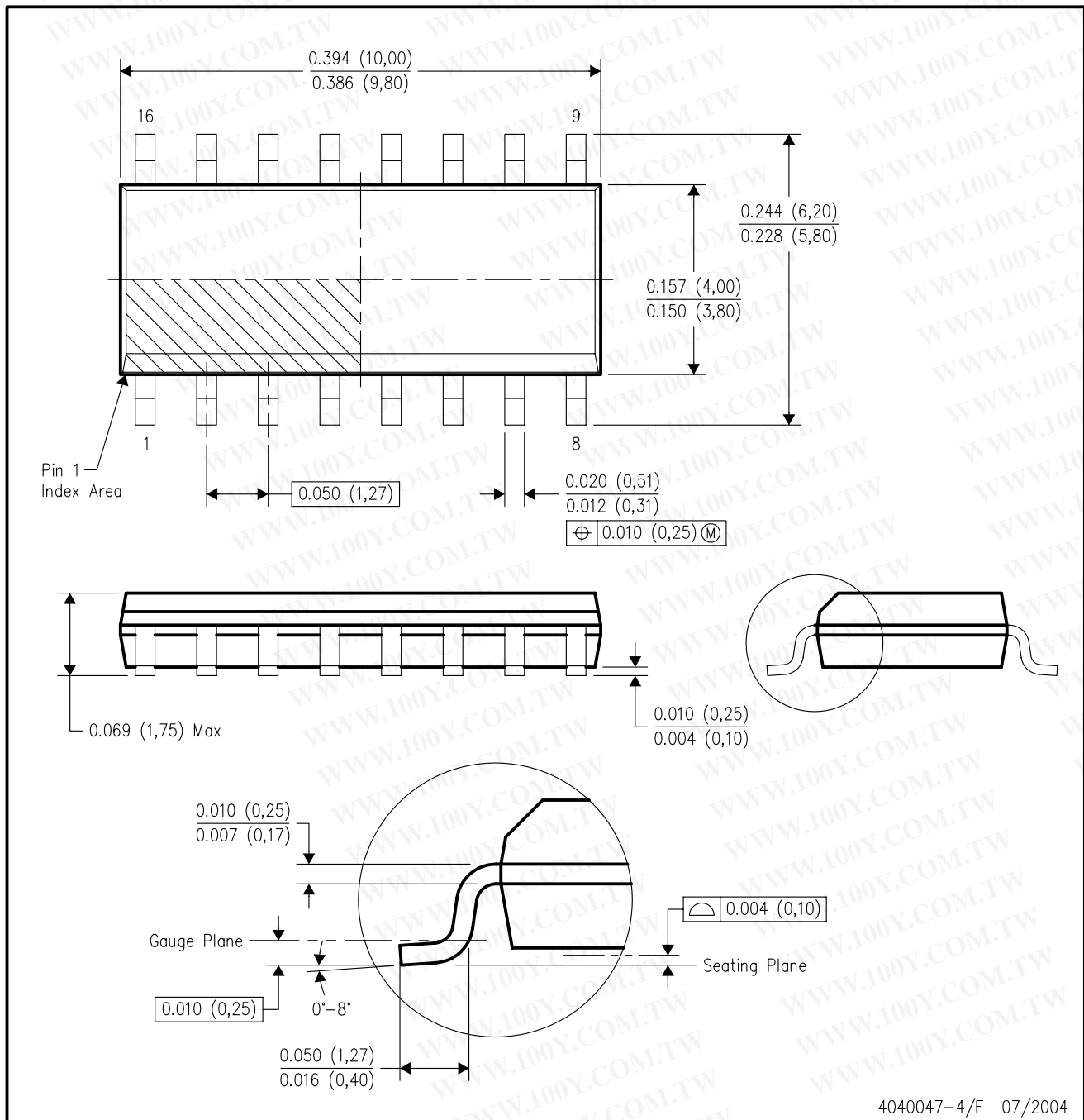
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D (R-PDSO-G16)

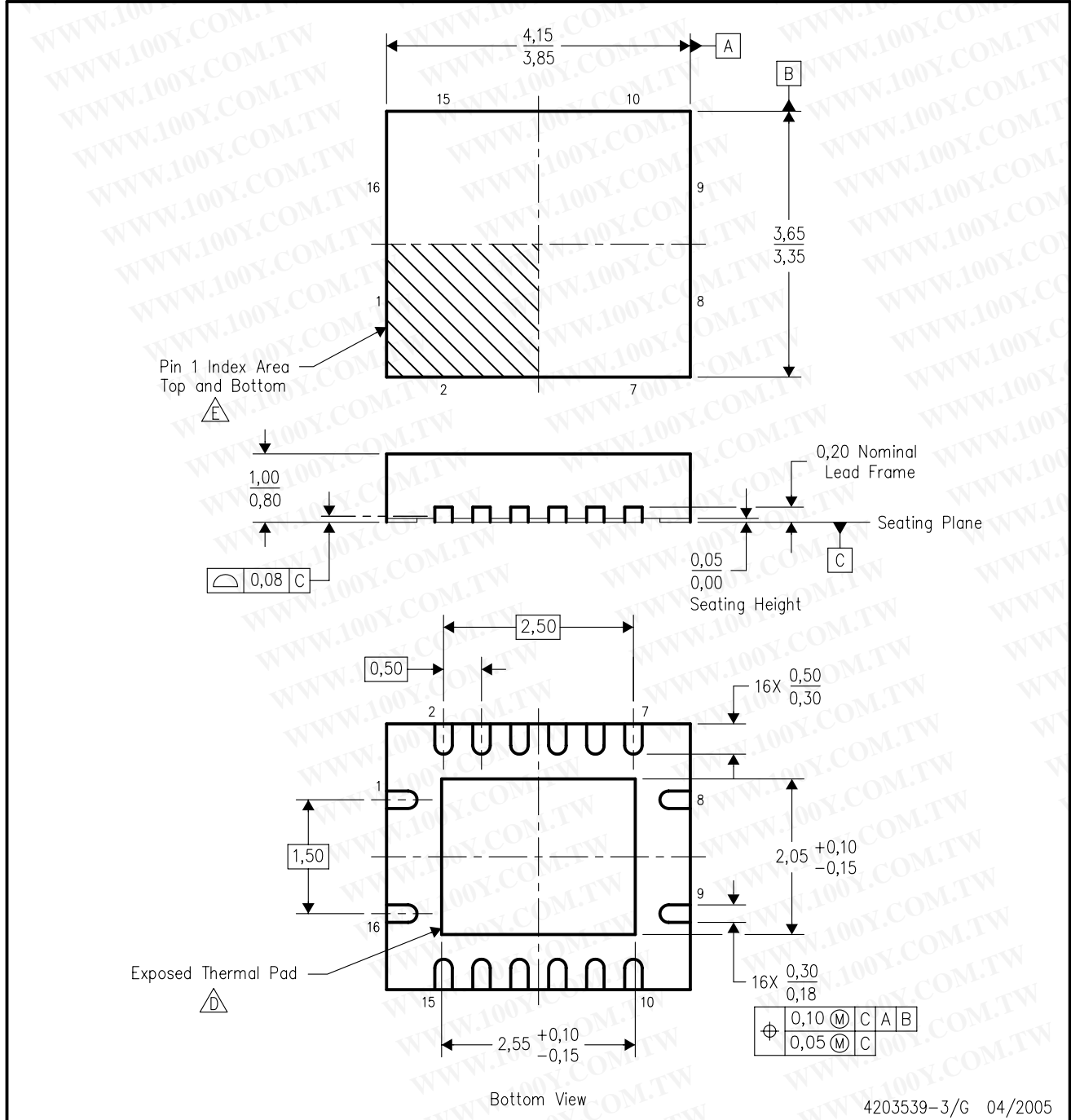
PLASTIC SMALL-OUTLINE PACKAGE





- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012 variation AC.

RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK

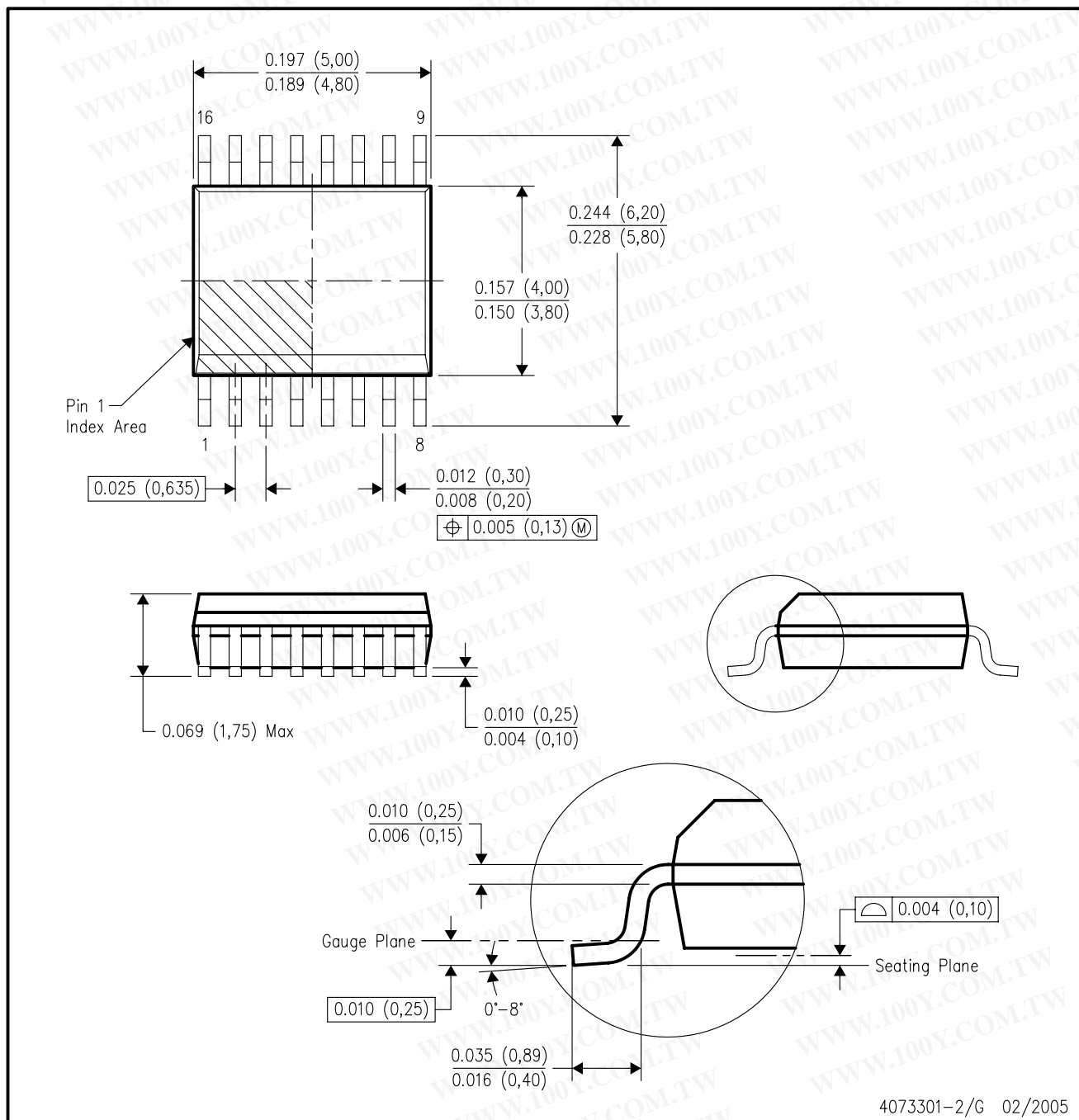


4203539-3/G 04/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BB.

DBQ (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

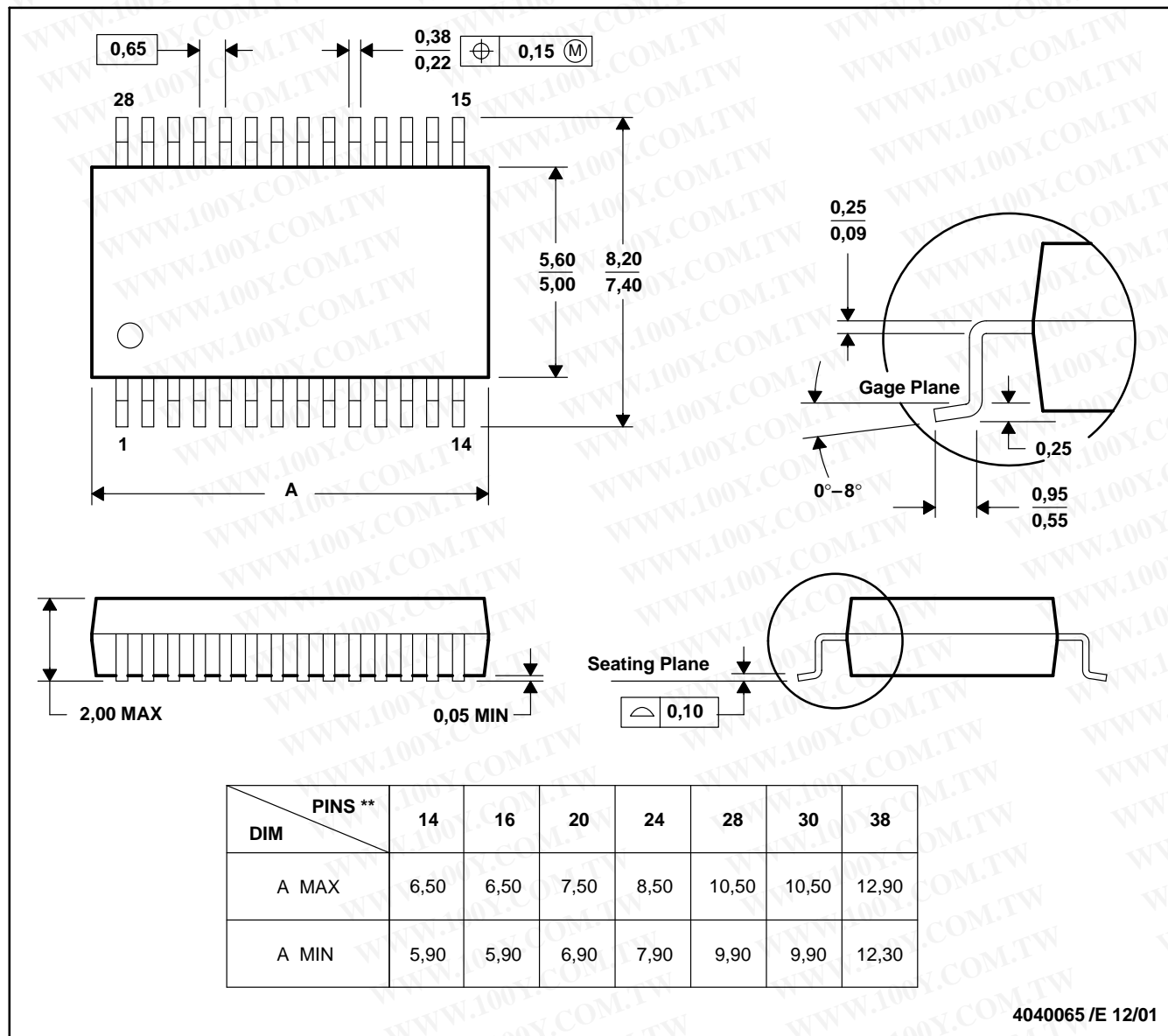


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AB.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



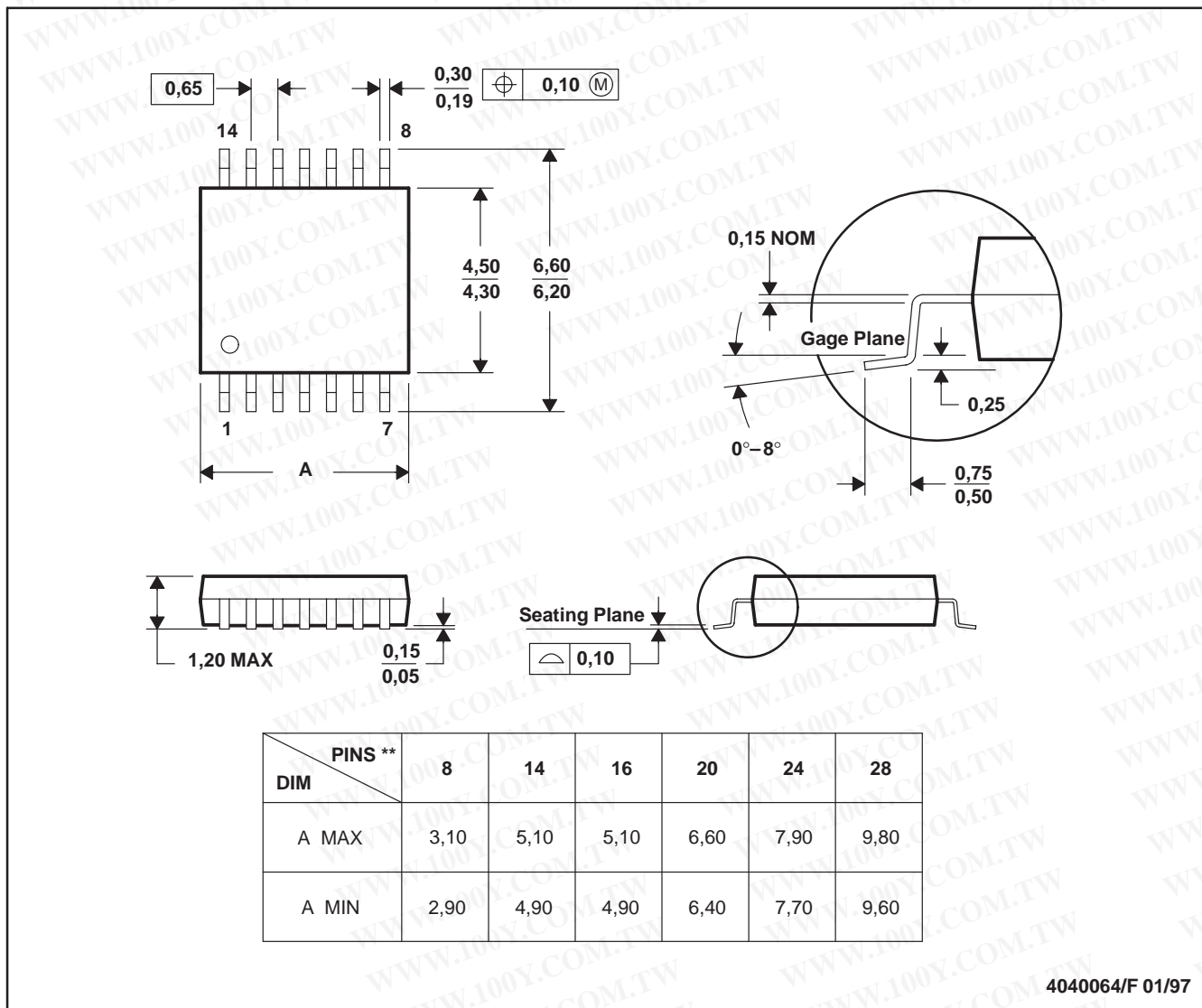
- NOTES: A. All linear dimensions are in millimeters.  
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PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



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 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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