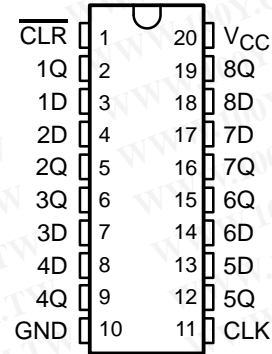
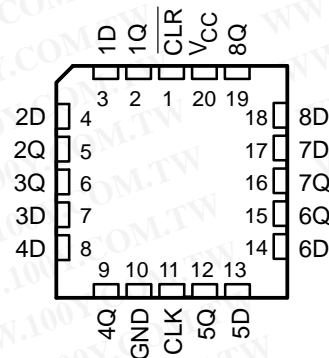


- Operating Range 2-V to 5.5-V V_{CC}
- Contain Eight Flip-Flops With Single-Rail Outputs
- Direct Clear Input
- Individual Data Input to Each Flip-Flop
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

SN54AHC273 ... J OR W PACKAGE
 SN74AHC273 ... DB, DGV, DW, N, NS, OR PW PACKAGE
 (TOP VIEW)



SN54AHC273 ... FK PACKAGE
 (TOP VIEW)



description/ordering information

These circuits are positive-edge-triggered D-type flip-flops with a direct clear (CLR) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC273N	SN74AHC273N
	SOIC – DW	Tube	SN74AHC273DW	AHC273
		Tape and reel	SN74AHC273DWR	
	SOP – NS	Tape and reel	SN74AHC273NSR	AHC273
	SSOP – DB	Tape and reel	SN74AHC273DBR	HA273
	TSSOP – PW	Tube	SN74AHC273PW	HA273
		Tape and reel	SN74AHC273PWR	
TVSOP – DGV	Tape and reel	SN74AHC273DGVR	HA273	
–55°C to 125°C	CDIP – J	Tube	SNJ54AHC273J	SNJ54AHC273J
	CFP – W	Tube	SNJ54AHC273W	SNJ54AHC273W
	LCCC – FK	Tube	SNJ54AHC273FK	SNJ54AHC273FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54AHC273, SN74AHC273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

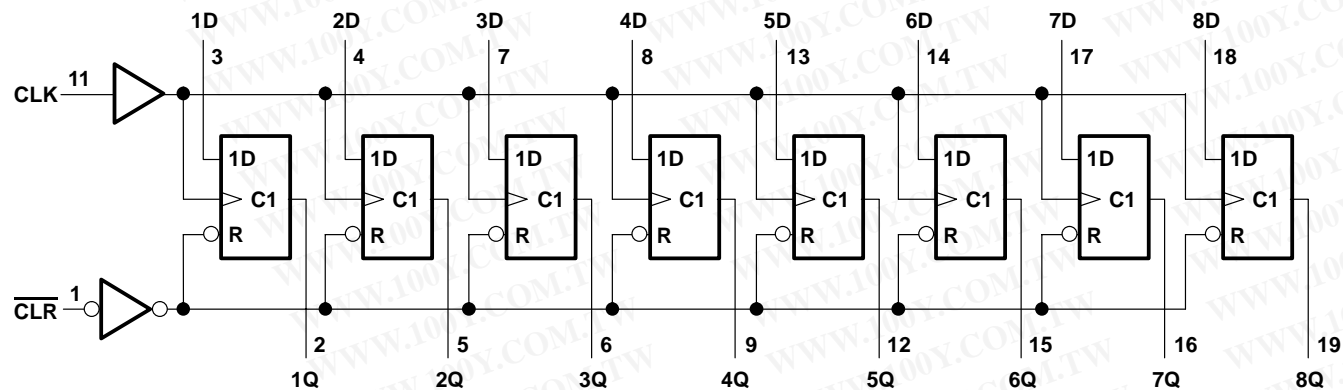
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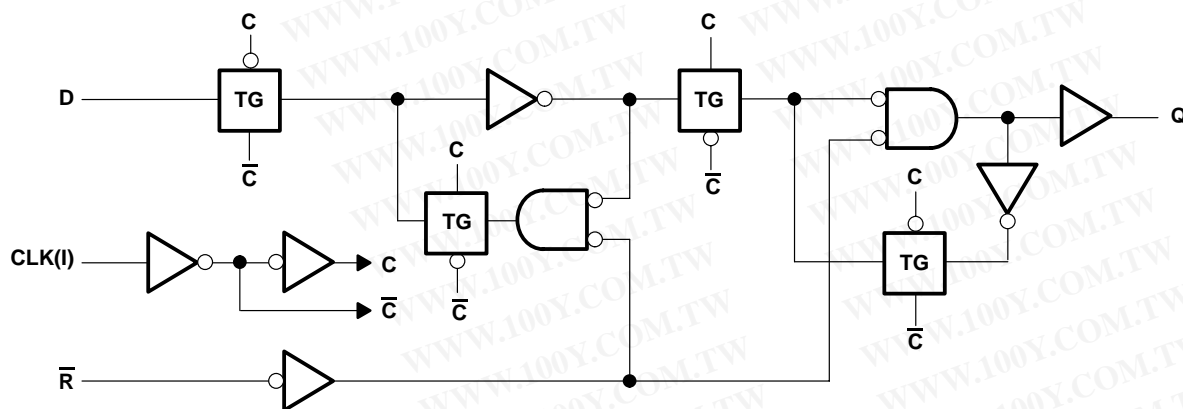
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic diagram (positive logic)



logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54AHC273		SN74AHC273		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5		V
		$V_{CC} = 3$ V		2.1		
		$V_{CC} = 5.5$ V		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		V
		$V_{CC} = 3$ V		0.9		
		$V_{CC} = 5.5$ V		1.65		
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		–50		μ A
		$V_{CC} = 3.3$ V ± 0.3 V		–4		mA
		$V_{CC} = 5$ V ± 0.5 V		–8		mA
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		μ A
		$V_{CC} = 3.3$ V ± 0.3 V		4		mA
		$V_{CC} = 5$ V ± 0.5 V		8		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54AHC273, SN74AHC273
OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC273		SN74AHC273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9			1.9		1.9		V
		3 V	2.9			2.9		2.9		
		4.5 V	4.4			4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V	0.1			0.1		0.1		V
		3 V	0.1			0.1		0.1		
		4.5 V	0.1			0.1		0.1		
	I _{OL} = 4 mA	3 V	0.36			0.5		0.44		
	I _{OL} = 8 mA	4.5 V	0.36			0.5		0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V	±0.1			±1*		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	4			40		40		μA
C _i	V _I = V _{CC} or GND	5 V	2.5 10					10		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		SN54AHC273				SN74AHC273				UNIT
		T _A = 25°C		MIN	MAX	T _A = 25°C		MIN	MAX	
		MIN	MAX			MIN	MAX			
t _w	Pulse duration	CLR low	5		6	5		6		ns
		CLK high or low	5			5		6.5		
t _{su}	Setup time	Data before CLK↑	5.5		6.5	5.5		6.5		ns
		CLR before CLK↑	2.5			2.5		2.5		
t _h	Hold time, data after CLK↑	1.5		2	1		1		ns	

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		SN54AHC273				SN74AHC273				UNIT
		T _A = 25°C		MIN	MAX	T _A = 25°C		MIN	MAX	
		MIN	MAX			MIN	MAX			
t _w	Pulse duration	CLR low	5		5	5		5		ns
		CLK high or low	5			5		5		
t _{su}	Setup time	Data before CLK↑	4.5		4.5	4.5		4.5		ns
		CLR before CLK↑	2			2		2		
t _h	Hold time, data after CLK↑	1.5		2	1		1		ns	



switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC273		SN74AHC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	75*	120*		65*		65		MHz
			$C_L = 50\text{ pF}$	50	75		45		45		
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		8.9*	13.6*	1*	16*	1	16	ns
t_{PLH}	CLK	Q	$C_L = 15\text{ pF}$		8.7*	13.6*	1*	16*	1	16	ns
t_{PHL}					8.7*	13.6*	1*	16*	1	16	
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		11.4	17.1	1	19.5	1	19.5	ns
t_{PLH}	CLK	Q	$C_L = 50\text{ pF}$		11.2	17.1	1	19.5	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	1	19.5	
$t_{\text{sk}(o)}$			$C_L = 50\text{ pF}$			1.5**				1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC273		SN74AHC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	120*	165*		100*		100		MHz
			$C_L = 50\text{ pF}$	80	110		70		70		
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		5.2*	8.5*	1*	10*	1	10	ns
t_{PLH}	CLK	Q	$C_L = 15\text{ pF}$		5.8*	9*	1*	10.5*	1	10.5	ns
t_{PHL}					5.8*	9*	1*	10.5*	1	10.5	
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		6.7	10.5	1	12	1	12	ns
t_{PLH}	CLK	Q	$C_L = 50\text{ pF}$		7.3	11	1	12.5	1	12.5	ns
t_{PHL}					7.3	11	1	12.5	1	12.5	
$t_{\text{sk}(o)}$			$C_L = 50\text{ pF}$			1**				1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHC273			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage		3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

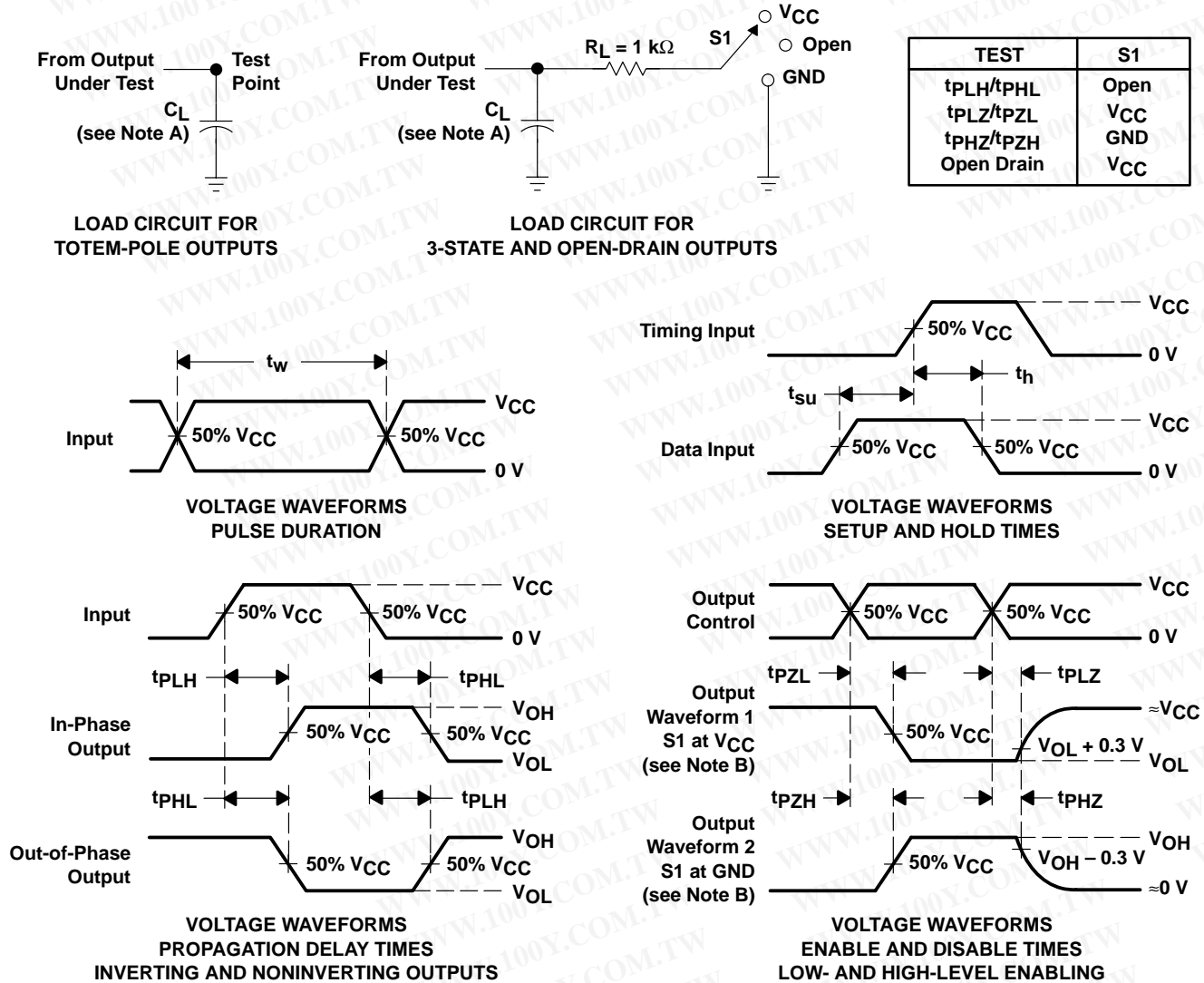
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	31	pF

SN54AHC273, SN74AHC273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCLS376G – JUNE 1997 – REVISED JULY 2003

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9853001Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
5962-9853001QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
5962-9853001QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN74AHC273DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74AHC273DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273DGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273DGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC273NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC273NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74AHC273PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC273PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54AHC273FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54AHC273J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54AHC273W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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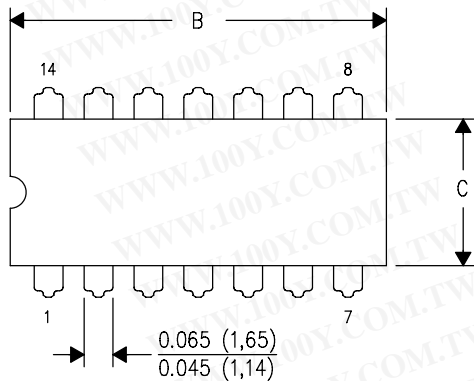
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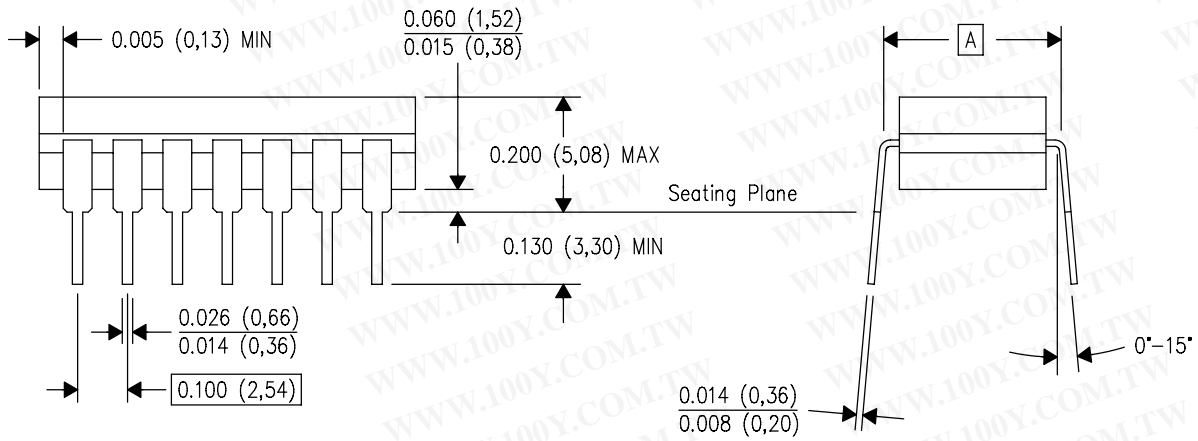
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J (R-GDIP-T**)
 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM	PINS **			
	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

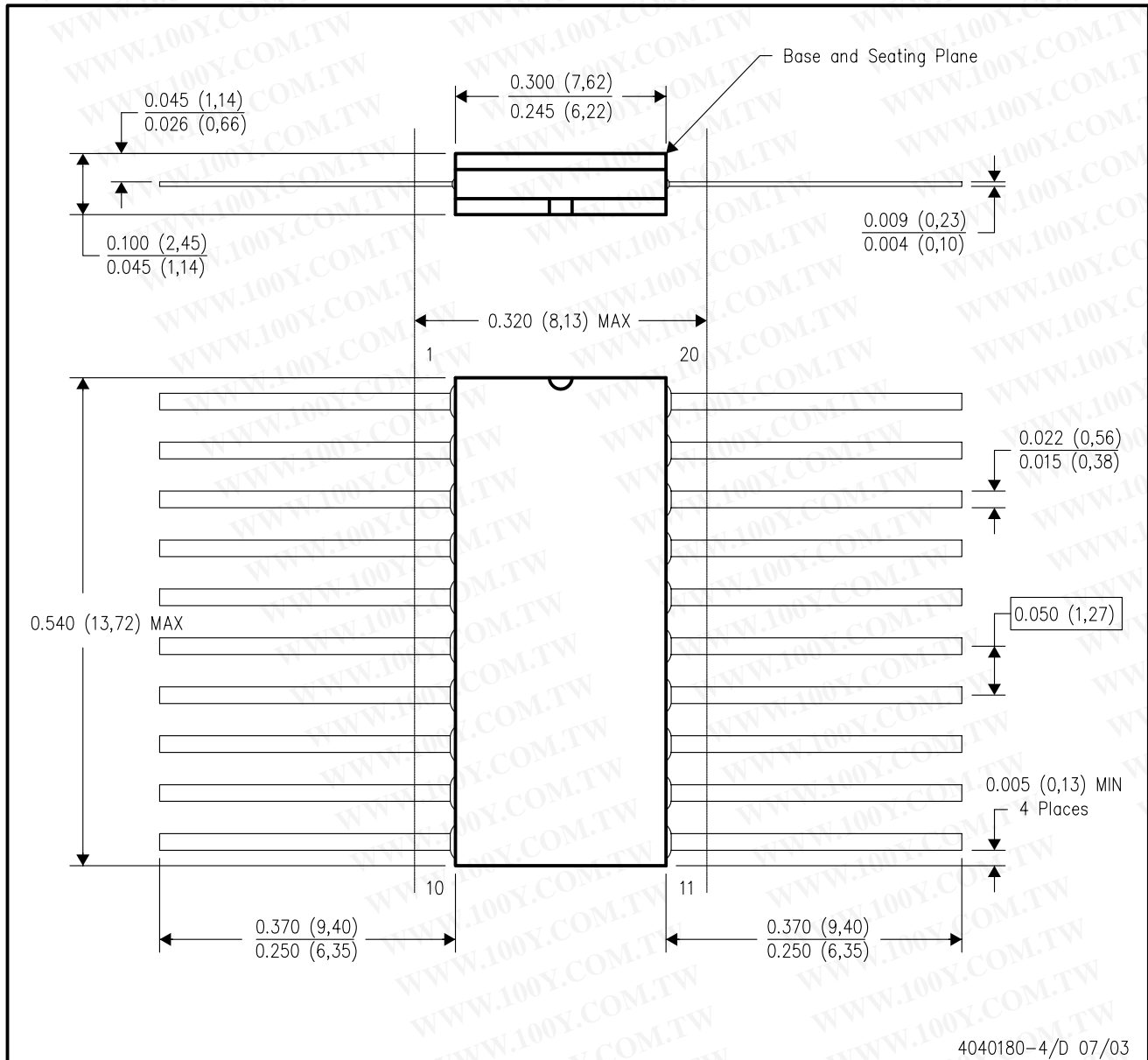


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



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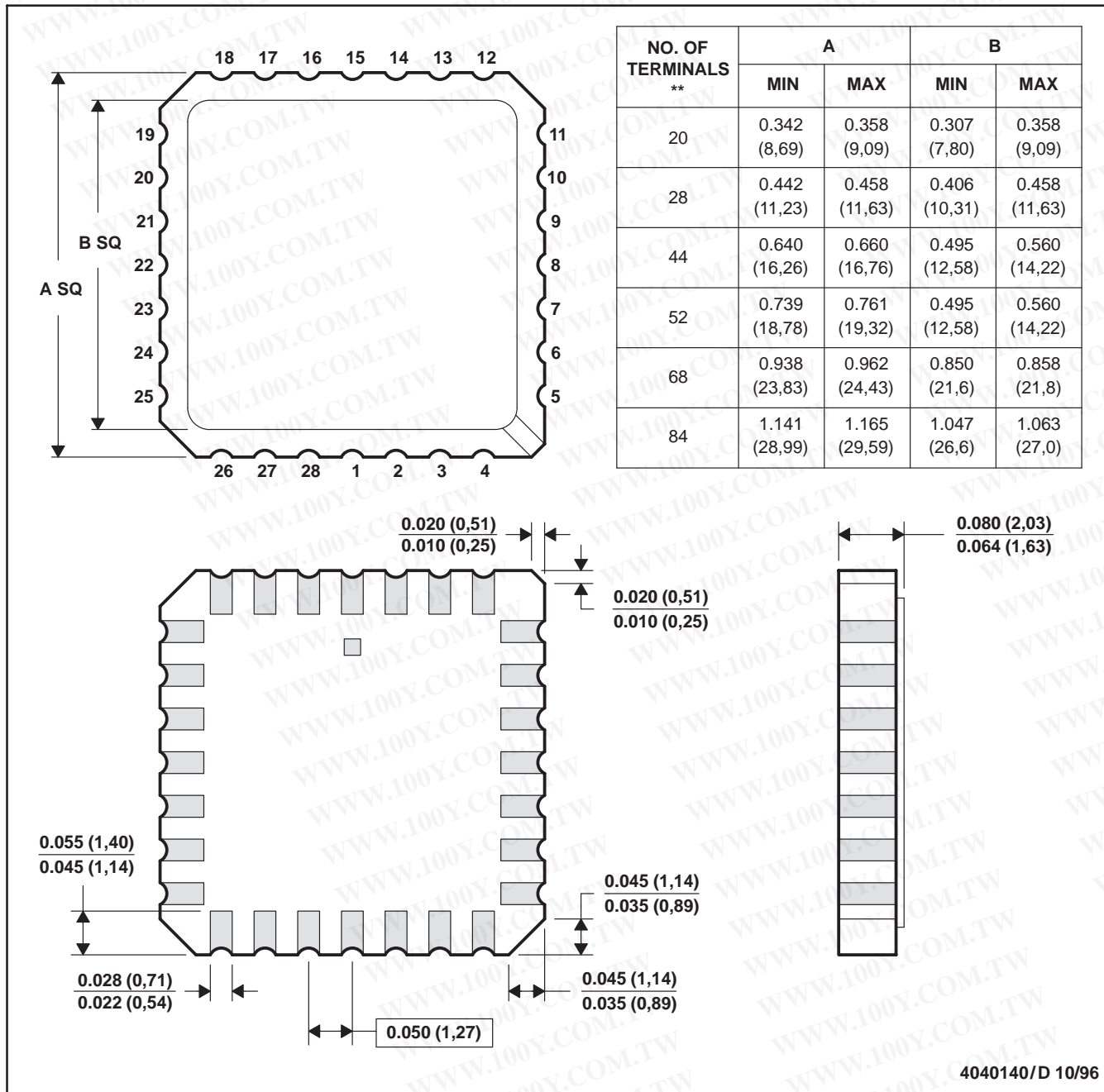
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

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FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



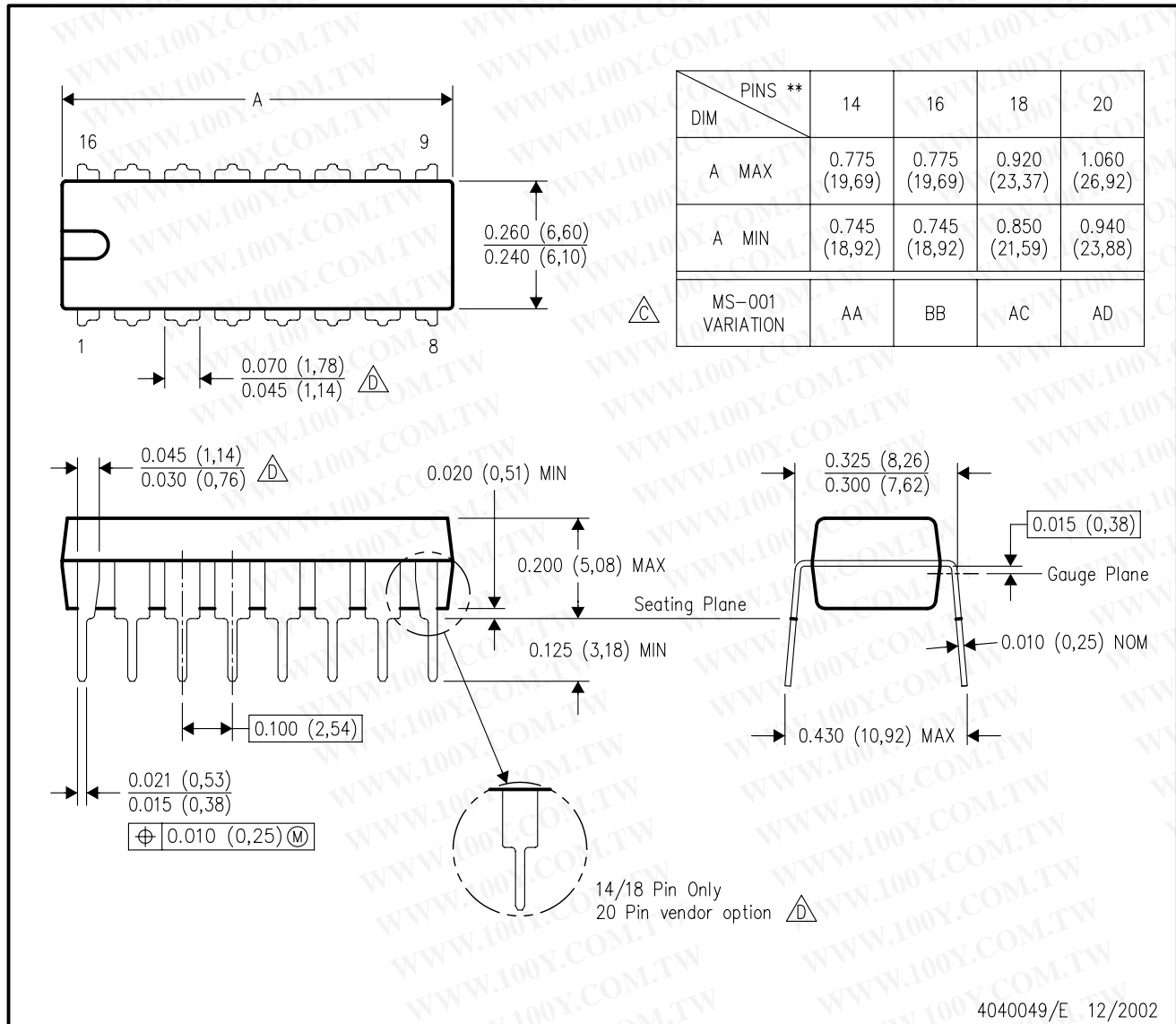
4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



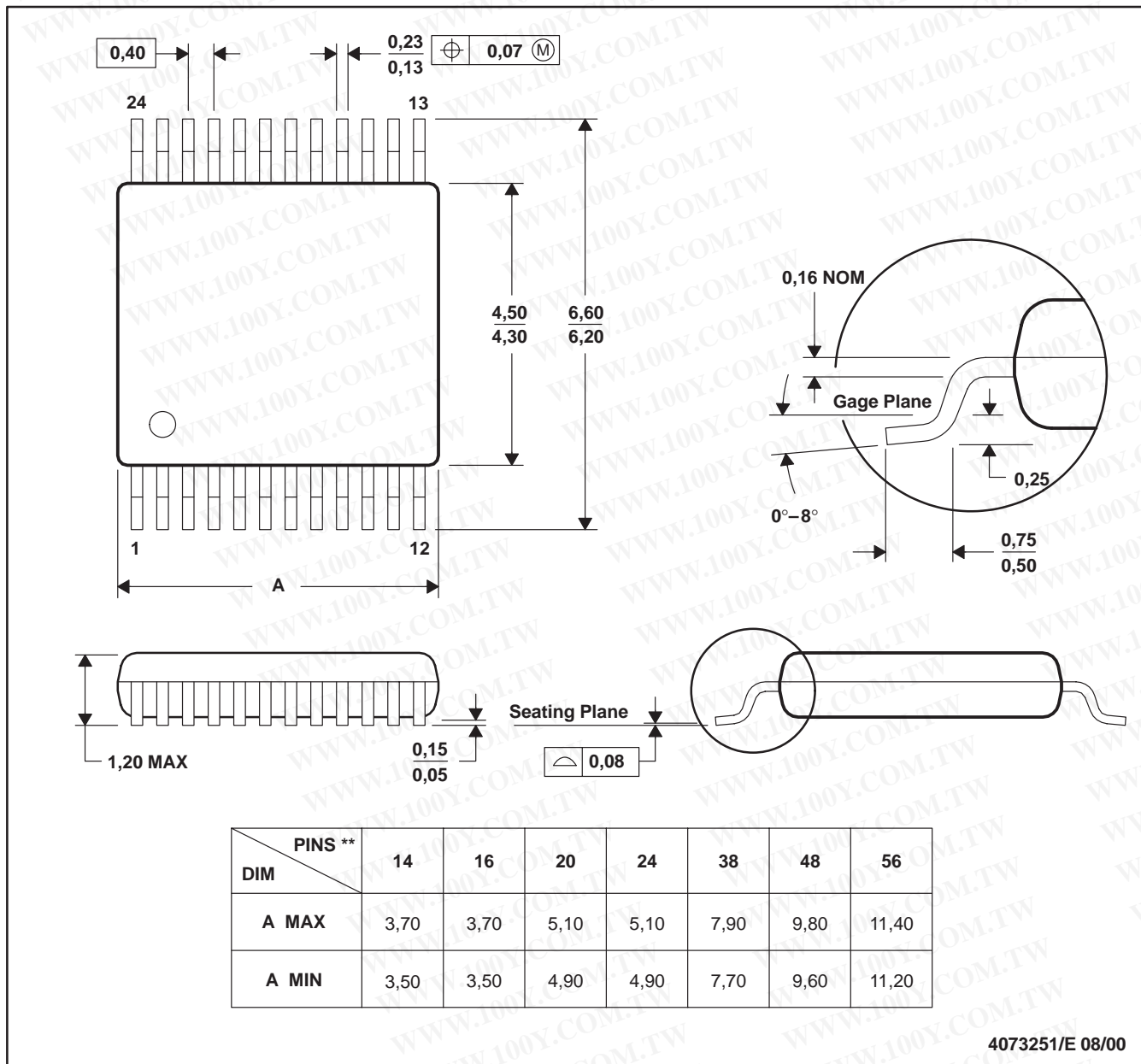
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

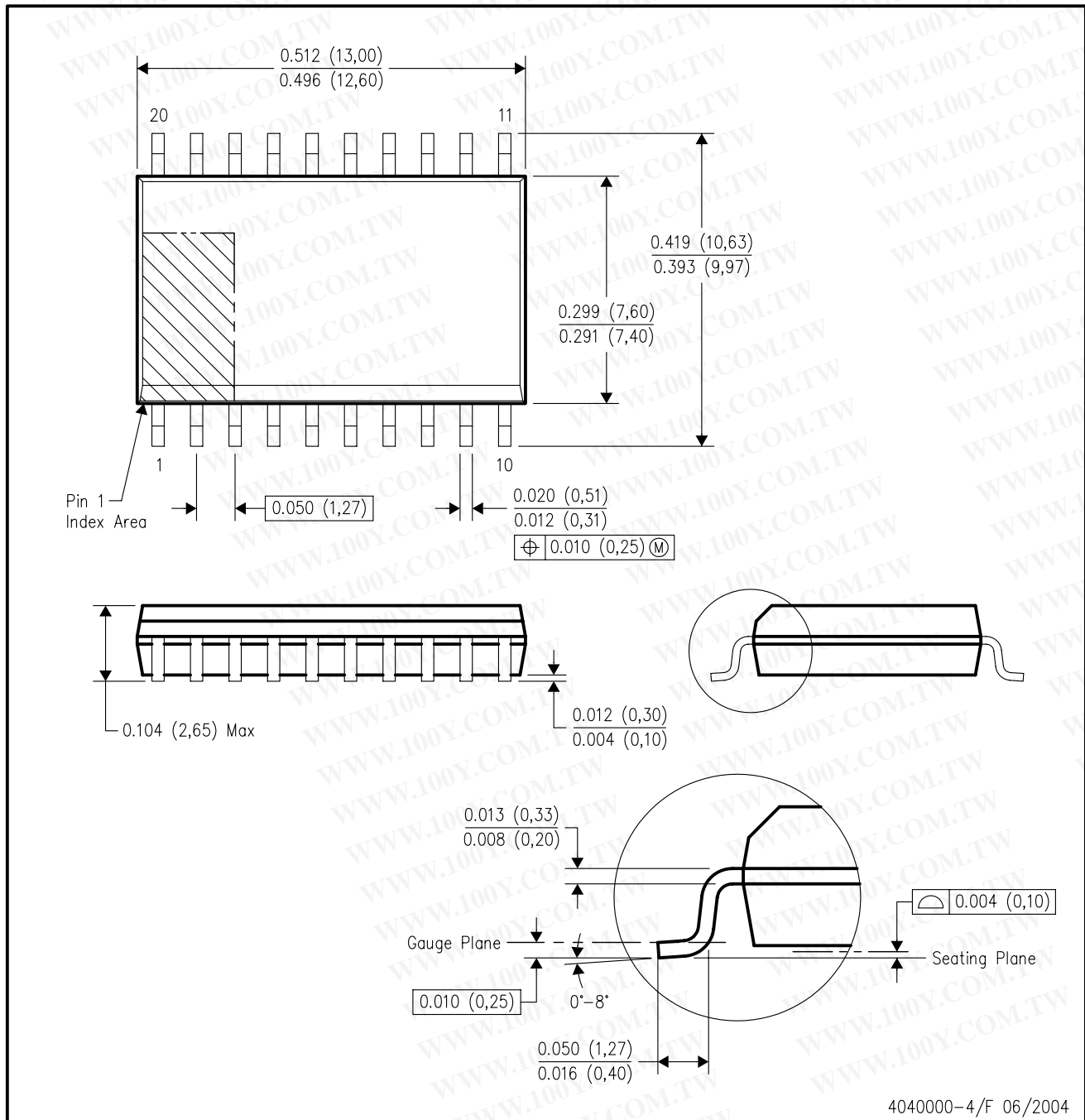


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



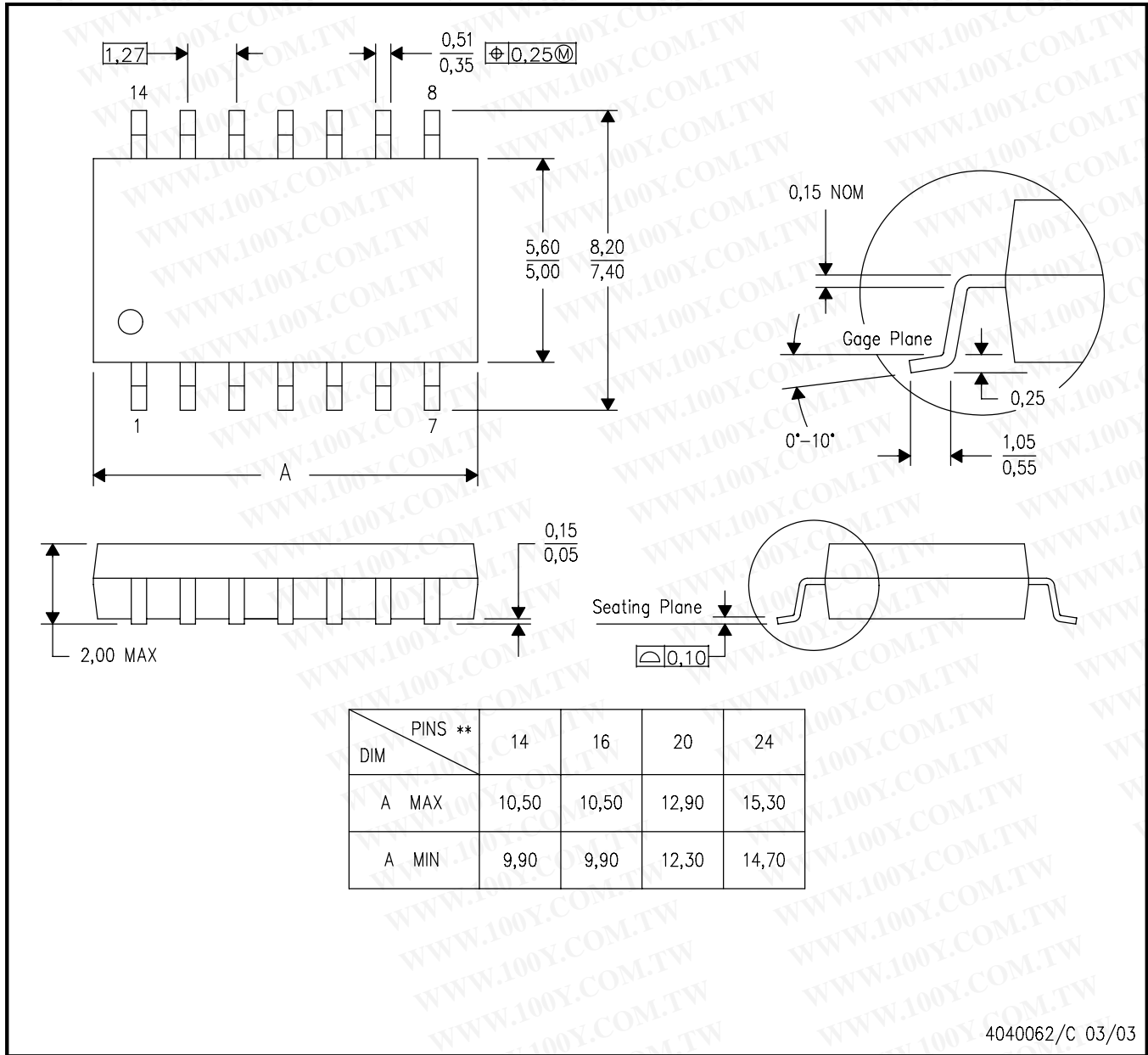
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

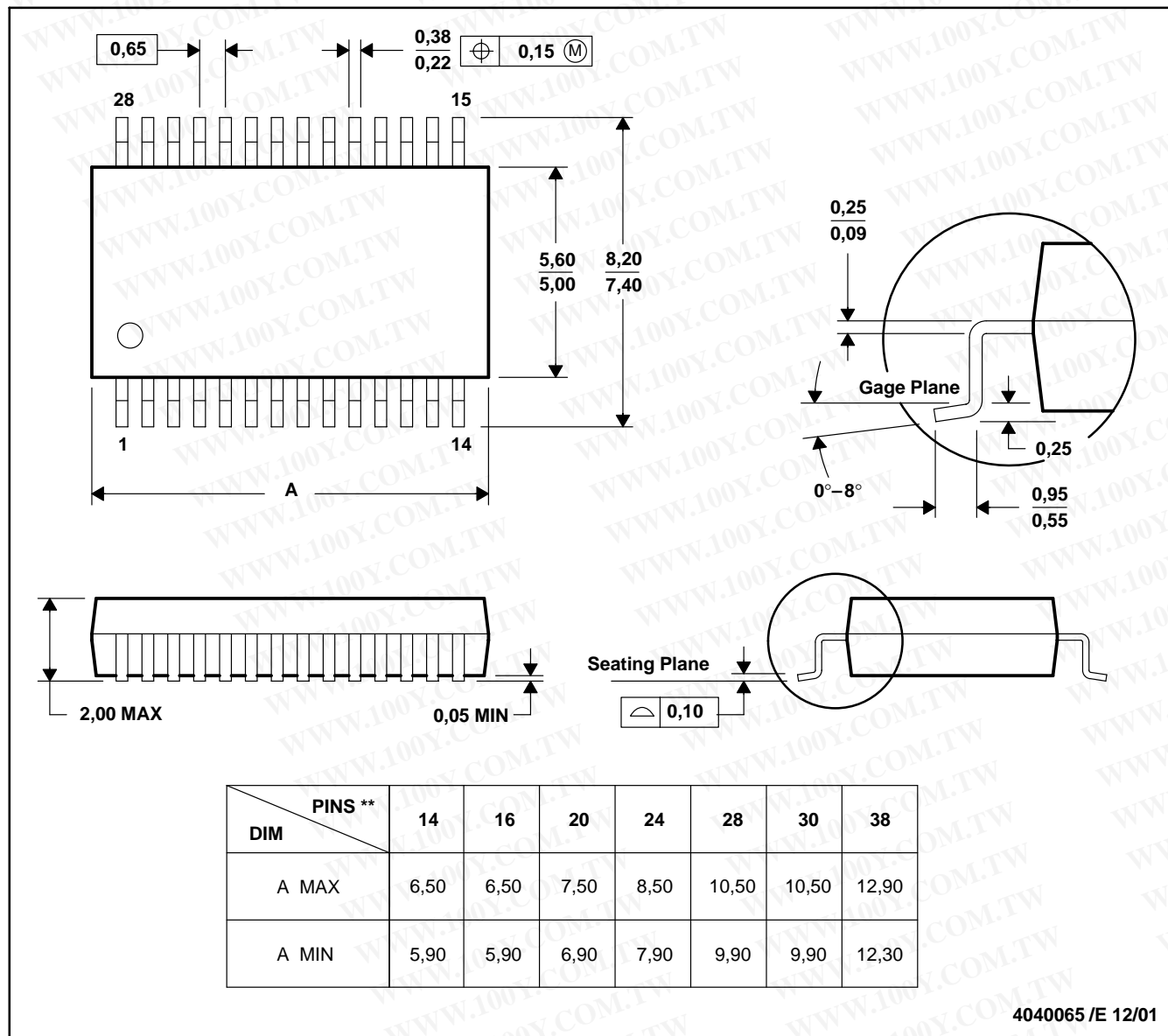


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



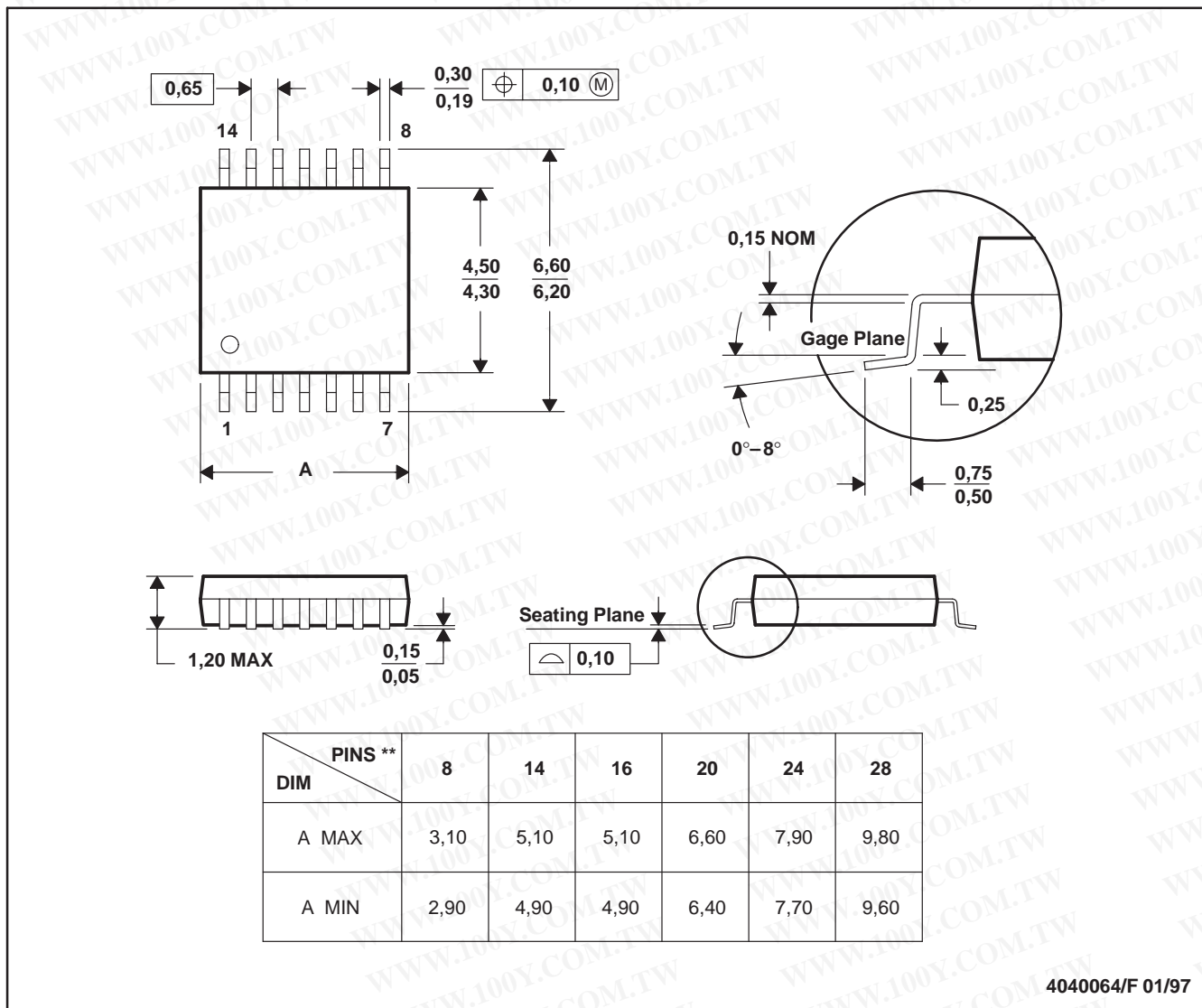
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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