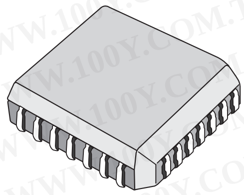
SGS-THOMSON MICROELECTRONICS

ST7537HS1

HOME AUTOMATION MODEM

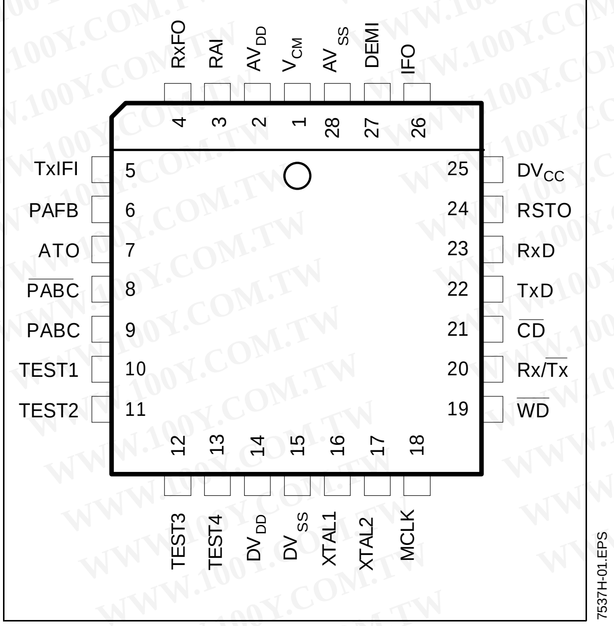
- HALF DUPLEX ASYNCHRONOUS 2400bps FSK MODEM
- Tx CARRIER FREQUENCY SYNTHESIZED FROM EXTERNAL CRYSTAL
- LOW DISTORTION Tx SIGNAL
- Rx SENSITIVITY BETTER THAN 1mV$_{RMS}$
- CARRIER DETECTION
- WATCH-DOG INPUT
- RESET AND MASTER CLOCK OUTPUTS FOR MICROCONTROLLER
- POWER AMPLIFIER BIAS CURRENT CONTROL (HIGH IMPEDANCE IN Rx MODE)
- SIMPLE AND ECONOMICAL APPLICATION SCHEMATICS
- COMPATIBLE WITH CENELEC EN 50065-1 AND FCC SPECIFICATION
- CARRIER DETECT CLAMPING ON RxD PROGRAMMABLE (ALLOWING DEMODULATION ON VERY LOW RECEIVE LEVEL, 1mV$_{RMS}$ TYPICALLY)



PLCC28
(Plastic Chip Carrier)

ORDER CODE : ST7537HS1

PIN CONNECTIONS



DESCRIPTION

The ST7537HS1 is a half duplex asynchronous FSK MODEM designed for home automation communication on the domestic electric mains which complies with the EN 50065-1 CENELEC standard.

It mainly operates from a 10V power supply and a 5V power supply for the microcontroller digital interface.

It is interfaced to the power line by an external driver, and a transformer (see Application Schematic Diagram). Its data transmission rate is 2400 bps and its carrier frequency is 132.45kHz.

PIN DESCRIPTION

Pin Name	Pin Number	Pin Type	Description
V_{CM}	1	Analog	Common Mode Voltage
AV_{DD}	2	Supply	Analog Power Supply : 10V ±5 %
RAI	3	Analog	Receive Analog Input
RxFO	4	Analog	Receive Filter Output
TxIFI	5	Analog	Transmit and Intermediate Frequency Filters Test Input (mode TEST3)
PAFB	6	Analog	Power Amplifier Feed-back Input
ATO	7	Analog	Analog Transmit Output
$\overline{PABC}$	8	Digital (10V)	Power Amplifier Bias Current Control Complementary Output
PABC	9	Digital (10V)	Power Amplifier Bias Current Control Output
TEST1	10	Digital	Tx to Rx Automatic Mode Switching Control Input
TEST2	11	Digital	Automatic Mode Switching Time and Watch-dog Time Reduction Control Input
TEST3	12	Digital	TxIFI Selection Input
TEST4	13	Digital	Undelayed Reset Input
DV_{DD}	14	Supply	Digital Power Supply : 10V ±5%
DV_{SS}	15	Supply	Digital Ground : 0V
XTAL1	16	Digital (10V)	Crystal Oscillator Input
XTAL2	17	Digital (10V)	Crystal Oscillator Output
MCLK	18	Digital	Master Clock Output
$\overline{WD}$	19	Digital	Watch-dog Input
Rx/Tx	20	Digital	Rx or Tx Mode Selection Input
$\overline{CD}$	21	Digital	Carrier Detect Output
TxD	22	Digital	Transmit Data Input
RxD	23	Digital	Receive Data Output
RSTO	24	Digital	Reset Output
DV_{CC}	25	Supply	Digital Buffers Supply Voltage : 5V ±5 %
IFO	26	Analog	Intermediate Frequency Filter Output
DEMI	27	Analog	Demodulator Input
AV_{SS}	28	Supply	Analog Ground : 0V

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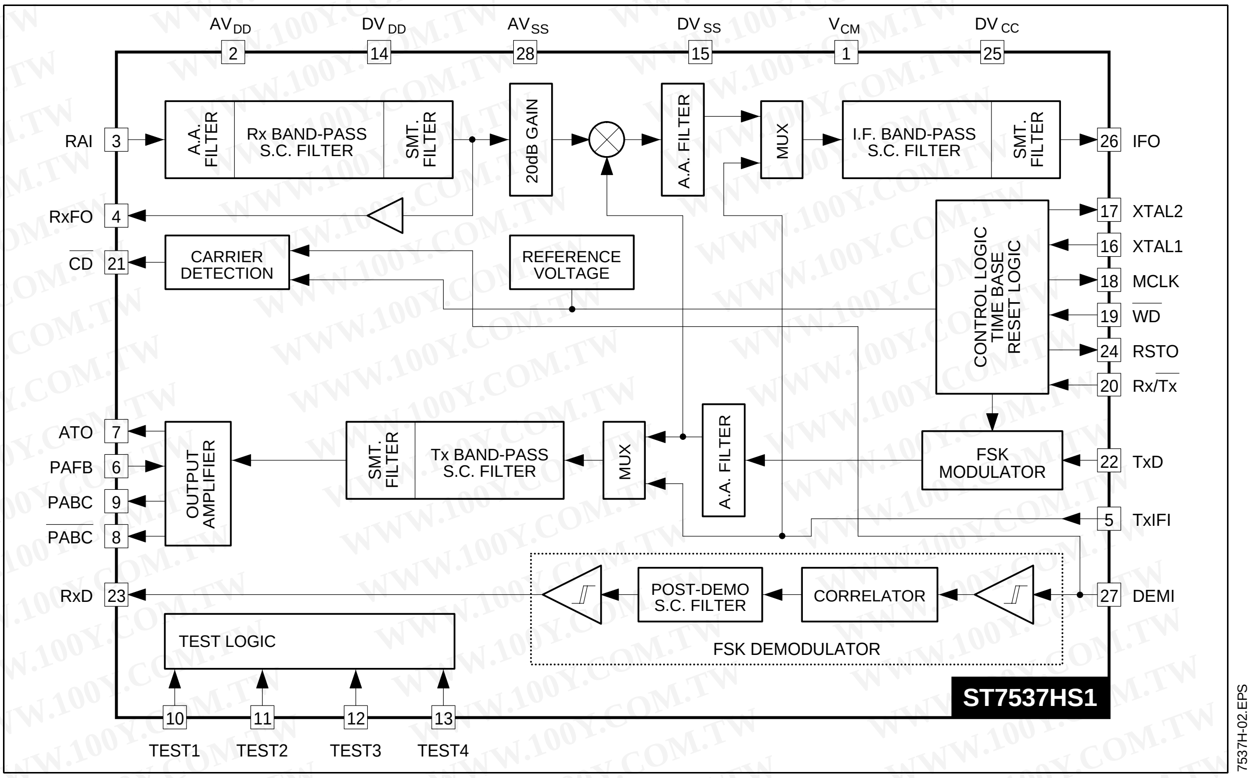
BLOCK DIAGRAM



TRANSMIT SECTION

The transmit mode is set when Rx/$\overline{Tx}$ = 0, if Rx/$\overline{Tx}$ is held at 0 longer than 1 second, then the device switches automatically in the Rx mode. A new activation of the Tx mode requires Rx/$\overline{Tx}$ to be returned to 1 for a minimum 2 microsecond period before being set to 0.

The Transmit Data (TxD) enter asynchronously the FSK modulator with a nominal intra-message data rate of 2400 bps.

The basic transmit frequencies are :
- f(TxD=0) = 133.05kHz
- f(TxD=1) = 131.85kHz

These frequencies are synthesized from a 11.0592MHz crystal oscillator; their precision is the same as the crystal one's (100ppm).

The modulated signal coming out of the FSK modulator is filtered by a switched-capacitor band-pass filter (Tx band-pass) in order to limit the output spectrum and to reduce the level of harmonic components.

The final stage of the Tx path consists of an operational amplifier which needs a feed-back signal (PAFB) from the power amplifier as shown on Application Schematic Diagram.

In Tx mode the Receive Data (RxD) signal is set to 1.

RECEIVE SECTION

The receive section is active when Rx/$\overline{Tx}$ = 1.

The Rx signal is applied on RAI and filtered by a band-pass switched capacitor filter (Rx band-pass) centered on the carrier frequency and whose bandwidth is around 12kHz.

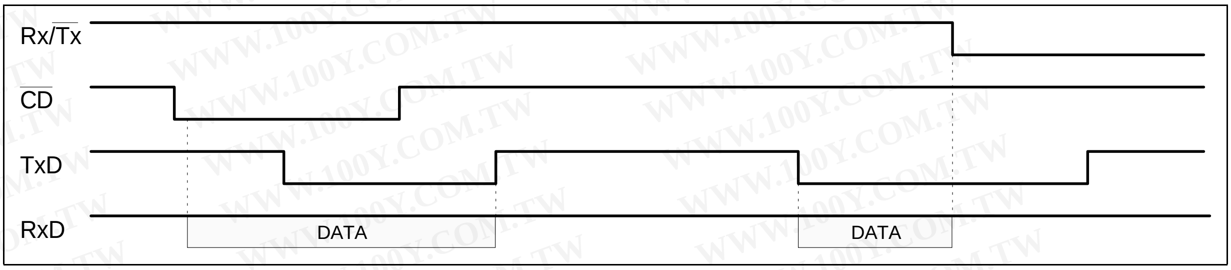
The Rx filter output is amplified by a 20dB gain stage which provides symetrical limitations for large voltage. The resulting signal is down-converted by a mixer which receives a local oscillator synthesized by the FSK modulator block. Finally an intermediate frequency band-pass filter (IF band-pass) whose central frequency is 5.4kHz improves the signal to noise ratio before entering the FSK demodulator.

The coupling of the intermediate frequency filter output (IFO) to the FSK demodulator input (DEMI) is made by an external capacitor C5 (100nF ±10%, 10V) which cancels the Rx path offset voltage.

The RxD output delivers the demodulated signal if the carrier detect ($\overline{CD}$) signal is low and is set to high level when $\overline{CD}$ = 1.

The RxD output can delivers the demodulated signal whatever the level of $\overline{CD}$ (0 or 1) if Rx/$\overline{Tx}$ = 1 and TxD = 0 (see Figure 1).

Figure 1 : Data Timing Chart



ADDITIONAL DIGITAL AND ANALOG FUNCTIONS

Time base

A time base section delivers all the internal clocks from a crystal oscillator (11.0592MHz). The crystal is connected between XTAL1 and XTAL2 pins and needs two external capacitors C3 and C4 (22pF ±10%, 10V) for proper operation.

Reset and watch-dog

The reset output (RSTO) is driven high when the supply voltage is lower than Vrh (typically 7.6V) with an hysteresis Vrh-Vrl (typically 300mV) or when no negative transition occurs on the watch-dog input (WD) for more than 1.5 second (see the timing chart on Figure 2). When a reset occurs RSTO is held high for at least 50ms.

Signal detection

The Carrier Detect output ($\overline{CD}$) is driven low when the input signal amplitude on RAI is greater than V_{CD} for at least T_{CD} (typically 6ms see the timing chart on Figure 3). When the input signal desappears or becomes lower than V_{CD}, $\overline{CD}$ is held low for at least Tcd before returning to a high level. V_{CD} is the carrier detection threshold voltage which is set internally to detect $5mV_{RMS}$ typically.

External power amplifier bias control

Two dedicated digital output (PABC and $\overline{PABC}$) delivering a signal between 0V and 10V are driven low respectively high, when the circuit is set in the receive mode (Rx/$\overline{Tx}$=1) or when the transmit mode time out (1 second) is exceeded; in the same time the output ATO is put in a high impedance state.

TESTING FEATURES

- An additionnal amplifier allows the observation of the Rx band-pass filter output on pin RxFO.
- A direct input to the Tx band-pass filter and to the IF filter (TxIFI) is selected when TEST3 = 1.
- The 1 second normal duration of the Tx to Rx mode automatic switching is reduced to 488µs and the 1.5 second watch-dog time out is reduced to 46.3µs when TEST2 = 1.
- When TEST1 = 1 the Tx to Rx mode automatic switching is desactivated and the functional mode of the circuit is fully controlled by Rx/$\overline{Tx}$.
- TEST4 is a reset input which allows an undelayed control of RSTO and of the internal state of the circuit.

POWER SUPPLIES WIRING PRECAUTIONS

The ST7537HS1 has two positive power supply terminals (AV_{DD},DV_{DD}) and two ground terminals (AV_{SS},DV_{SS}) in order to separate internal analog and digital supplies. The analog and digital terminals of each supply pair must be connected together externally for proper operation.

The V_{DD} must be protected against short-circuit for proper operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV_{DD}/DV_{DD}	Supply Voltage (1)	- 0.3, + 12	V
V_I	Digital Input Voltage	DV_{SS} - 0.3, DV_{DD} + 0.3	V
V_O	Digital Output Voltage (microcontroller interface)	DV_{SS} - 0.3, DV_{CC} + 0.3	V
V_O	Digital Output Voltage (PABC and $\overline{PABC}$)	DV_{SS} - 0.3, DV_{DD} + 0.3	V
I_O	Digital Output Current	- 5, + 5	mA
V_I	Analog Input Voltage	AV_{SS} - 0.3, AV_{DD} + 0.3	V
V_O	Analog Output Voltage	AV_{SS} - 0.3, AV_{DD} + 0.3	V
I_O	Analog Output Current	- 5, + 5	mA
P_D	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0, + 70	^oC
T_{stg}	Storage Temperature	- 55, + 150	^oC

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Notes :
1. The voltages are referenced to AV_{SS} and DV_{SS}.
2. Absolute maximum ratings are values beyond which damage to device may occur. Functional operation under these conditions is not implied.

GENERAL ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^oC \le T_{amb} \le 70^oC$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AV_{DD} DV_{DD}	Supply Voltage		9.5	10	10.5	V
AI_{DD} + DI_{DD}	Supply Current			30		mA
DV_{CC}	Digital Output Supply Voltage		4.75		5.25	V
DI_{CC}	Digital Output Supply Current			1.5		mA
V_{IH}	High Level Input Voltage	Digital Inputs	4.2			V
V_{IL}	Low Level Input Voltage	Digital Inputs			0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -100μA • Digital Outputs • Digital Outputs PABC and $\overline{PABC}$	 4.9 9.8			 V V
V_{OL}	Low Level Output Voltage	I_{OL} = 100μA • Digital Outputs • Digital Outputs PABC and $\overline{PABC}$			 0.1 0.2	 V V
DC	Duty Cycle	MCLK Output, C_L = 15pF	40		60	%

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TRANSMITTER ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^oC \le T_{amb} \le 70^oC$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VTAC	Max Carrier Output AC Voltage	R_L = 5.6kΩ $R_L(AV_{SS})$ = 5.6kΩ R(ATO, PAFB) = 1kΩ	0.8	1.0	1.3	V_{RMS}
HD2	Second Harmonic Distortion			- 50		dB
HD3	Third Harmonic Distortion			- 60		dB
FD	FSK Peak-to-peak Deviation			1200		Hz

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RECEIVER ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^oC \leq T_{amb} \leq 70^oC$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input Sensitivity			1	10	mV_{RMS}
V_{IN}	Maximum Input Signal				2	V_{RMS}
R_{IN}	Input Impedance		15			kΩ
GRx	Receive Gain	f = 132.45kHz		20		dB
BER	Bit Error Rate (1)	S/N = 15dB, S = 10mV_{RMS}, N : white		10^{-5}	10^{-3}	
t_{DEM}	Demodulation Time	Alternate 0 , 1 sequence		3		T bit
V_{CD}	Carrier Detection Level	f = 132.45kHz, sine wave		5	10	mV_{RMS}

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Note 1 : This parameter is guaranteed by correlation

ADDITIONAL DIGITAL AND ANALOG FUNCTIONS ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^oC \leq T_{amb} \leq 70^oC$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	High Level Reset Voltage	See Figure 2		7.9		V
V_{RL}	Low Level Reset Voltage	See Figure 2		7.6		V
t_{RST}	Reset Time	See Figure 2	50			ms
t_{WD}	Watch-dog Pulse Width	See Figure 2	500			ns
t_{WM}	Watch-dog Pulse Period	See Figure 2	800			µs
t_{OUT}	Watch-dog Time Out	See Figure 2			1.5	s
t_{CD}	Carrier Detection Time	See Figure 3	3		6.5	ms

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Figure 2 : Reset and Watch-dog Timing Chart

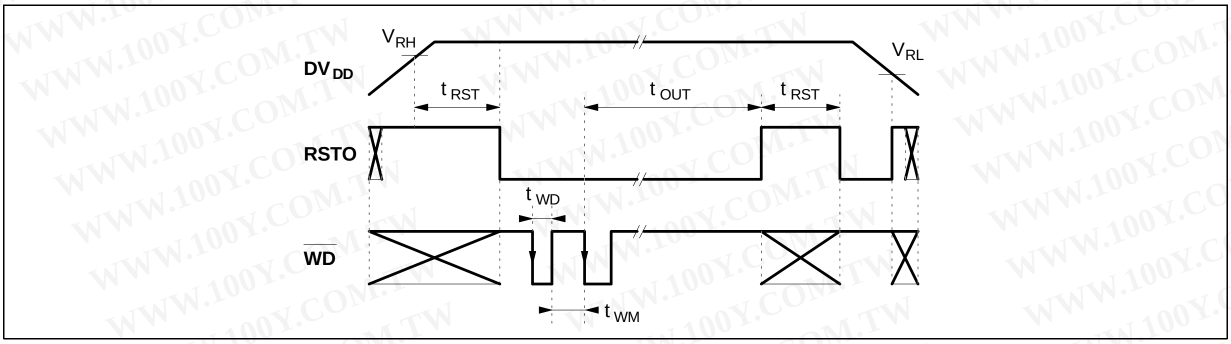
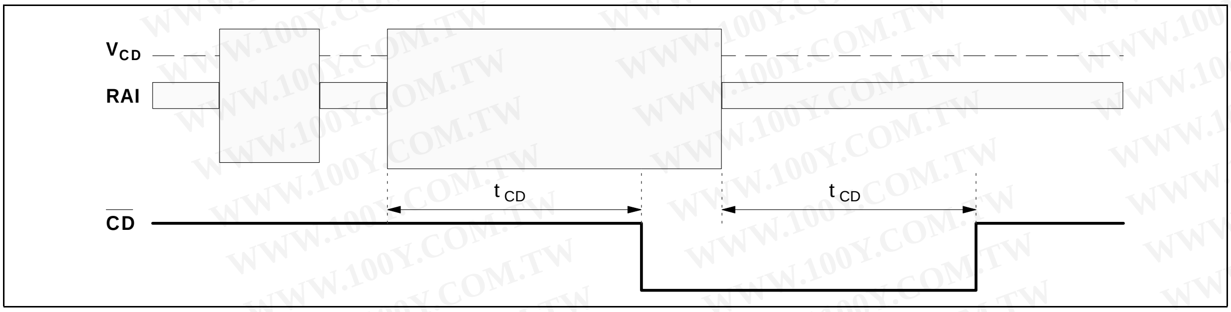


Figure 3 : Carrier Detection Timing Chart



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FILTER TEMPLATES

Receive and Transmit Filter

Frequency (kHz)	Gain (dB)		
	Min.	Typ.	Max.
92			- 30
126.45	- 5	- 3	- 2
Ref 132.45		0	
138.45	- 5	- 3	- 2
180			- 30

Intermediate FrequencyFilter

Frequency (kHz)	Gain (dB)		
	Min.	Typ.	Max.
2.4			- 35
4.3	- 4	- 3	- 1
Ref 5.4		0	
6.5	- 5	- 3	- 2
11.6			- 35

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APPLICATION SCHEMATIC INFORMATIONS

RESISTORS			CAPACITORS			
R1	180Ω		C1	1µF		Ceramic 50
R2	2.2Ω		C2	470nF		Paper, class X2
R3	2.2Ω		C3 (2)	22pF	10%	Ceramic 10V
R4	2.2Ω		C4 (2)	22pF	10%	Ceramic 10V
R5	2.2Ω		C5	100nF	10%	Ceramic 10V
R6	180Ω		C6	6.8nF	5%	Plastic Film 50V
R7	47kΩ		C7	100nF		Ceramic 10V
R8	1kΩ		C8	2.2µF		
R9	1kΩ	5%	C9	100nF		Ceramic 10V
R11	47kΩ		C10	2.2µF		
INDUCTOR			C11 (1)	100nF		Ceramic 10V
L1	10µH	≅ 1.5Ω	C12 (1)	100nF		Ceramic 10V
TRANSISTORS			**TRANSIL**			
Q1 : 2N2907 Q2 : 2N2222 Q3 : 2N2222 Q4 : 2N2907 Q5 : 2N2907 Q6 : 2N2222			TRL1 : SGS-THOMSON P6KE6V8CP **TRANSFORMER** TR1 : TOKO T1002 N **CRYSTAL** QTZ1 : 11.0592MHz parallel resonance			

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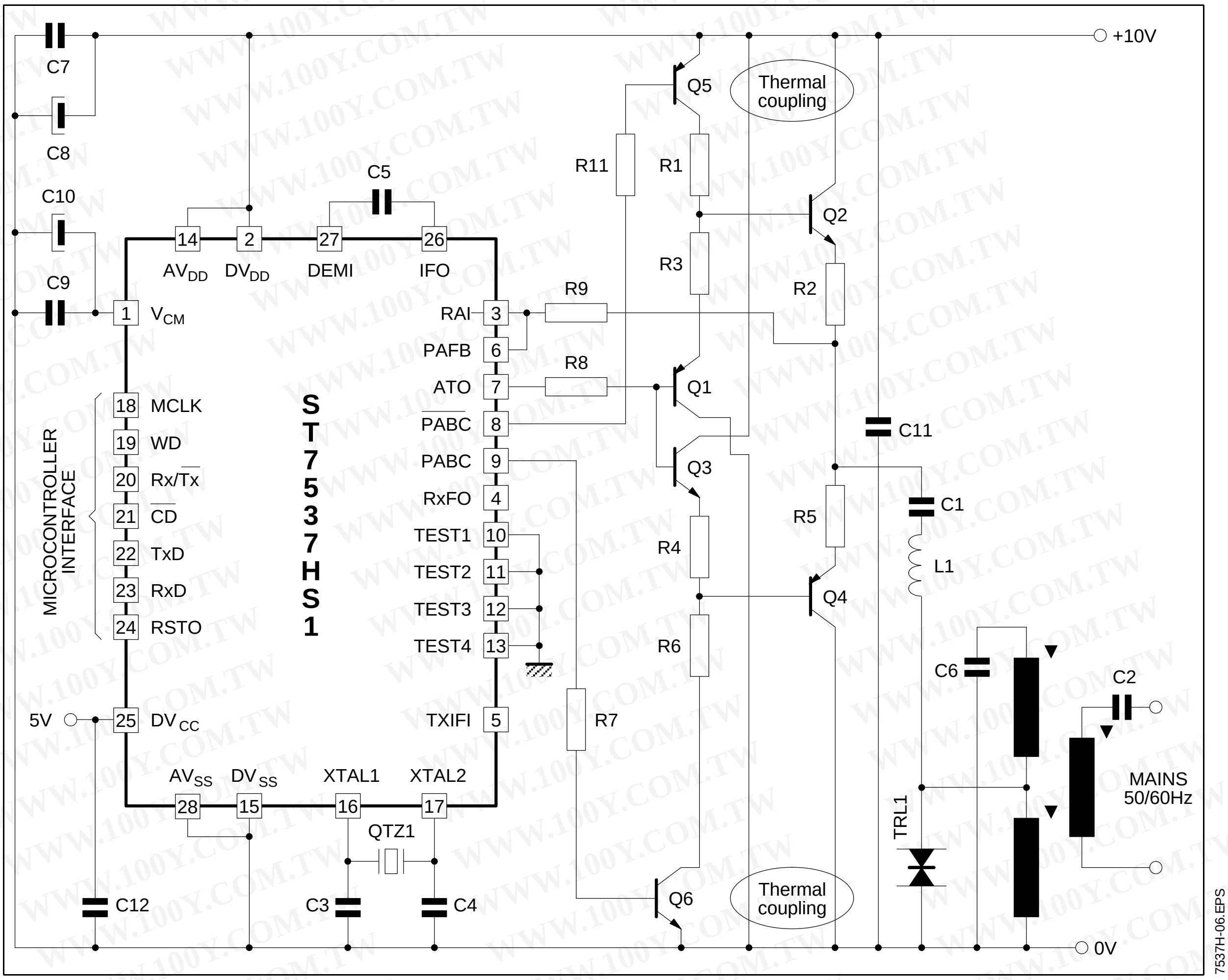
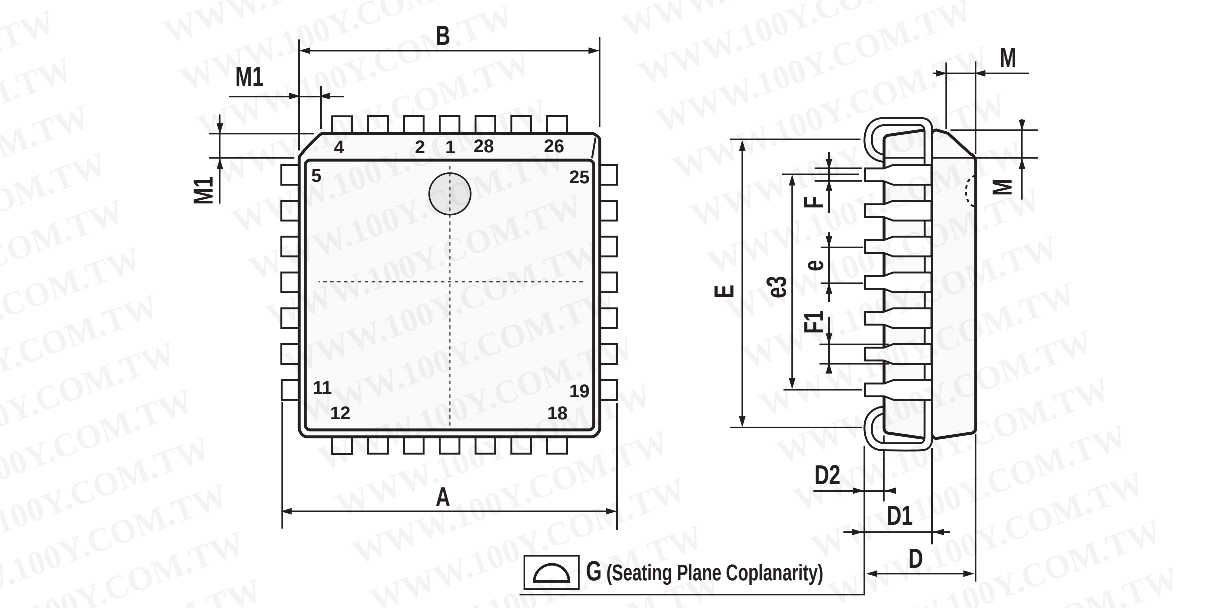
Notes :
1. These capacitors might not be necessary if the overall power supplies decoupling is sufficient.
2. The value of these capacitors depends on the crystal parameters.

APPLICATION SCHEMATIC DIAGRAM



PACKAGE MECHANICAL DATA

28 PINS - PLASTIC CHIP CARRIER



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

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