4 Mbit (512K x8) SuperFlash EEPROM

SST28SF040A / SST28VF040A

Data Sheet

FEATURES:

- **Single Voltage Read and Write Operations**
  - 4.5-5.5V-only for SST28SF040A
  - 2.7-3.6V for SST28VF040A
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Memory Organization: 512K x8**
- **Sector-Erase Capability: 256 Bytes per Sector**
- **Low Power Consumption**
  - Active Current: 15 mA (typical) for 5.0V and 10 mA (typical) for 2.7-3.6V
  - Standby Current: 5 µA (typical)
- **Fast Sector-Erase/Byte-Program Operation**
  - Byte-Program Time: 35 µs (typical)
  - Sector-Erase Time: 2 ms (typical)
  - Complete Memory Rewrite: 20 sec (typical)
- **Fast Read Access Time**
  - 4.5-5.5V-only operation: 90 and 120 ns
  - 2.7-3.6V operation: 150 and 200 ns
- **Latched Address and Data**
- **Hardware and Software Data Protection**
  - 7-Read-Cycle-Sequence Software Data Protection
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **TTL I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 20mm)
  - 32-pin PDIP

PRODUCT DESCRIPTION

The SST28SF/VF040A are 512K x8 bit CMOS Sector-Erase, Byte-Program EEPROMs. The SST28SF/VF040A are manufactured using SST's proprietary, high performance CMOS SuperFlash EEPROM Technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternative approaches. The SST28SF/VF040A erase and program with a single power supply. The SST28SF/VF040A conform to JEDEC standard pinouts for byte wide memories and are compatible with existing industry standard flash EEPROM pinouts.

Featuring high performance programming, the SST28SF/VF040A typically Byte-Program in 35 µs. The SST28SF/VF040A typically Sector-Erase in 2 ms. Both Program and Erase times can be optimized using interface features such as Toggle bit or Data# Polling to indicate the completion of the Write cycle. To protect against an inadvertent write, the SST28SF/VF040A have on chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST28SF/VF040A are offered with a guaranteed sector endurance of 10,000 cycles. Data retention is rated greater than 100 years.

The SST28SF/VF040A are best suited for applications that require re-programmable nonvolatile mass storage of program, configuration, or data memory. For all system applications, the SST28SF/VF040A significantly improve performance and reliability, while lowering power consumption when compared with floppy diskettes or EPROM approaches. Flash EEPROM technology makes possible convenient and economical updating of codes and control programs on-line. The SST28SF/VF040A improve flexibility, while lowering the cost of program and configuration storage application.

The functional block diagram shows the functional blocks of the SST28SF/VF040A. Figures 1, 2, and 3 show the pin assignments for the 32-lead PLCC, 32-lead TSOP, and 32-pin PDIP packages. Pin descriptions and operation modes are described in Tables 2 through 5.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first. Note, during the Software Data Protection sequence the addresses are latched on the rising edge of OE# or CE#, whichever occurs first.

Command Definitions

Table 4 contains a command list and a brief summary of the commands. The following is a detailed description of the operations initiated by each command.

Sector-Erase

The Sector-Erase operation erases all bytes within a sector and is initiated by a setup command and an execute command. A sector contains 256 Bytes. This sector erasability enhances the flexibility and usefulness of the SST28SF/VF040A, since most applications only need to change a small number of bytes or sectors, not the entire chip.

The setup command is performed by writing 20H to the device. The execute command is performed by writing D0H to the device. The Erase operation begins with the rising edge of the WE# or CE#, whichever occurs first and terminates automatically by using an internal timer. The End-of-Erase can be determined using either Data# Polling, Toggle Bit, or Successive Reads detection methods. See Figure 9 for timing waveforms.

The two-step sequence of a setup command followed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Sector-Erase Flowchart Description

Fast and reliable erasing of the memory contents within a sector is accomplished by following the Sector-Erase flowchart as shown in Figure 18. The entire procedure consists of the execution of two commands. The Sector-Erase operation will terminate after a maximum of 4 ms. A Reset command can be executed to terminate the Sector-Erase operation; however, if the Erase operation is terminated prior to the 4 ms time-out, the sector may not be fully erased. A Sector-Erase command can be reissued as many times as necessary to complete the Erase operation. The SST28SF/VF040A cannot be over-erased.

Chip-Erase

The Chip-Erase operation is initiated by a setup command (30H) and an execute command (30H). The Chip-Erase operation allows the entire array of the SST28SF/VF040A to be erased in one operation, as opposed to 2048 Sector-Erase operations. Using the Chip-Erase operation will minimize the time to rewrite the entire memory array. The Chip-Erase operation will terminate after a maximum of 20 ms. A Reset command can be executed to terminate the Erase operation; however, if the Chip-Erase operation is terminated prior to the 20 ms time-out, the chip may not be completely erased. If an erase error occurs a Chip-Erase command can be reissued as many times as necessary to complete the Chip-Erase operation. The SST28SF/VF040A cannot be over-erased. (See Figure 8)

Byte-Program

The Byte-Program operation is initiated by writing the setup command (10H). Once the program setup is performed, programming is executed by the next WE# pulse. See Figures 5 and 6 for timing waveforms. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first, and begins the Program operation. The Program operation is terminated automatically by an internal timer. See Figure 16 for the programming flowchart.

The two-step sequence of a setup command followed by an execute command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte-Program Flowchart Description

Programming data into the SST28SF/VF040A is accomplished by following the Byte-Program flowchart shown in Figure 16. The Byte-Program command sets up the byte for programming. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first and begins the Program operation. The end of program can be detected using either the Data# Polling, Toggle bit, or Successive reads.

Reset

The Reset command is provided as a means to safely abort the Erase or Program command sequences. Following either setup command (Erase or Program) with a write of FFH will safely abort the operation. Memory contents will not be altered. After the Reset command, the device returns to the Read mode. The Reset command does not enable Software Data Protection. See Figure 7 for timing waveforms.

Read

The Read operation is initiated by setting CE#, and OE# to logic low and setting WE# to logic high (See Table 3). See Figure 4 for Read cycle timing waveform. The Read operation from the host retrieves data from the array. The device remains enabled for Read until another operation mode is accessed. During initial power-up, the device is in the Read mode and is Software Data protected. The device must be unprotected to execute a Write command.

The Read operation of the SST28SF/VF040A are controlled by OE# and CE# at logic low. When CE # is high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when CE# or OE# are high.

Read-ID

The Read-ID operation is initiated by writing a single command (90H). A read of address 0000H will output the manufacturer's ID (BFH). A read of address 0001H will output the device ID (04H). Any other valid command will terminate this operation.

Data Protection

In order to protect the integrity of nonvolatile data storage, the SST28SF/VF040A provide both

hardware and software features to prevent inadvertent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Data Protection

The SST28SF/VF040A are designed with hardware features to prevent inadvertent writes. This is done in the following ways:

1. Write Cycle Inhibit Mode: OE# low, CE#, or WE# high will inhibit the Write operation.
2. Noise/Glitch Protection: A WE# pulse width of less than 5 ns will not initiate a Write cycle.
3. V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 2.0V.
4. After power-up, the device is in the Read mode and the device is in the Software Data Protect state.

Software Data Protection (SDP)

The SST28SF/VF040A have software methods to further prevent inadvertent writes. In order to perform an Erase or Program operation, a two-step command sequence consisting of a set-up command followed by an execute command avoids inadvertent erasing and programming of the device.

The SST28SF/VF040A will default to Software Data Protection after power up. A sequence of seven consecutive reads at specific addresses will unprotect the device The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising edge of OE# or CE#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also refer to Figures 10 and 11 for the 7 Read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tri-state).

Write Operation Status Detection

The SST28SF/VF040A provide three means to detect the completion of a Write operation, in order to optimize the system Write operation. The end of a Write operation (Erase or Program) can be detected by three means: 1) monitoring the Data# Polling bit, 2) monitoring the Toggle bit, or 3) by two successive reads of the same data. These three detection mechanisms are described below.

The actual completion of the nonvolatile Write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with the DQ used. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both Reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

The SST28SF/VF040A feature Data# Polling to indicate the Write operation status. During a Write operation, any attempt to read the last byte loaded during the byte-load cycle will receive the complement of the true data on DQ_7. Once the Write cycle is completed, DQ_7 will show true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. See Figure 12 for Data# Polling timing waveforms. In order for Data# Polling to function correctly, the byte being polled must be erased prior to programming.

Toggle Bit (DQ_6)

An alternative means for determining the Write operation status is by monitoring the Toggle Bit, DQ_6. During a Write operation, consecutive attempts to read data from the device will result in DQ_6 toggling between logic 0 (low) and logic 1 (high). When the Write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 13 for Toggle Bit timing waveforms.

Successive Reads

An Alternative means for determining an end of a Write operation is by reading the same address for two consecutive data matches.

Product Identification

The Product Identification mode identifies the device as SST28SF/VF040A and the manufacturer as SST. This mode may be accessed by hardware and software operations. The hardware operation is typically used by an external programmer to identify the correct algorithm for the SST28SF/VF040A. Users may wish to use the software operation to identify the device (i.e., using the device ID). For details see Table 3 for the hardware operation and Figure 19 for the software operation. The manufacturer's and device IDs are the same for both operations.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST28SF/VF040A	0001H	04H

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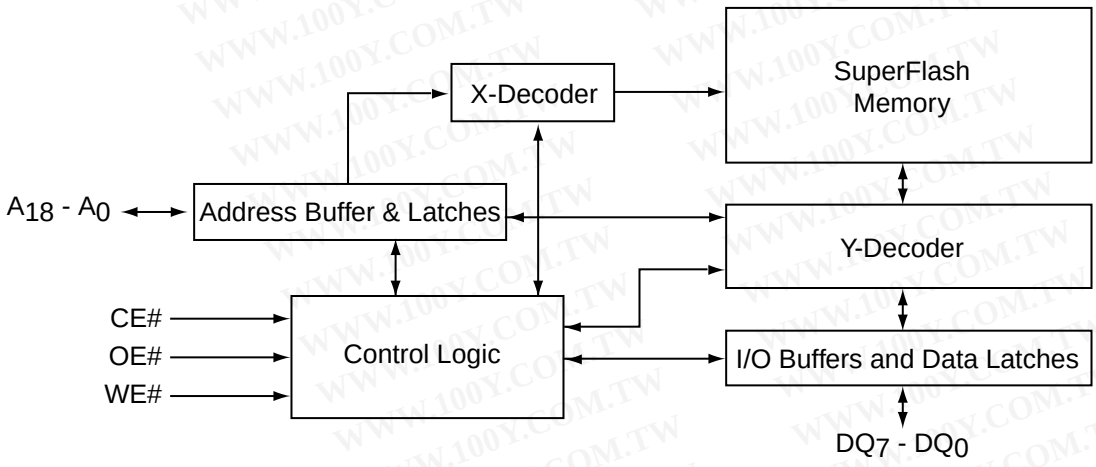
FUNCTIONAL BLOCK DIAGRAM



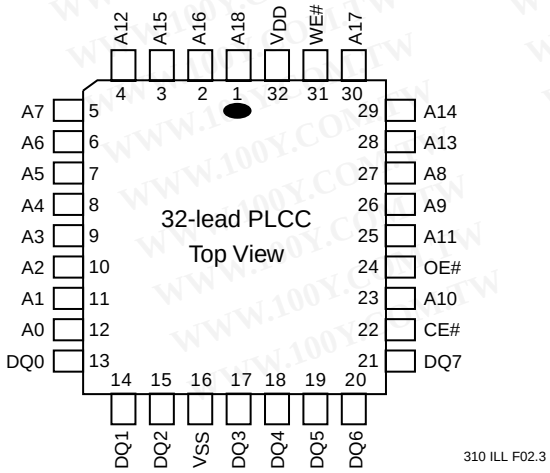


FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD PLCC

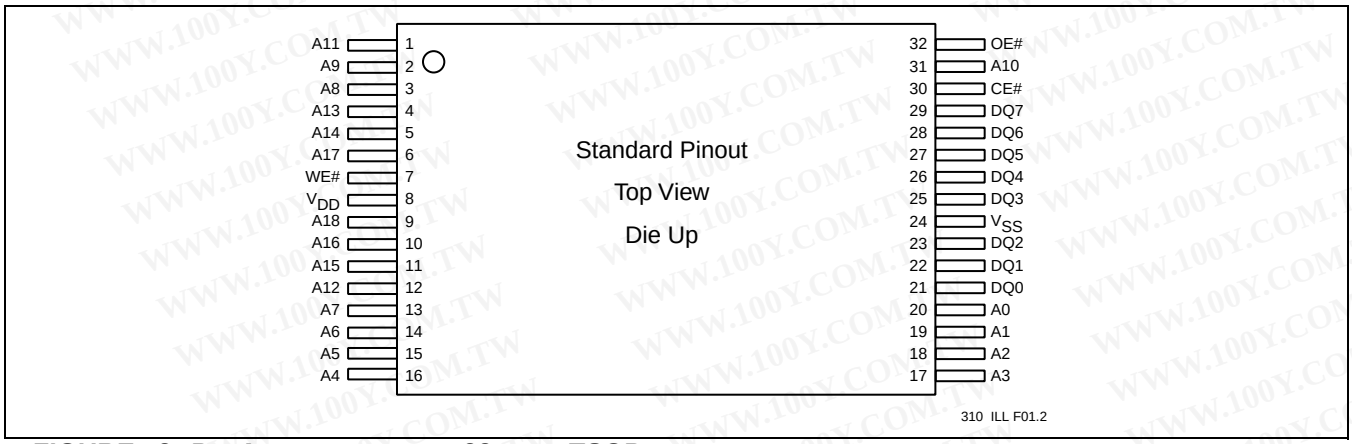


FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD TSOP

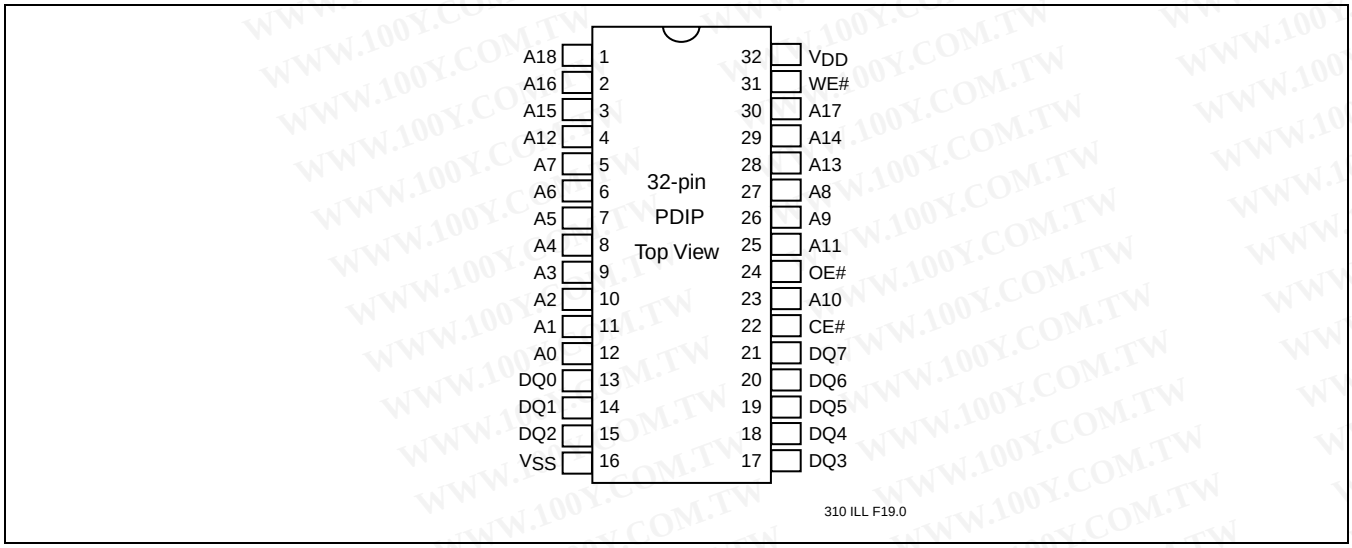


FIGURE 3: PIN ASSIGNMENTS FOR 32-PIN PDIP

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{18}-A_8	Row Address Inputs	To provide memory addresses. Row addresses define a sector.
A_7-A_0	Column Address Inputs	Selects the byte within the sector
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.[1]
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.[1]
V_{DD}	Power Supply	To provide: 5.0V supply (4.5-5.5V) for SST28SF040A 2.7V supply (2.7-3.6V) for SST28VF040A
V_{SS}	Ground	

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1. This pin has an internal pull-up resistor.

TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Byte-Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Sector-Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Standby	V_{IH}	X[1]	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip-Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer's ID (BFH) Device ID (04H)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IL} A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IH}
Software Mode	V_{IL}	V_{IL}	V_{IH}		See Table 4
SDP Enable & Disable Mode	V_{IL}	V_{IL}	V_{IH}		See Table 4
Reset	V_{IL}	V_{IH}	V_{IL}		See Table 4

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1. X can be V_{IL} or V_{IH}, but no other value.

TABLE 4: SOFTWARE COMMAND SUMMARY

	Required	Setup Command Cycle			Execute Command Cycle			
Command Summary	Cycle(s)	Type[1]	Addr[2,3]	Data[4]	Type[1]	Addr[2,3]	Data[4]	SDP[5]
Sector-Erase	2	W	X	20H	W	SA	D0H	N
Byte-Program	2	W	X	10H	W	PA	PD	N
Chip-Erase[6]	2	W	X	30H	W	X	30H	N
Reset	1	W	X	FFH				Y
Read-ID	2	W	X	90H	R	7	7	Y
Software Data Protect	7	R	8					
Software Data Unprotect	7	R	9					

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1. Type definition: W = Write, R = Read, X can be V_{IL} or V_{IH}, but no other value.
2. Addr (Address) definition: SA = Sector Address = A_{18}-A_8, sector size = 256 Bytes; A_7-A_0 = X for this command.
3. Addr (Address) definition: PA = Program Address = A_{18}-A_0.
4. Data definition: PD = Program Data, H = number in hex.
5. SDP = Software Data Protect mode using 7 Read Cycle Sequence.
   a) Y = the operation can be executed with protection enabled
   b) N = the operation cannot be executed with protection enabled
6. The Chip-Erase function is not supported on industrial temperature parts.
7. Address 0000H retrieves the Manufacturer's ID of BFH and address 0001H retrieves the Device ID of 04H.
8. Refer to Figure 11 for the 7 Read Cycle sequence for Software-Data-Protect.
9. Refer to Figure 10 for the 7 Read Cycle sequence for Software-Data-Unprotect.

TABLE 5: MEMORY ARRAY DETAIL

Sector Select	Byte Select
A_{18} - A_8	A_7 - A_0

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Voltage on A_9 Pin to Ground Potential . . . . . -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hold Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 100 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE FOR SST28SF040A

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	4.5-5.5V
Industrial	-40°C to +85°C	4.5-5.5V

OPERATING RANGE FOR SST28VF040A

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 10 ns
Output Load . . . . . 1 TTL Gate and C_L = 100 pF for SST28SF040A
C_L = 100 pF for SST28VF040A
See Figures 14 and 15

TABLE 6: DC OPERATING CHARACTERISTICS FOR SST28SF040A

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input=V_{ILT}/V_{IHT}, at f=1/T_{RC} Min, $V_{DD}=V_{DD}$ Max
	Read		32	mA	CE#=OE#=V_{IL}, WE#=V_{IH}, all I/Os open
	Program and Erase		40	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, $V_{DD}=V_{DD}$ Max
I_{SB1}	Standby V_{DD} Current (TTL input)		3	mA	CE#=V_{IH}, $V_{DD}=V_{DD}$ Max
I_{SB2}	Standby V_{DD} Current (CMOS input)		20	µA	CE#=V_{DD}-0.3V, $V_{DD}=V_{DD}$ Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
V_{IL}	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
V_{IH}	Input High Voltage	2.0		V	$V_{DD}=V_{DD}$ Max
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=2.1 mA, $V_{DD}=V_{DD}$ Min
V_{OH}	Output High Voltage	2.4		V	I_{OH}=-400 µA, $V_{DD}=V_{DD}$ Min
V_H	Supervoltage for A_9	11.6	12.4	V	CE#=OE#=V_{IL}, WE#=V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL}, WE#=V_{IH}, $A_9=V_H$ Max

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TABLE 7: DC OPERATING CHARACTERISTICS FOR SST28VF040A

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input=V_{ILT}/V_{IHT}, at f=1/T_{RC} Min, $V_{DD}=V_{DD}$ Max
	Read		10	mA	CE#=OE#=V_{IL}, WE#=V_{IH}, all I/Os open
	Program and Erase		25	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, $V_{DD}=V_{DD}$ Max
I_{SB2}	Standby V_{DD} Current (CMOS input)		20	µA	CE#=OE#=WE#=V_{DD}-0.3V, $V_{DD}=V_{DD}$ Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
V_{IL}	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
V_{IH}	Input High Voltage	2.0		V	$V_{DD}=V_{DD}$ Max
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=100 µA, $V_{DD}=V_{DD}$ Min
V_{OH}	Output High Voltage	2.4		V	I_{OH}=-100 µA, $V_{DD}=V_{DD}$ Min
V_H	Supervoltage for A_9	11.6	12.4	V	CE#=OE#=V_{IL}, WE#=V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL}, WE#=V_{IH}, $A_9=V_H$ Max

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TABLE 8: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	10	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	10	ms

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 11: READ CYCLE TIMING PARAMETERS FOR SST28SF040A

IEEE Symbol	Industry Symbol	Parameter	SST28SF040A-90		SST28SF040A-120		Units
			Min	Max	Min	Max	
tAVAV	T_{RC}	Read Cycle Time	90		120		ns
tAVQV	T_{AA}	Address Access Time		90		120	ns
tELQV	T_{CE}	Chip Enable Access Time		90		120	ns
tGLQV	T_{OE}	Output Enable Access Time		45		50	ns
tEHQZ	T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
tGHQZ	T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
tELQX	T_{CHZ}[1]	CE# High to High-Z Output		20		30	ns
tGLQX	T_{OHZ}[1]	OE# High to High-Z Output		20		30	ns
tAXQX	T_{OH}[1]	Output Hold from Address Change	0		0		ns

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12: READ CYCLE TIMING PARAMETERS FOR SST28VF040A

IEEE Symbol	Industry Symbol	Parameter	SST28VF040A-150		SST28VF040A-200		Units
			Min	Max	Min	Max	
tAVAV	T_{RC}	Read Cycle Time	150		200		ns
tAVQV	T_{AA}	Address Access Time		150		200	ns
tELQV	T_{CE}	Chip Enable Access Time		150		200	ns
tGLQV	T_{OE}	Output Enable Access Time		75		100	ns
tEHQZ	T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
tGHQZ	T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
tELQX	T_{CHZ}[1]	CE# High to High-Z Output		40		60	ns
tGLQX	T_{OHZ}[1]	OE# High to High-Z Output		40		60	ns
tAXQX	T_{OH}[1]	Output Hold from Address Change	0		0		ns

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 13: ERASE/PROGRAM CYCLE TIMING PARAMETERS

IEEE Symbol	Industry Symbol	Parameter	SST28SF040A		SST28VF040A		Units
			Min	Max	Min	Max	
tAVA	T_{BP}	Byte-Program Cycle Time		40		40	µs
tWLWH	T_{WP}	Write Pulse Width (WE#)	90		100		ns
tAVWL	T_{AS}	Address Setup Time	10		10		ns
tWLAX	T_{AH}	Address Hold Time	50		100		ns
tELWL	T_{CS}	CE# Setup Time	0		0		ns
tWHEX	T_{CH}	CE# Hold Time	0		0		ns
tGHWL	T_{OES}	OE# High Setup Time	10		20		ns
tWGL	T_{OEH}	OE# High Hold Time	10		20		ns
tWLEH	T_{CP}	Write Pulse Width (CE#)	90		100		ns
tDVWH	T_{DS}	Data Setup Time	50		100		ns
tWHDX	T_{DH}	Data Hold Time	10		20		ns
tWHWL2	T_{SE}	Sector-Erase Cycle Time		4		4	ms
	T_{RST}[1]	Reset Command Recovery Time		4		4	µs
tWHWL3	T_{SCE}	Software Chip-Erase Cycle Time		20		20	ms
tEHEL	T_{CPH}	CE# High Pulse Width	50		50		ns
tWHWL1	T_{WPH}	WE# High Pulse Width	50		50		ns
	T_{PCP}[1]	Protect CE# or OE# Pulse Width	50		50		ns
	T_{PCH}[1]	Protect CE# or OE# High Time	50		50		ns
	T_{PAS}[1]	Protect Address Setup Time	40		40		ns
	T_{PAH}[1]	Protect Address Hold Time	0		0		ns

T13.6 310

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

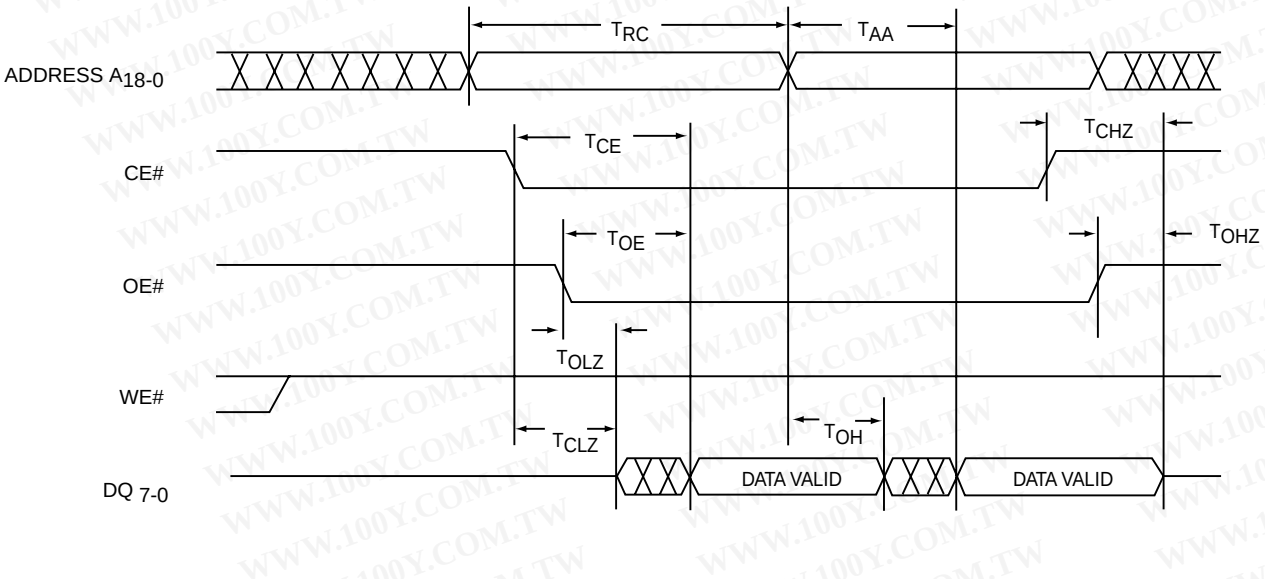


FIGURE 4: READ CYCLE TIMING DIAGRAM

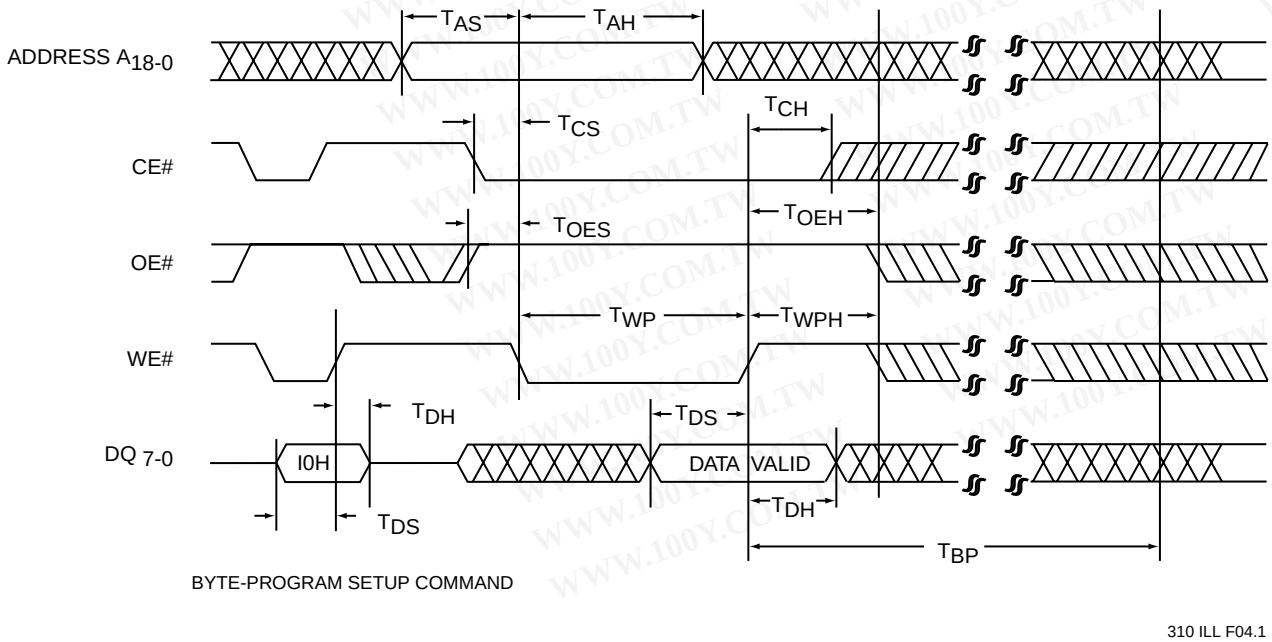


FIGURE 5: WE# CONTROLLED BYTE-PROGRAM CYCLE TIMING DIAGRAM

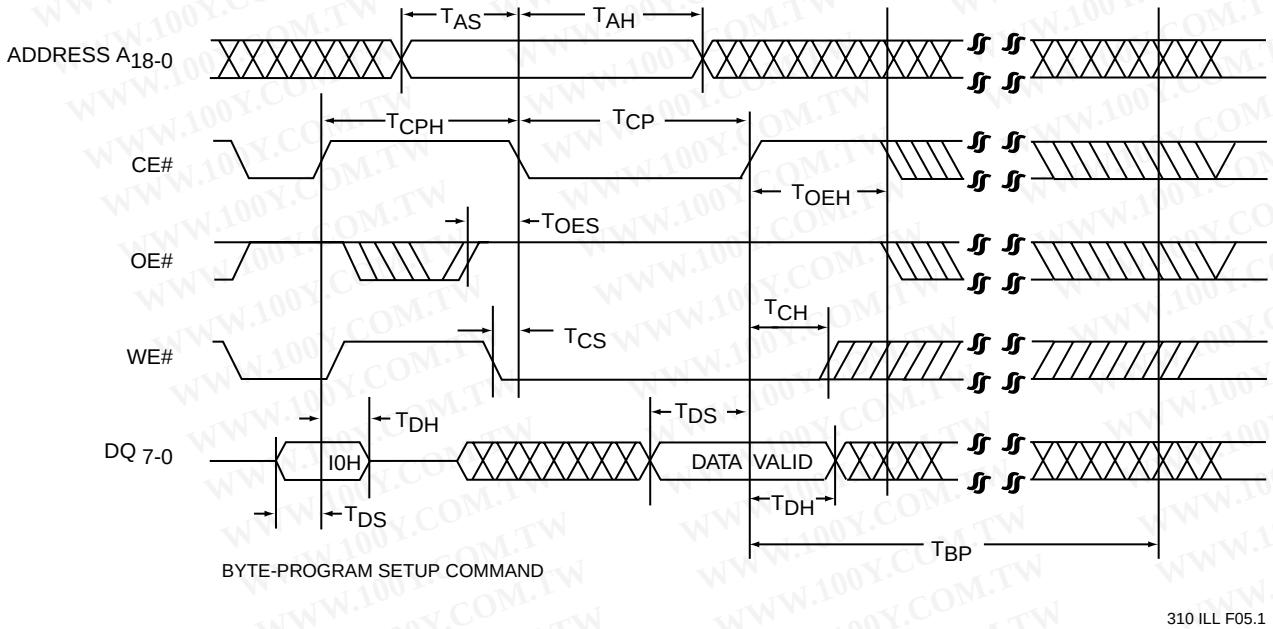


FIGURE 6: CE# CONTROLLED BYTE-PROGRAM CYCLE TIMING DIAGRAM

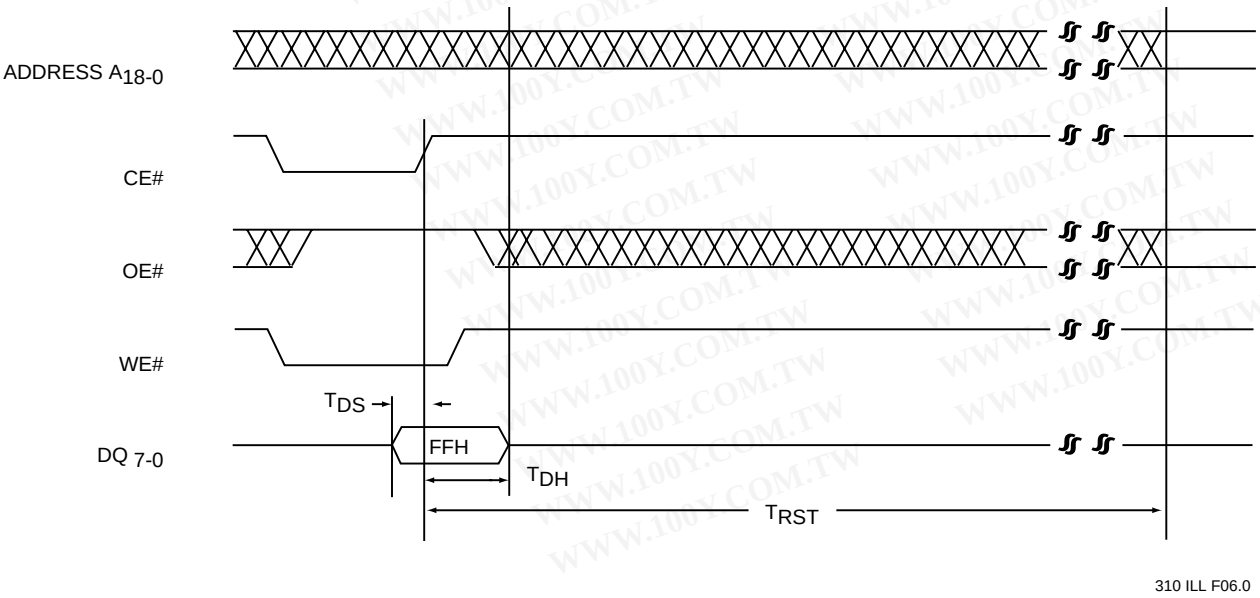


FIGURE 7: RESET COMMAND TIMING DIAGRAM

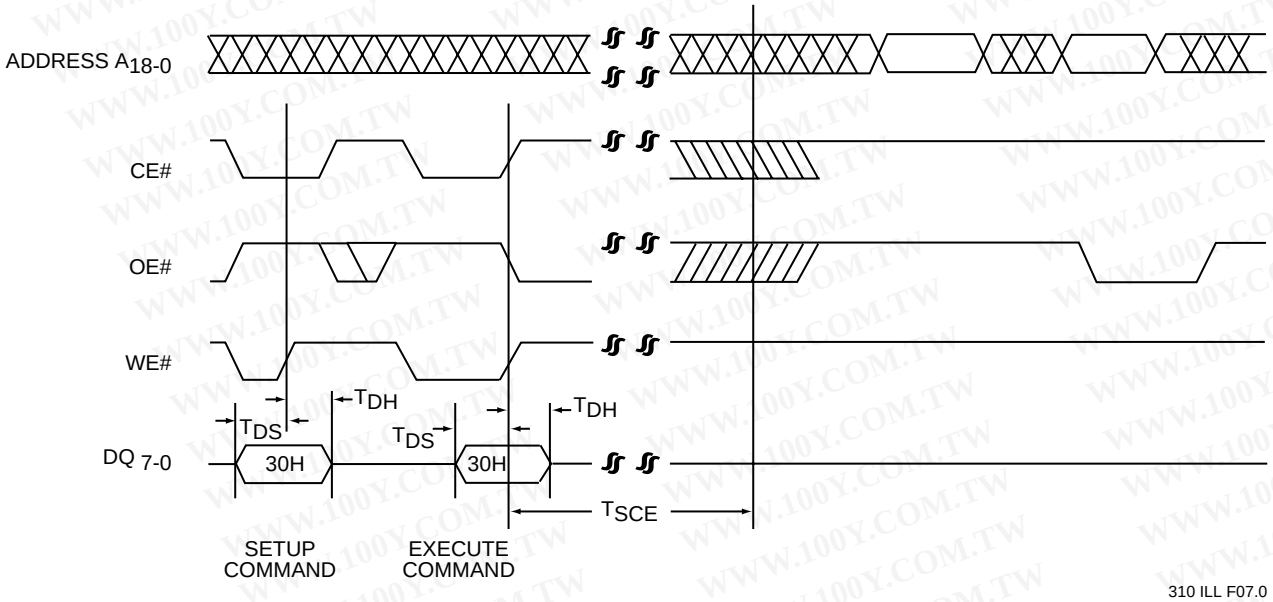


FIGURE 8: CHIP-ERASE TIMING DIAGRAM

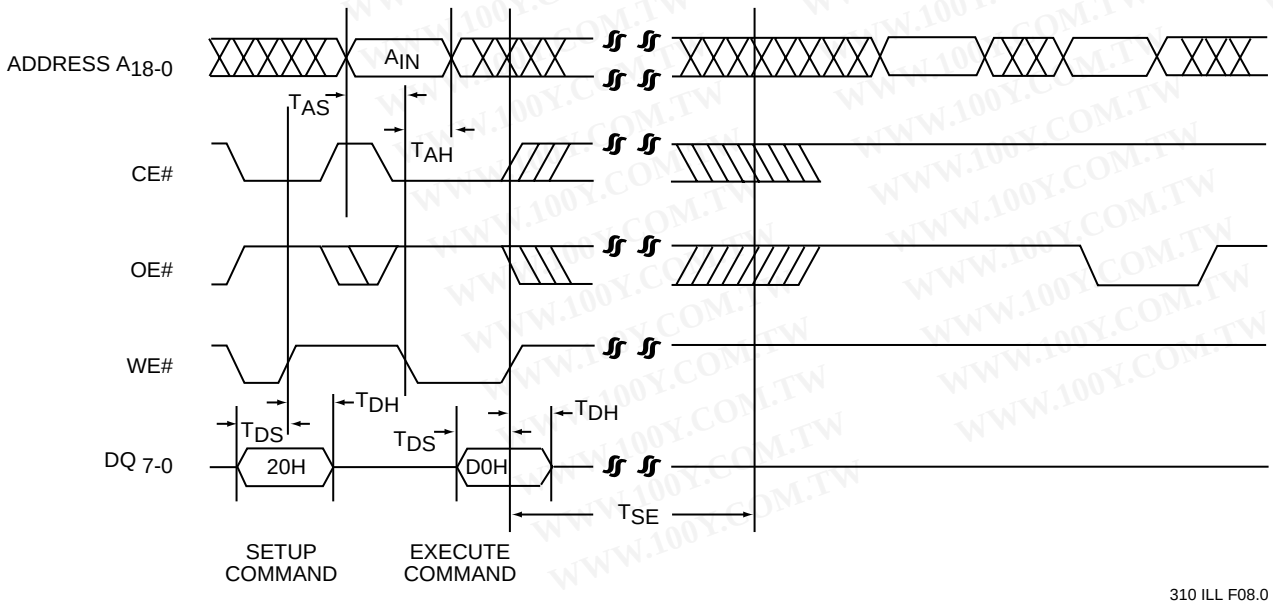
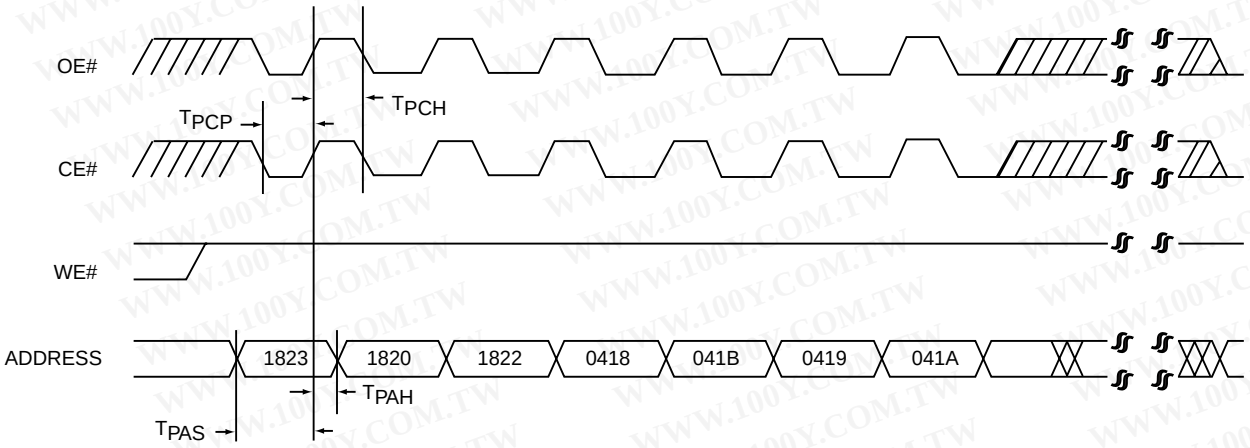


FIGURE 9: SECTOR-ERASE TIMING DIAGRAM



NOTE: A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A12 ARE "DON'T CARE"

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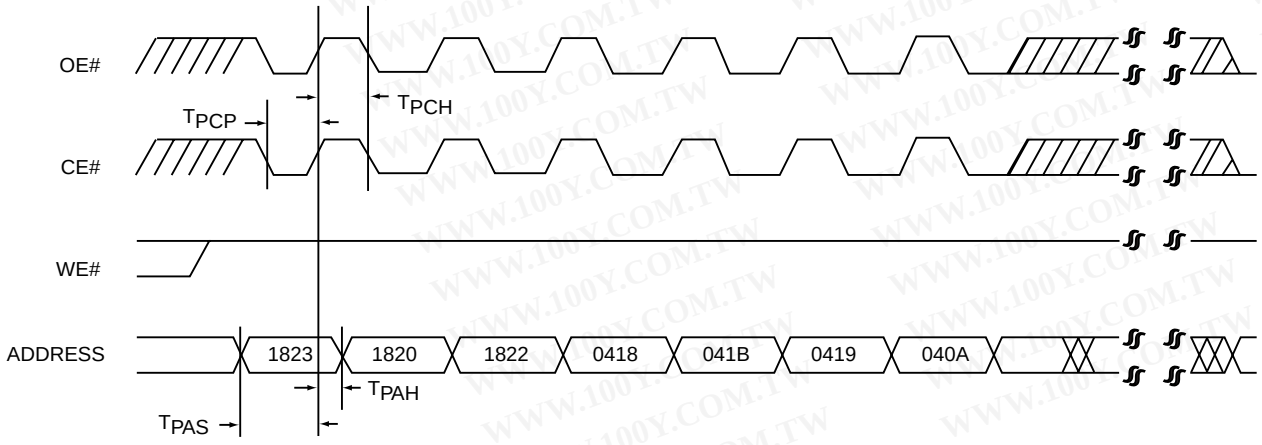
FIGURE 10: SOFTWARE DATA UNPROTECT DISABLE TIMING DIAGRAM



NOTE: A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

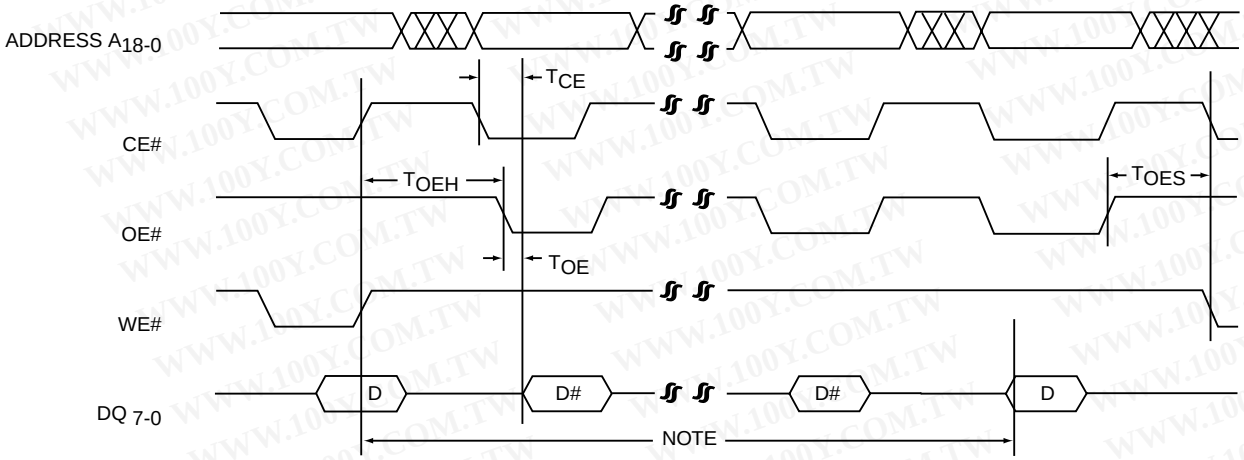
1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A12 ARE "DON'T CARE"

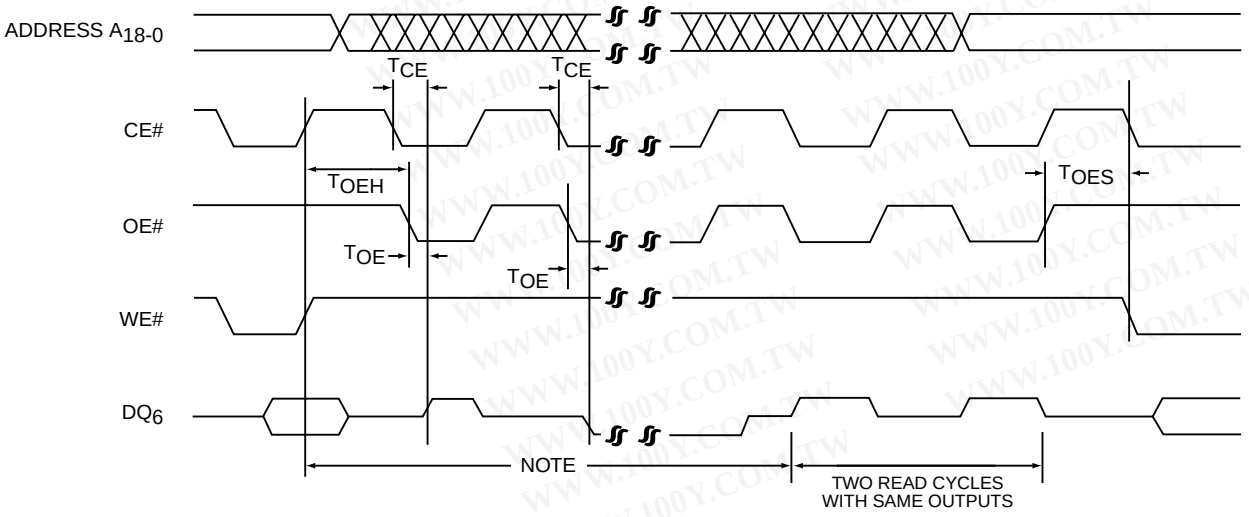
310 ILL F10.4

FIGURE 11: SOFTWARE DATA PROTECT DISABLE TIMING DIAGRAM



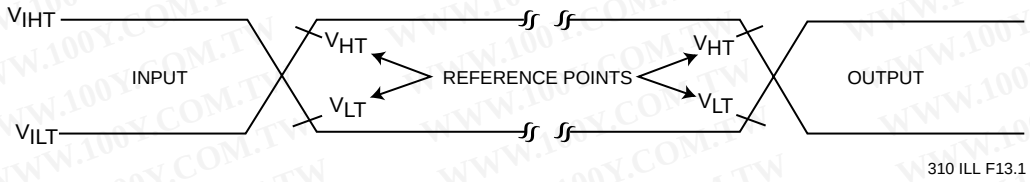
NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} or T_{BP} DEPENDING UPON THE SELECTED OPERATION MODE.

FIGURE 12: DATA# POLLING TIMING DIAGRAM



NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} or T_{BP} DEPENDING UPON THE SELECTED OPERATION MODE.

FIGURE 13: TOGGLE BIT TIMING DIAGRAM



AC test inputs are driven at V_{IHT} (2.4V) for a logic "1" and V_{ILT} (0.4 V) for a logic "0". Measurement reference points for inputs and outputs are V_{HT} (2.0 V) and V_{LT} (0.8 V). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 14: AC INPUT/OUTPUT REFERENCE WAVEFORMS

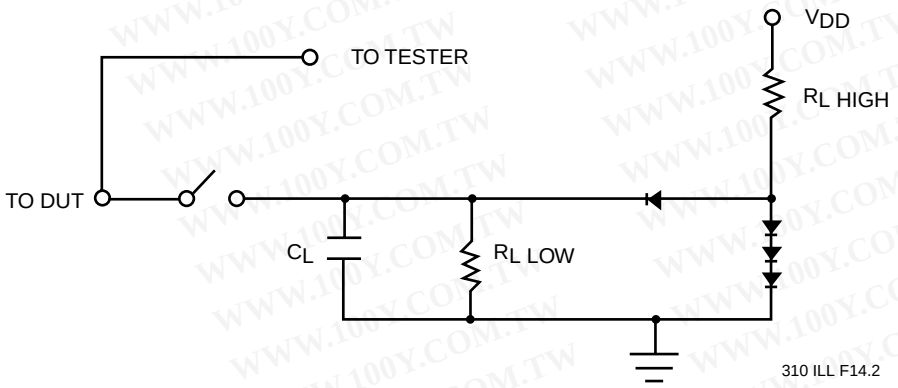


FIGURE 15: A TEST LOAD EXAMPLE

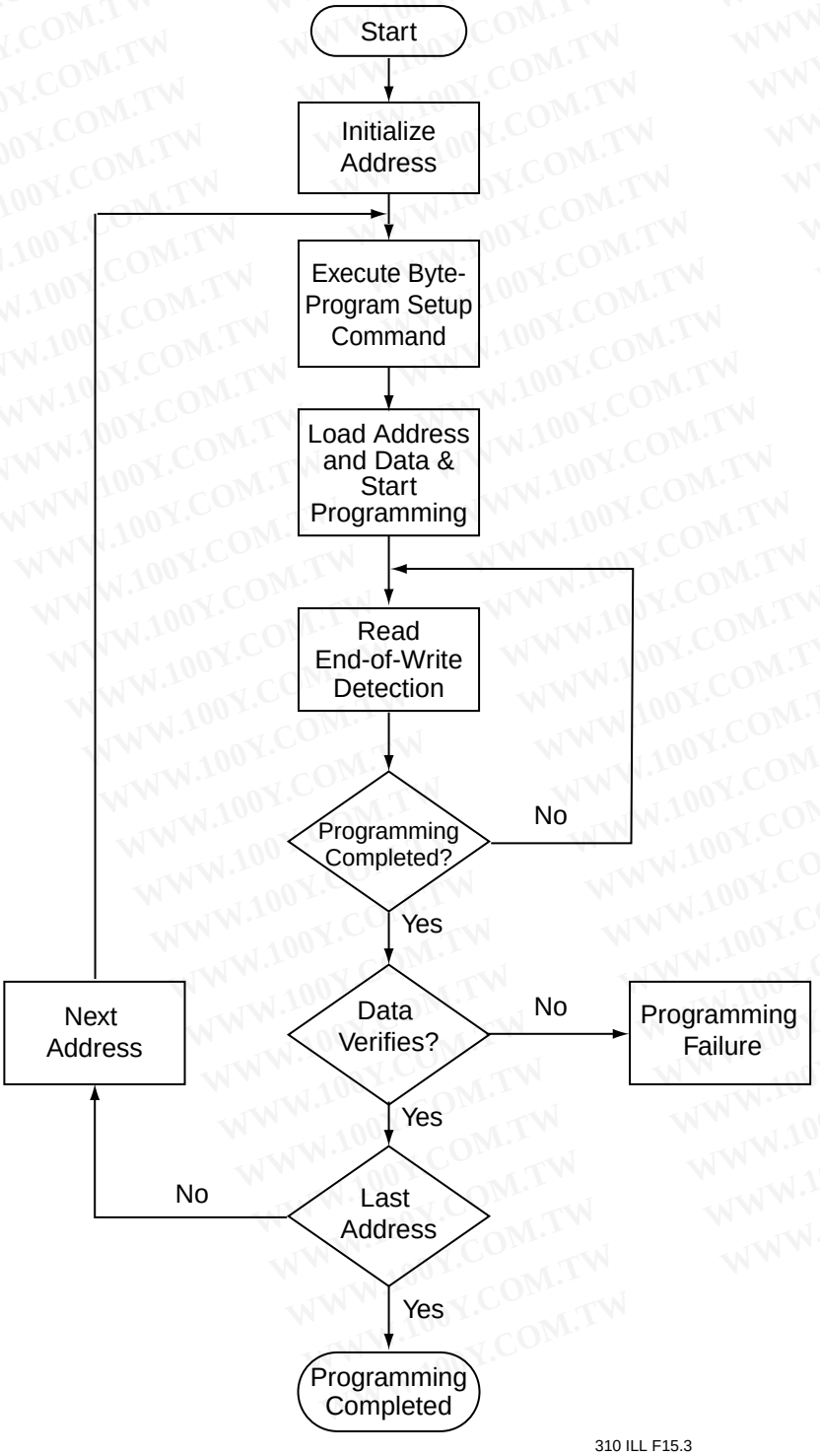


FIGURE 16: BYTE-PROGRAM FLOWCHART

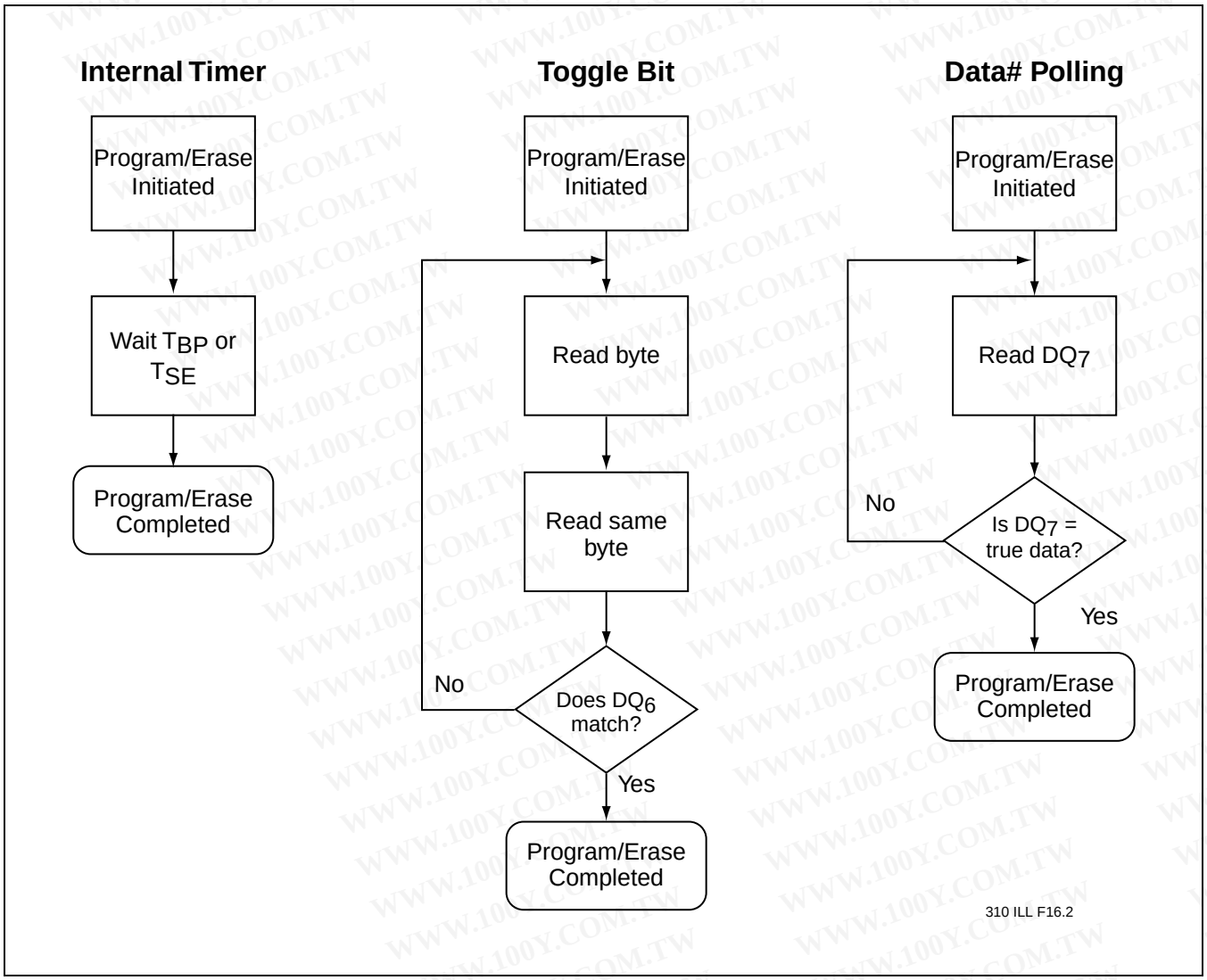


FIGURE 17: WRITE WAIT OPTIONS

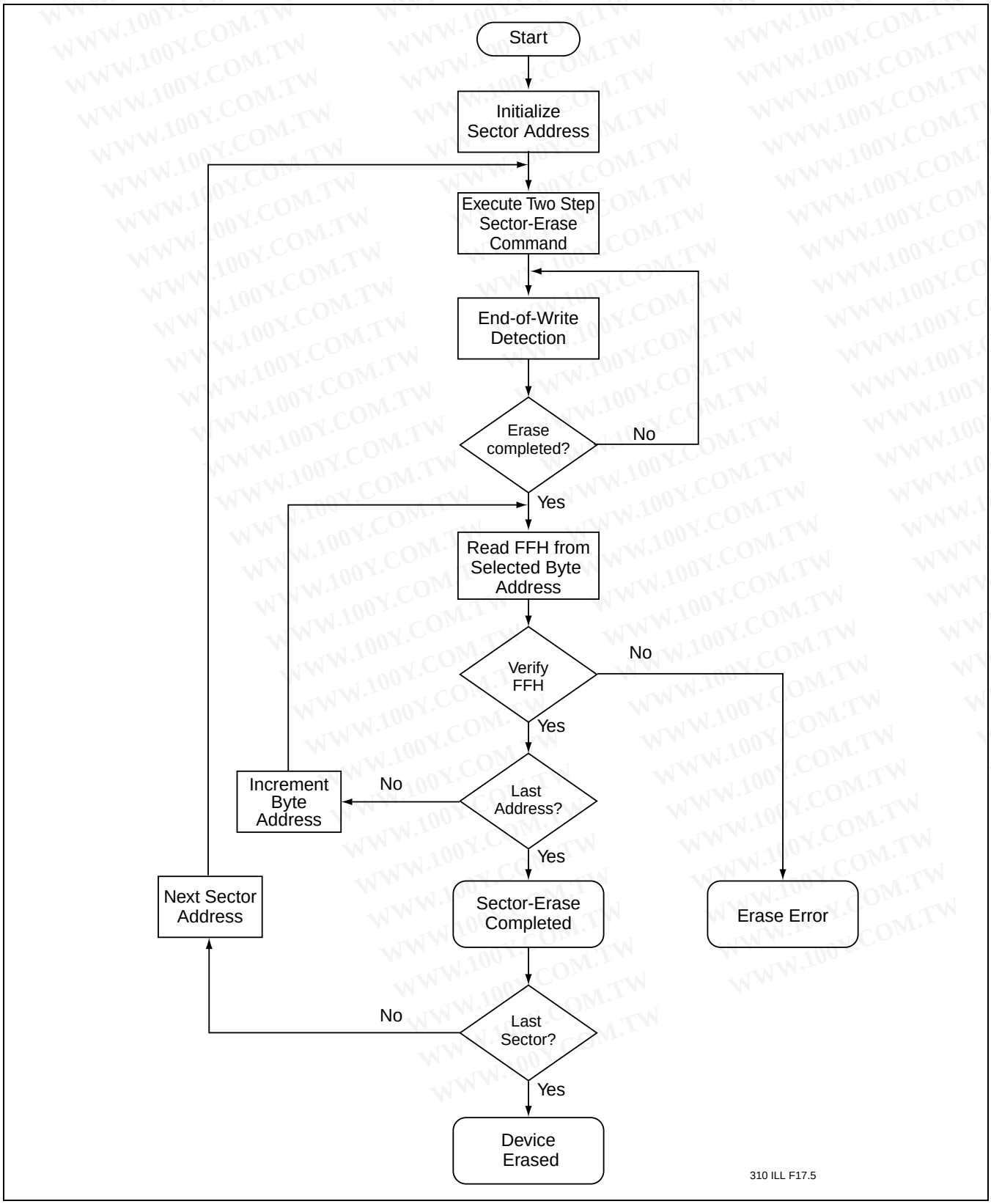


FIGURE 18: SECTOR-ERASE FLOWCHARTS

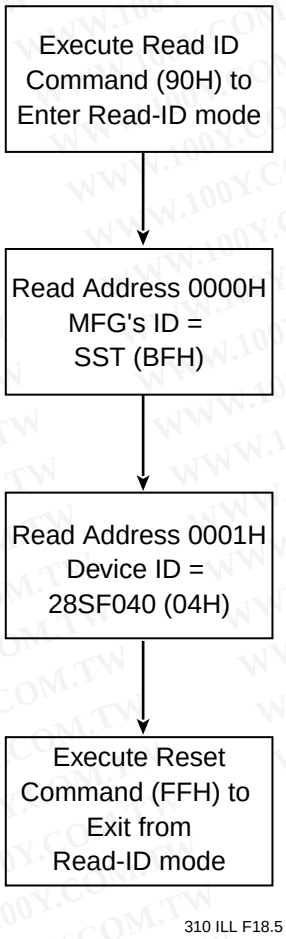


FIGURE 19: SOFTWARE PRODUCT ID FLOW

PRODUCT ORDERING INFORMATION

Device **Speed** **Suffix1** **Suffix2**

SST28xF040A - XXX - XX - XX

Package Modifier
H = 32 leads or pins

Package Type
E = TSOP (type 1, die up, 8mm x 20mm)
N = PLCC
P = PDIP

Temperature Range
C = Commercial = 0°C to +70°C
I = Industrial = -40°C to +85°C

Minimum Endurance
4 = 10,000 cycles

Read Access Speed
200 = 200 ns
150 = 150 ns
120 = 120 ns
90 = 90 ns

Function
F = Chip- or Sector-Erase
Byte- or Word-Program

Voltage
S = 4.5-5.5V
V = 2.7-3.6V

Valid combinations for SST28SF040A

SST28SF040A-90-4C-NH SST28SF040A-90-4C-EH SST28SF040A-90-4C-PH
SST28SF040A-120-4C-NH SST28SF040A-120-4C-EH
SST28SF040A-120-4I-NH‡ SST28SF040A-120-4I-EH‡

Valid combinations for SST28VF040A

SST28VF040A-150-4C-NH SST28VF040A-150-4C-EH
SST28VF040A-200-4C-NH* SST28VF040A-200-4C-EH*
SST28VF040A-200-4I-NH*‡ SST28VF040A-200-4I-EH*‡

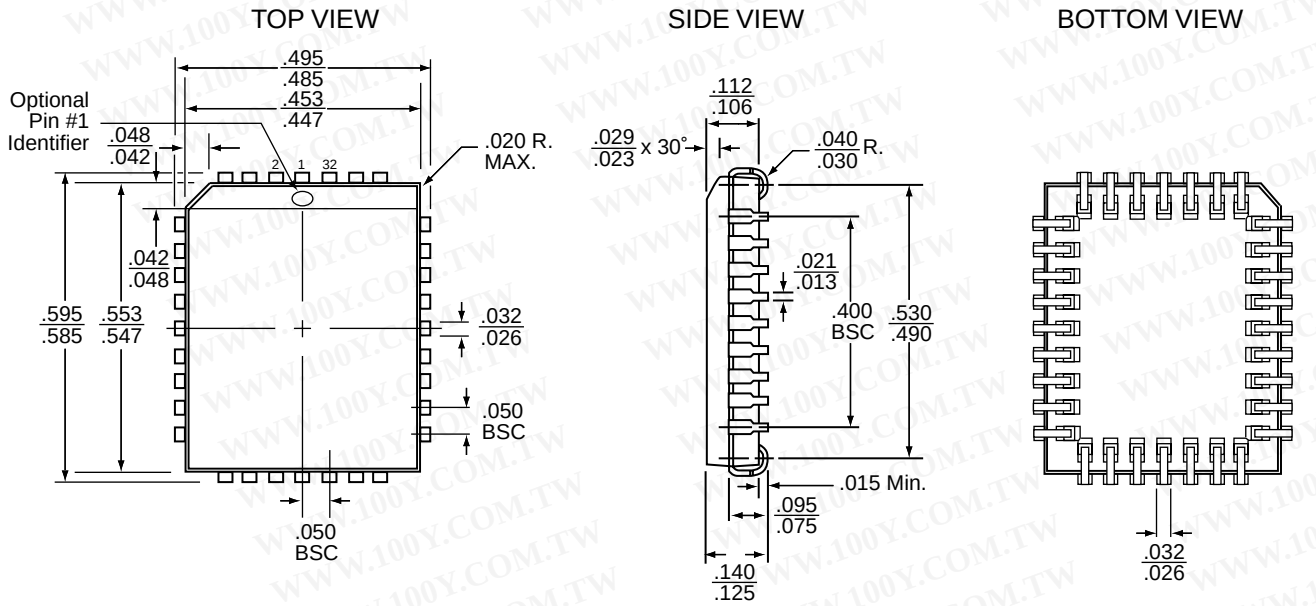
Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

***** Not recommended for new designs.

‡ The software Chip-Erase function is not supported by the industrial temperature part. Please contact SST if you require this function for an industrial temperature part.

Non-Pb: Several devices in this data sheet are also offered in non-Pb (no lead added) packages. The non-Pb part number is simply the standard part number with the letter “E” added to the end of the package code. The non-Pb package codes corresponding to the packages listed above are NHE and EHE.

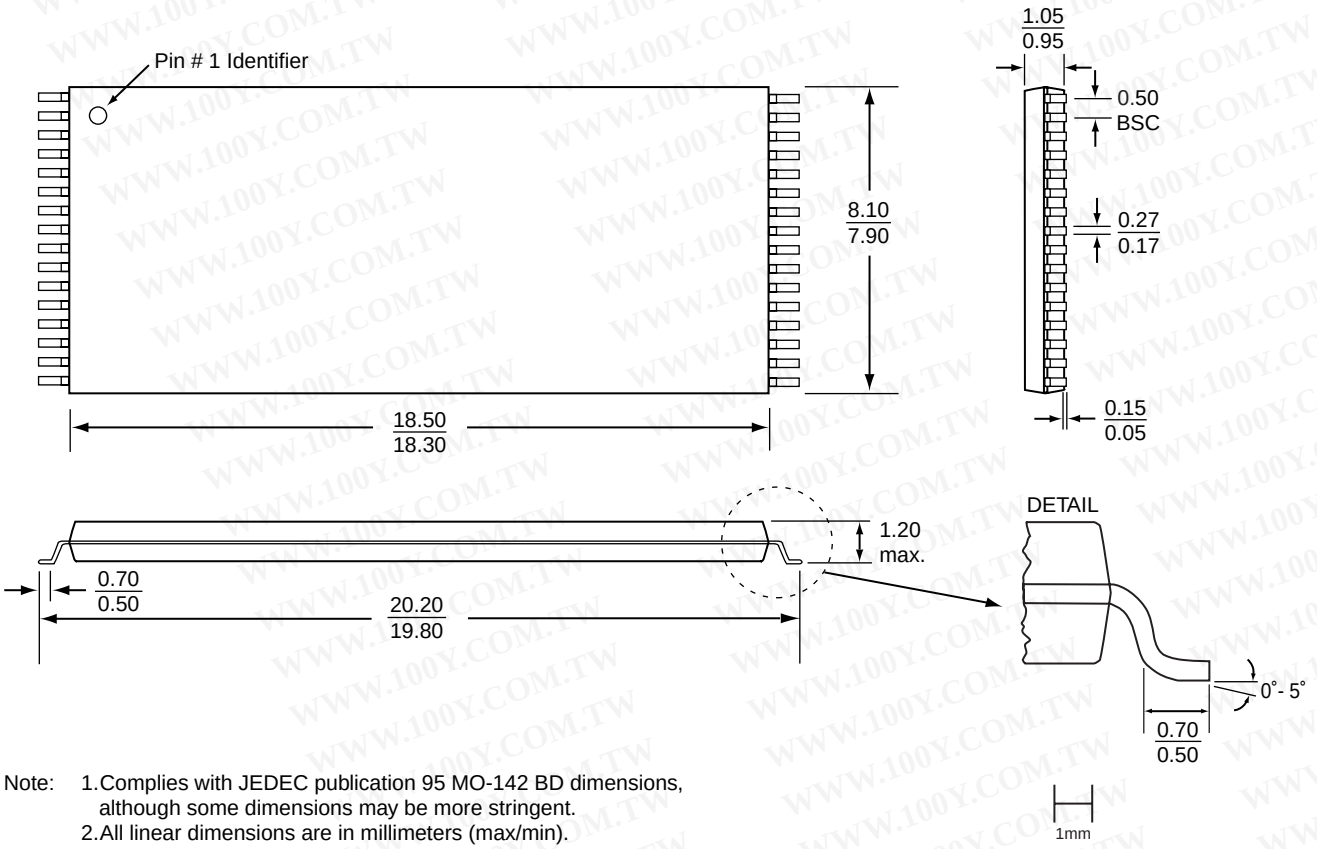
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

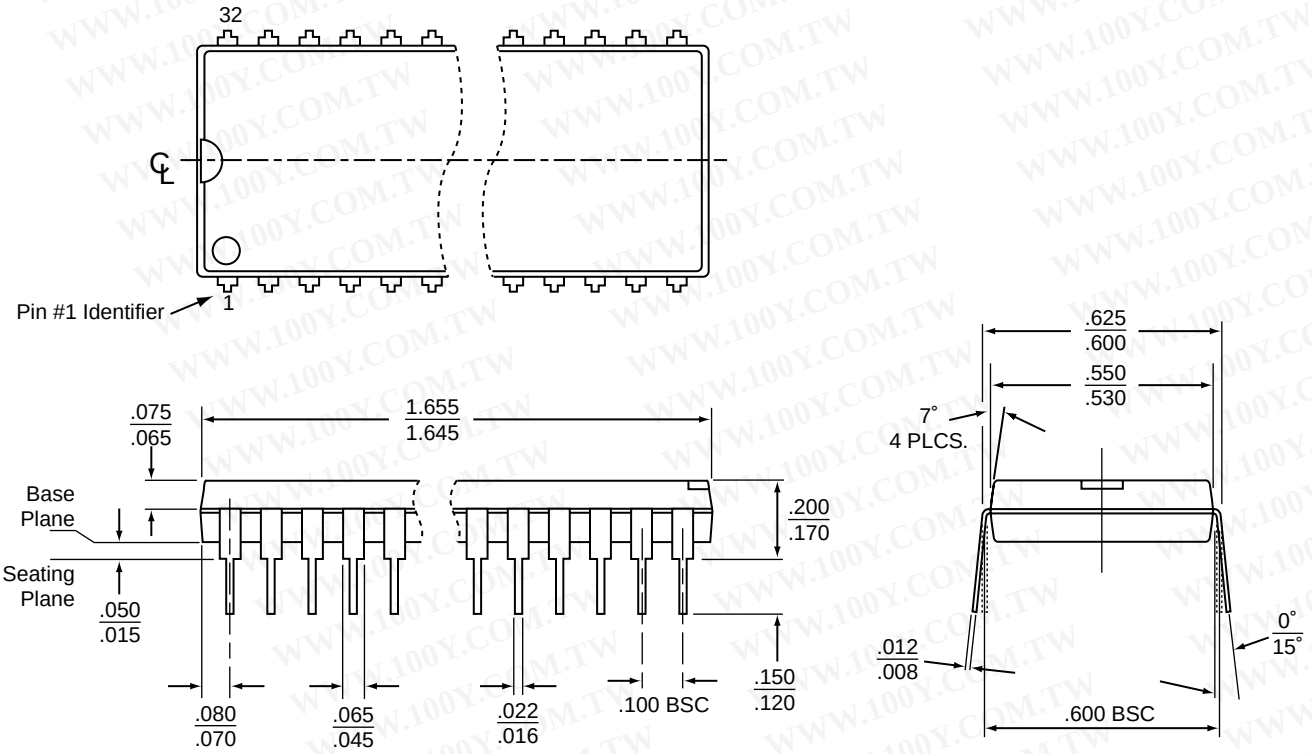
32-plcc-NH-3

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1.Complies with JEDEC publication 95 MO-142 BD dimensions, although some dimensions may be more stringent.
2.All linear dimensions are in millimeters (max/min).
3.Coplanarity: 0.1 mm
4.Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 20MM
SST PACKAGE CODE: EH



Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32-pdip-PH-3

32-PIN PLASTIC DUAL IN-LINE PINS (PDIP)
SST PACKAGE CODE: PH

TABLE 14: REVISION HISTORY

Number	Description	Date
04	• 2002 Data Book	May 2002
05	• Removed WH package • Part number changes - see page 22 for additional information • Clarified the Test Conditions for V_{DD} Read Current parameter in Table 6 and Table 7 on page 8 – Address input = V_{ILT}/V_{IHT}	Mar 2003