DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  - **SN54ALS874B, SN74ALS874B, SN74AS874 Have True Outputs**
  - **SN74ALS876A, SN74AS876 Have Inverting Outputs**
- **Asynchronous Clear**
- **Package Options Include Plastic Small-Outline (DW) Packages, Plastic (FN) and Ceramic (FK) Chip Carriers, and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

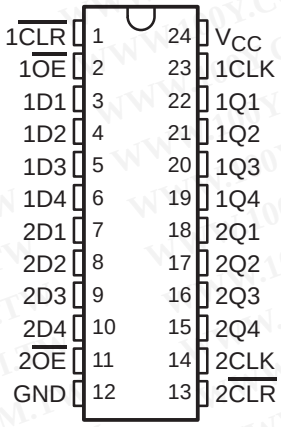
description

These dual 4-bit D-type edge-triggered flip-flops feature 3-state outputs designed specifically as bus drivers. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

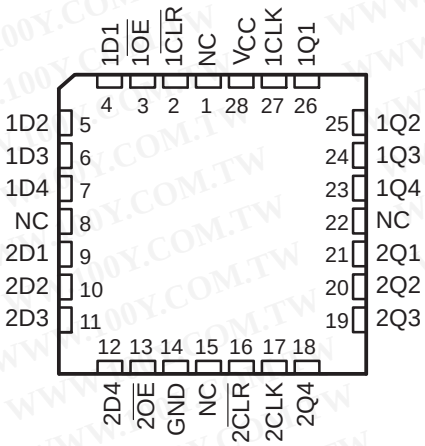
The edge-triggered flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN54ALS874B, SN74ALS874B, and SN74AS874 have clear ($\overline{CLR}$) inputs and noninverting Q outputs. The SN74ALS876A and SN74AS876 have preset ($\overline{PRE}$) inputs and inverting $\overline{Q}$ outputs; taking $\overline{PRE}$ low causes the four Q or $\overline{Q}$ outputs to go low independently of the clock.

The SN54ALS874B is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS874B, SN74ALS876A, SN74AS874, and SN74AS876 devices are characterized for operation from 0°C to 70°C.

SN54ALS874B . . . JT PACKAGE
SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE
(TOP VIEW)

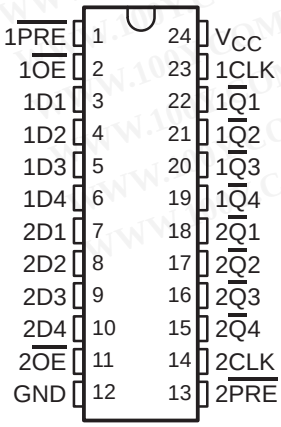


SN54ALS874B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE
(TOP VIEW)



Function Tables

SN54ALS874B, SN74ALS874B, SN74AS874 (each flip-flop)

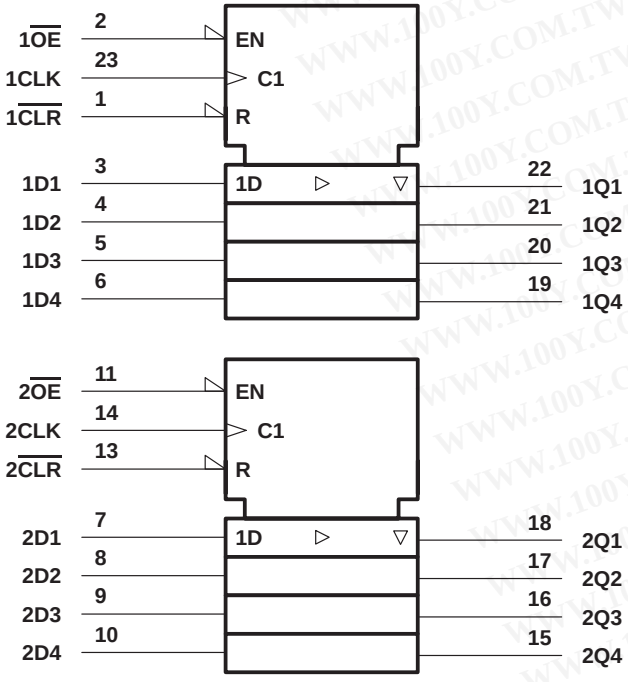
INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

SN74ALS876A, SN74AS876 (each flip-flop)

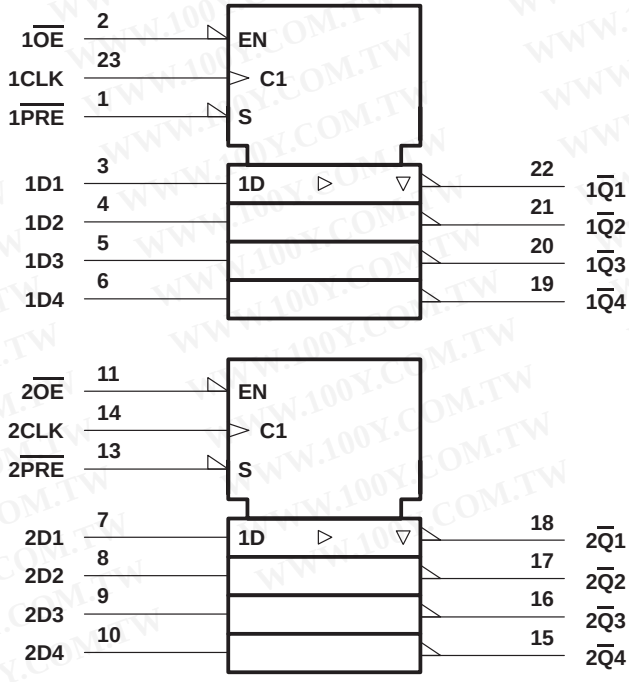
INPUTS				OUTPUT
$\overline{OE}$	$\overline{PRE}$	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbols†

SN54ALS874B, SN74ALS874B, SN74AS874



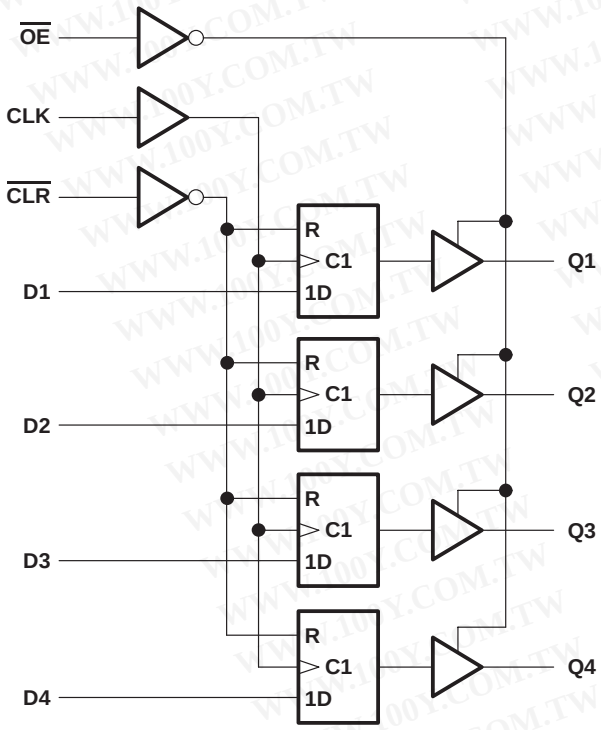
SN74ALS876A, SN74AS876



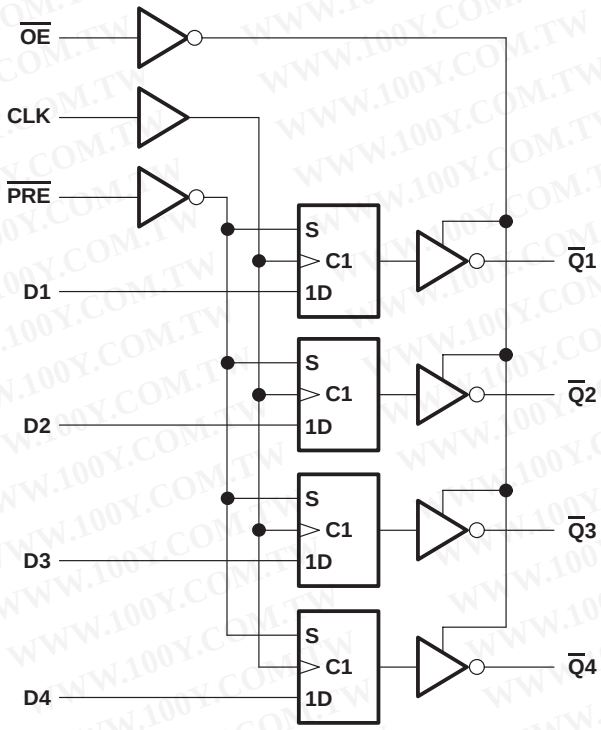
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagrams (positive logic)

SN54ALS874B, SN74ALS874B, SN74AS874
(each quad flip-flop)



SN74ALS876A, SN74AS876
(each quad flip-flop)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS874B . . . . . –55°C to 125°C
SN74ALS874B, SN74ALS876A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	15			10			
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
		V_{CC} = 4.5 V	I_{OH} = −1 mA	2.4	3.3					
			I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CC}	′ALS874B	V_{CC} = 5.5 V	Outputs high		14	21		14	21	mA
			Outputs low		19	30		19	30	
			Outputs disabled		20	32		20	32	
	SN74ALS876A	V_{CC} = 5.5 V	Outputs high					14	21	
			Outputs low					18	29	
			Outputs disabled					20	31	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS874B		SN74ALS874B		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	Any Q	4	18	4	14	ns
t_{PHL}			4	16	4	14	
t_{PHL}	$\overline{CLR}$	Any Q	5	23	5	17	ns
t_{PZH}	$\overline{OE}$	Any Q	4	24	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OE}$	Any Q	2	15	2	10	ns
t_{PLZ}			3	22	3	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			SN74ALS876A		
			MIN	MAX	
f_{max}			30		MHz
t_{PLH}	CLK	Any $\overline{Q}$	4	14	ns
t_{PHL}			4	14	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$	6	19	ns
t_{PZH}	$\overline{OE}$	Any $\overline{Q}$	4	18	ns
t_{PZL}			4	18	
t_{PHZ}	$\overline{OE}$	Any $\overline{Q}$	2	10	ns
t_{PLZ}			3	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN74AS874, SN74AS876 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74AS874			SN74AS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−15			−15	mA
I_{OL}	Low-level output current				48			48	mA
f_{clock}	Clock frequency		0		125	0		80	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2			4.5			ns
		CLK high	3			6.2			
		CLK low	4			6.2			
t_{su}	Setup time before CLK↑	Data	2			4.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	4			5			
t_h	Hold time, data after CLK↑		1			2			ns
T_A	Operating free-air temperature		0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS874 SN74AS876			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} −2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−2	mA
	All others					−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	SN74AS874	V_{CC} = 5.5 V	Outputs high		82	133	mA
			Outputs low		92	149	
			Outputs disabled		100	160	
	SN74AS876	V_{CC} = 5.5 V	Outputs high		88	142	
			Outputs low		94	150	
			Outputs disabled		100	160	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			SN74AS874		
			MIN	MAX	
f_{max}			125		MHz
t_{PLH}	CLK	Any Q	3	8.5	ns
t_{PHL}			4	10.5	
t_{PHL}	$\overline{CLR}$	Any Q	4	9.5	ns
t_{PZH}	$\overline{OE}$	Any Q	2	7	ns
t_{PZL}			3	10.5	
t_{PHZ}	$\overline{OE}$	Any Q	2	6	ns
t_{PLZ}			2	7.5	

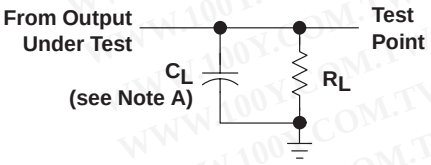
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

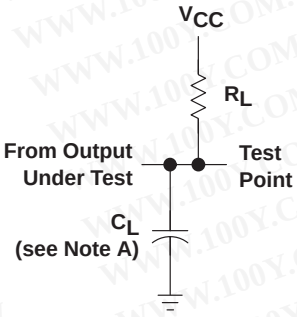
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			SN74AS876		
			MIN	MAX	
f_{max}			80		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	8.5	ns
t_{PHL}			4	10.5	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$	4	9.5	ns
t_{PZH}	$\overline{OE}$	Any $\overline{Q}$	2	7	ns
t_{PZL}			3	11	
t_{PHZ}	$\overline{OE}$	Any $\overline{Q}$	2	7	ns
t_{PLZ}			2	7	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

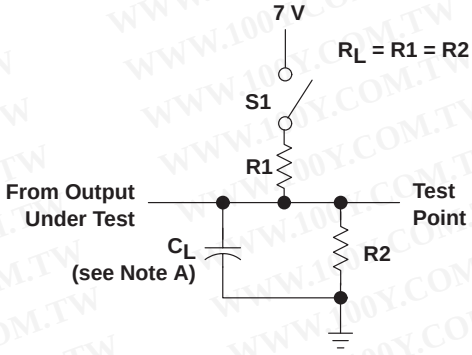
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



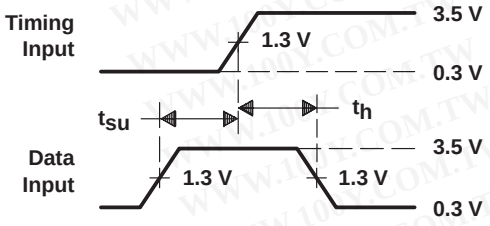
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



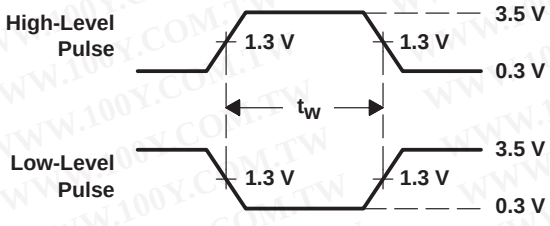
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



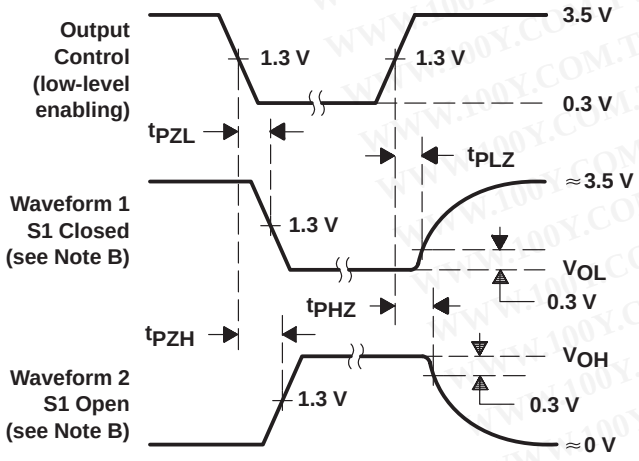
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



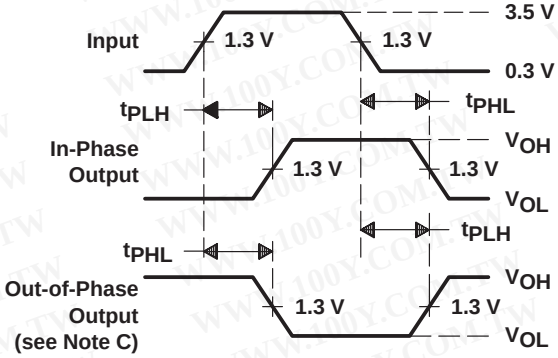
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.