

HD74LS73A

Dual J-K Flip-Flops (with Clear)

REJ03D0414-0300

Rev.3.00

Jul.22.2005

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 勝特力電子 86-755-83289527
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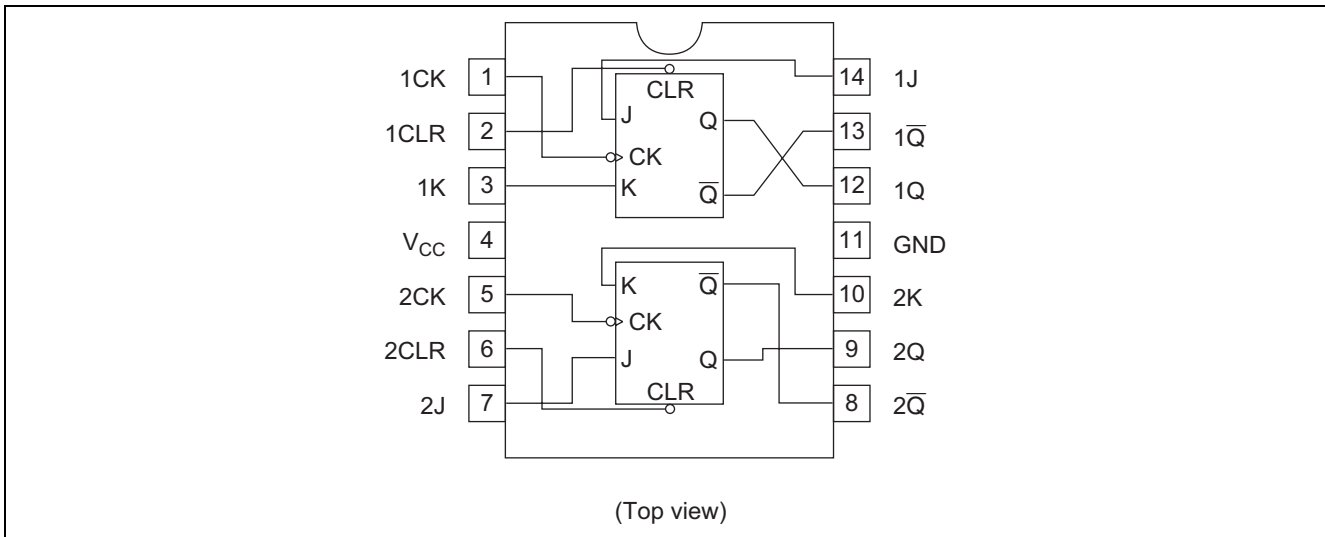
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS73AP	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS73ARPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

Inputs				Outputs	
Clear	Clock	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	\bar{Q}_0

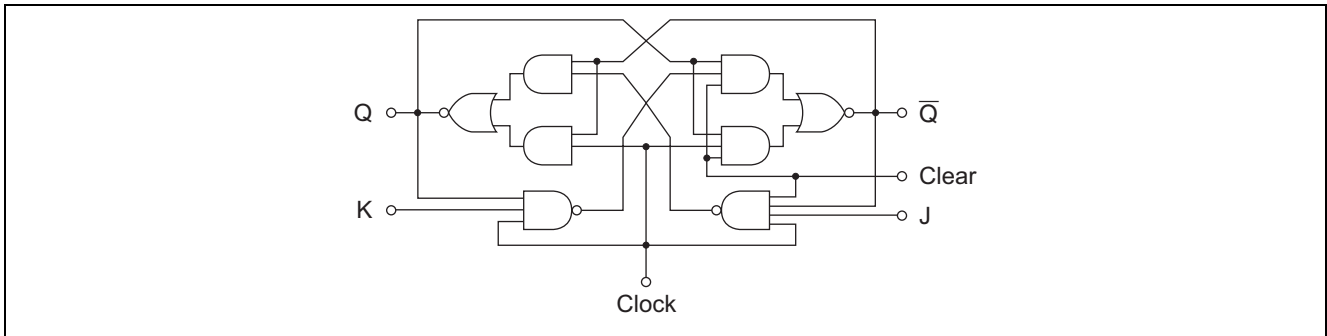
H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,

Q_0 ; level of Q before the indicated steady-state input conditions were established.

\bar{Q}_0 ; complement of \bar{Q}_0 or level of Q before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

Block Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	-400	μA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	-20	25	75	°C
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	t_w (Clock High)	20	—	—	ns
	t_w (Clear Low)	25	—	—	
Setup time	t_{su} ("H" Data)	20↓	—	—	ns
	t_{su} ("L" Data)	20↓	—	—	
Hold time	t_h	0↓	—	—	ns

Note: ↓; The arrow indicates the falling edge.

Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V _{IH}	2.0	—	—	V	
	V _{IL}	—	—	0.8	V	
Output voltage	V _{OH}	2.7	—	—	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 μA
	V _{OL}	—	—	0.5	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V
—		—	0.4			
Input current	J, K	—	—	20	μA	V _{CC} = 5.25 V, V _I = 2.7 V
	Clear	—	—	60		
	Clock	—	—	80		
	J, K	—	—	-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V
	Clear	—	—	-0.8		
	Clock	—	—	-0.8		
	J, K	—	—	0.1	mA	V _{CC} = 5.25 V, V _I = 7 V
	Clear	—	—	0.3		
	Clock	—	—	0.4		
Short-circuit output current	I _{OS}	-20	—	-100	mA	V _{CC} = 5.25 V
Supply current**	I _{CC}	—	4	6	mA	V _{CC} = 5.25 V
Input clamp voltage	V _{IK}	—	—	-1.5	V	V _{CC} = 4.75 V, I _{IN} = -18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

** With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At time of measurement, the clock input is founded.

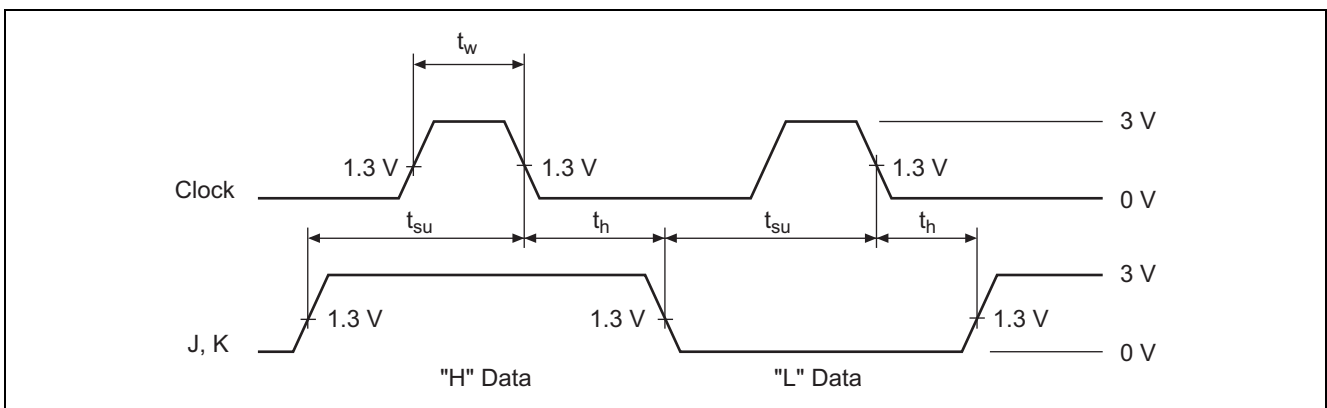
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Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f _{max}			30	45	—	MHz	
Propagation delay time	t _{PLH}	Clear	Q, \bar{Q}	—	15	20	ns	C _L = 15 pF, R _L = 2 kΩ
	t _{PHL}	Clock		—	15	20	ns	

Timing Definition

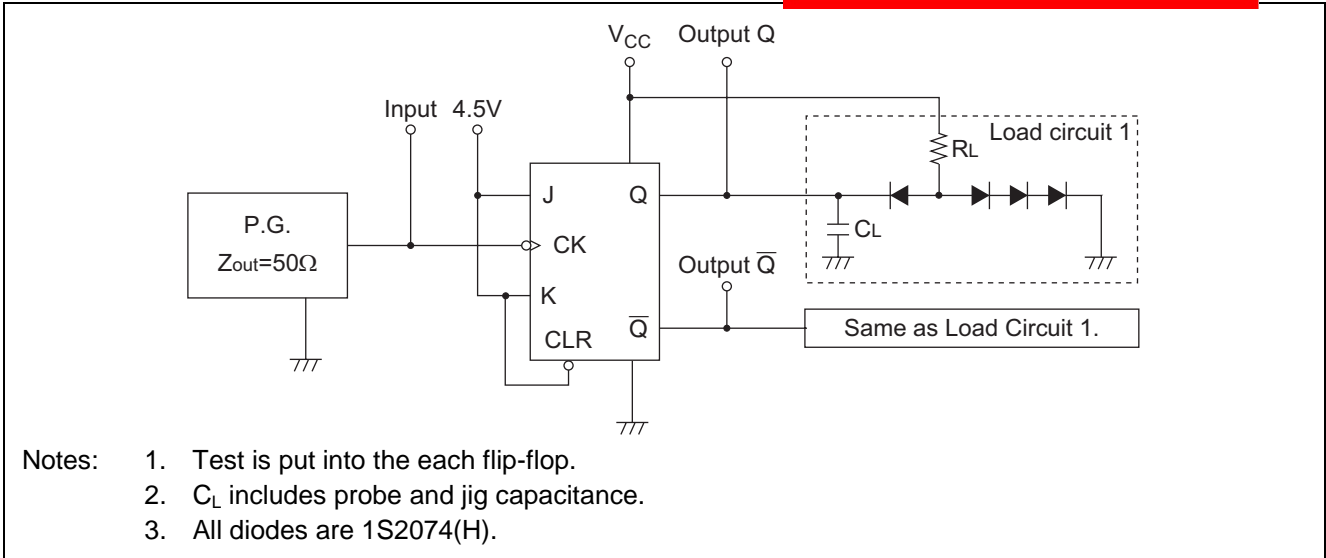


Testing Method

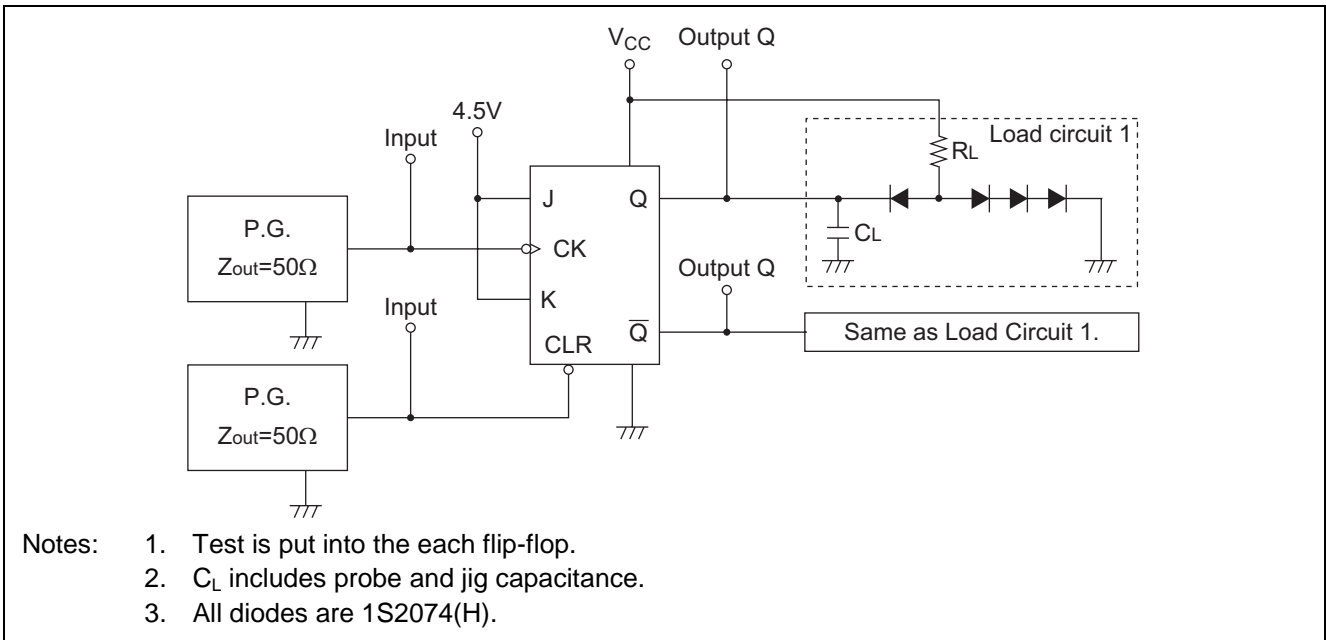
Test Circuit

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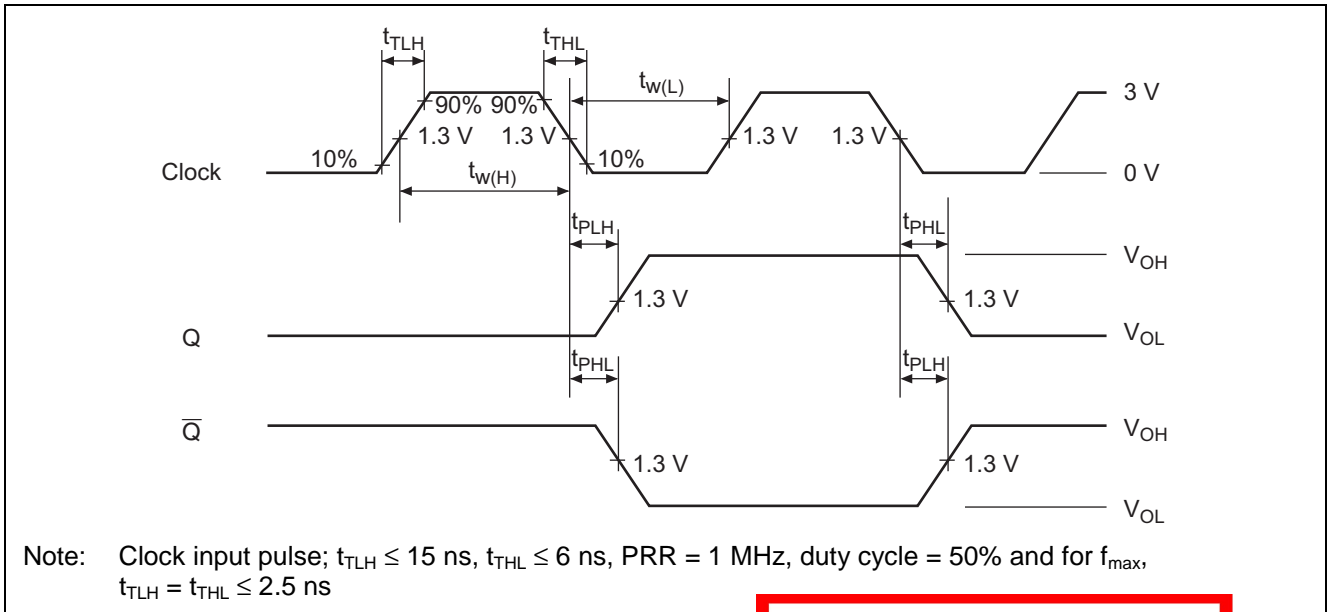
1. f_{max} , t_{PLH} , t_{PHL} , (Clock \rightarrow Q, \bar{Q})



2. t_{PHL} (Clear \rightarrow Q), t_{PLH} (Clear \rightarrow \bar{Q})

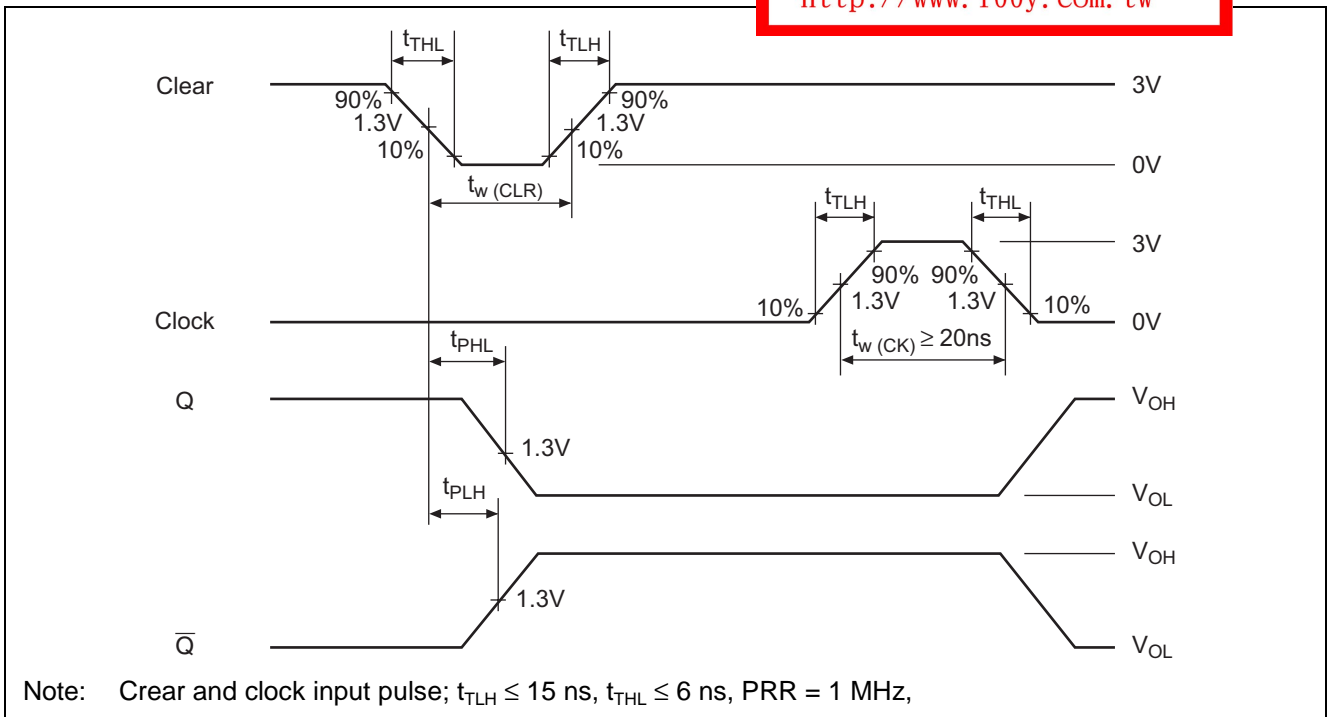


Waveforms 1

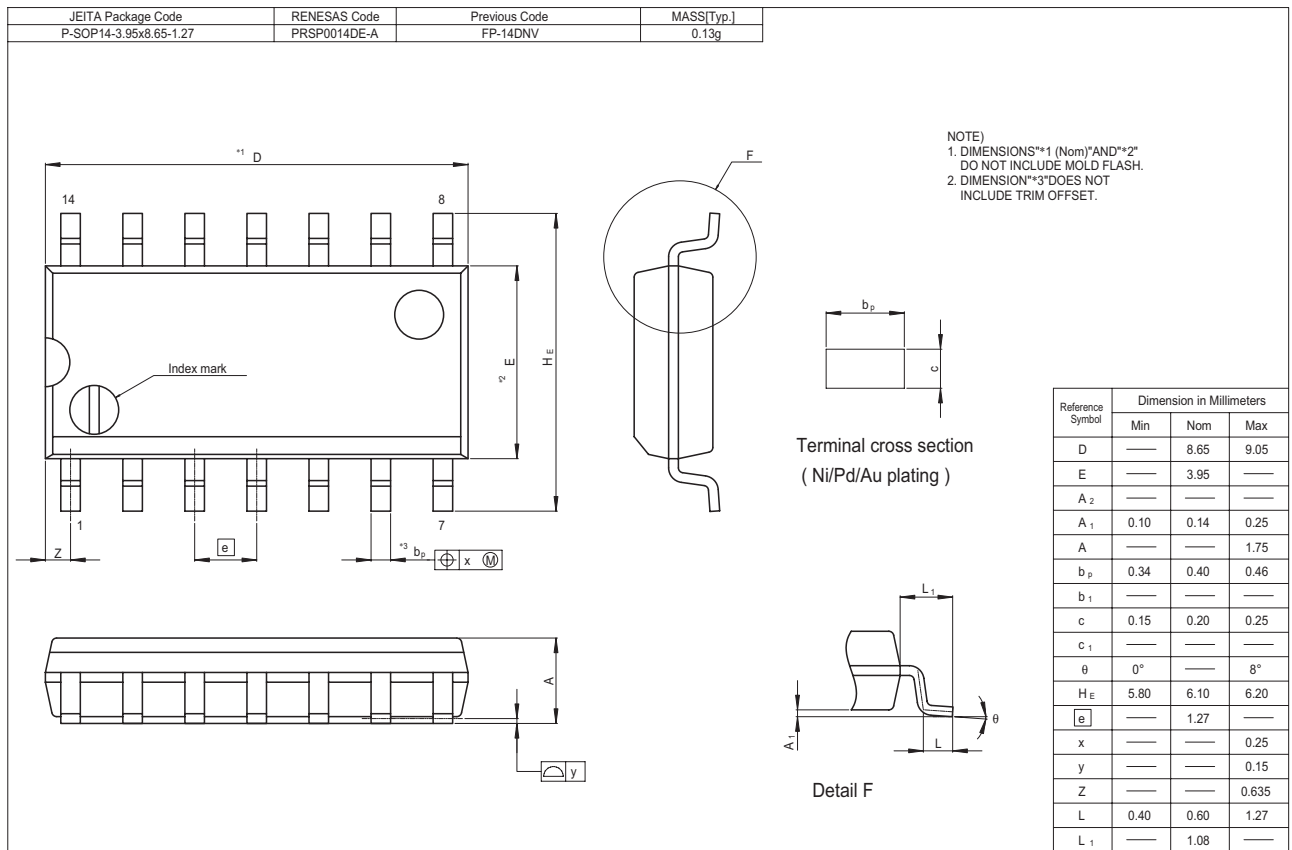
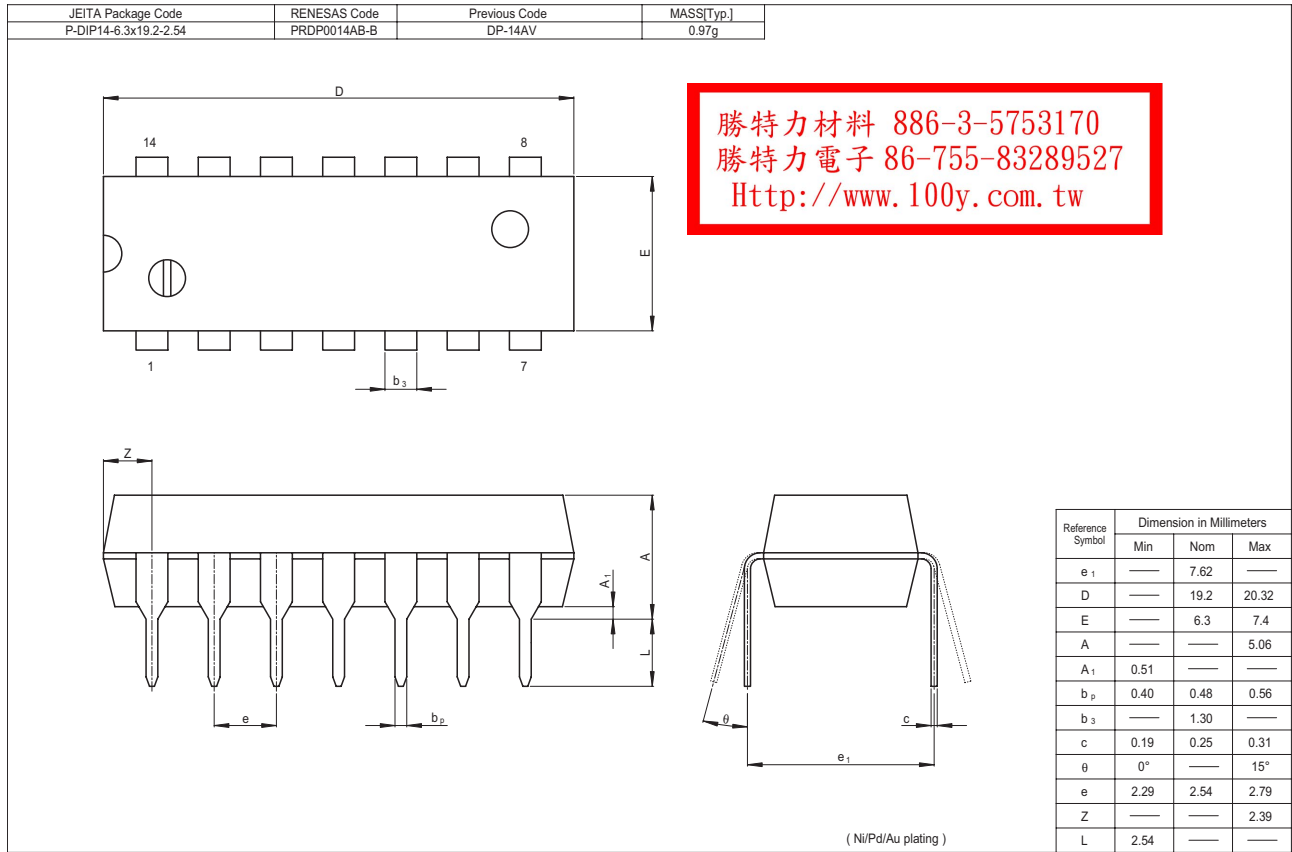


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Waveforms 2



Package Dimensions



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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

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