

HD75161A

Octal General Purpose Interface Bus Transceivers

REJ03D0309-0200Z
(Previous ADE-205-591 (Z))
Rev.2.00
Jul.16.2004

Description

The HD75161A is an 8 channel general purpose interface bus transceiver designed to meet the requirements of IEEE standard 488-1978. The transceiver is to provide the bus management and data transfer signals during operating in a controller instrumentation system. When combined with the HD75160A octal bus transceiver, the HD75161A provides the complete 16 wire interface for the IEEE 488 bus. The HD75161A features eight driver receiver pairs connected in a front to back configuration to form input/output ports at both the bus and terminal sides. The direction of data through these driver receiver pairs is determined by the DC and TE enable signals. The device exhibits a high impedance to the bus when $V_{CC} = 0$ V since the bus terminating resistors are built in. It features driver outputs which can handle loads up to 48 mA of sink current. Each receiver features p n p transistor inputs for high input impedance and guaranteed hysteresis of 400 mV for increased noise immunity.

Features

- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD75161AP	DILP-20 pin	DP-20N, -20NEV	P	—

Pin Arrangement

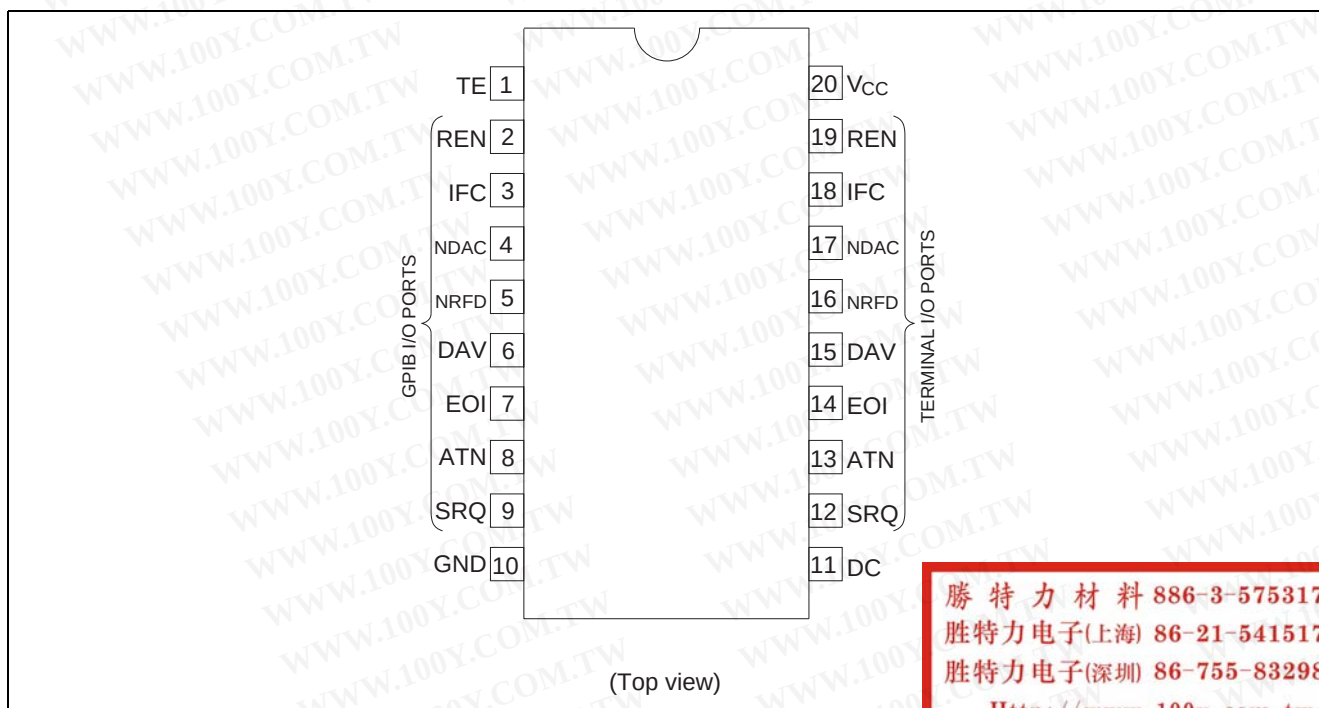


Table Of Abbreviation

DRIVERS		
Name	Identity	Class
DC	Direction Control	Control
TE	Talk Enable	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End Or Identify	
DAV	Data Valid	
NDAC	Not Data Accepted	Data Transfer
NRFD	Not Ready For Data	

Function Table

Controls			Bus management Channels					Data transfer Channels		
			ATN*1	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
DC	TE	ATN	Controlled By DC				EOI	Controlled by TE		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

H : High level

L : Low level

X : Irrelevant

R : Receiver

T : Transmit

Notes: 1. ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state.

2. Direction of data transmission is from the terminal side to the bus side and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	7	V
Input Voltage	V_{IC}	5.5	V
Output Current	I_{OL}	100	mA
Power Dissipation ($T_a = 25^\circ\text{C}$)	P_T	1150	mW
Operating Temperature Range	T_{opr}	0 to 70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

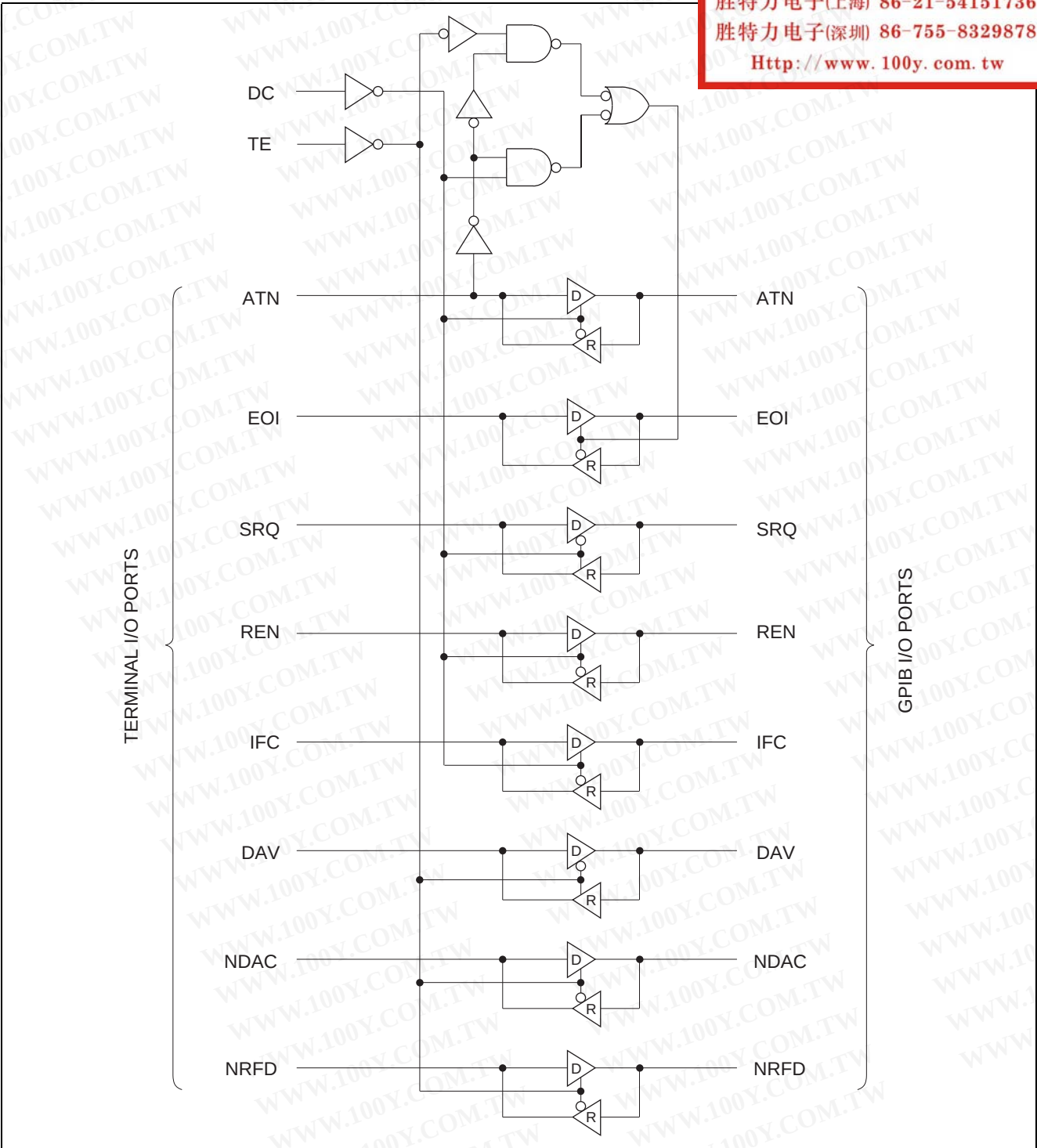
Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

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Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.75	5.00	5.25	V
Output Current	Bus Ports With 3 State Outputs	I_{OH}	—	—	-5.2	mA
	Terminal Ports		—	—	-800	μ A
Output Current	Bus Ports With 3 State Outputs	I_{OL}	—	—	48	mA
	Terminal Ports		—	—	16	
Operating Temperature		T_{opr}	0	—	70	$^{\circ}$ C

Logic Diagram



DC Electrical Characteristics (Ta = 0 to 70°C)

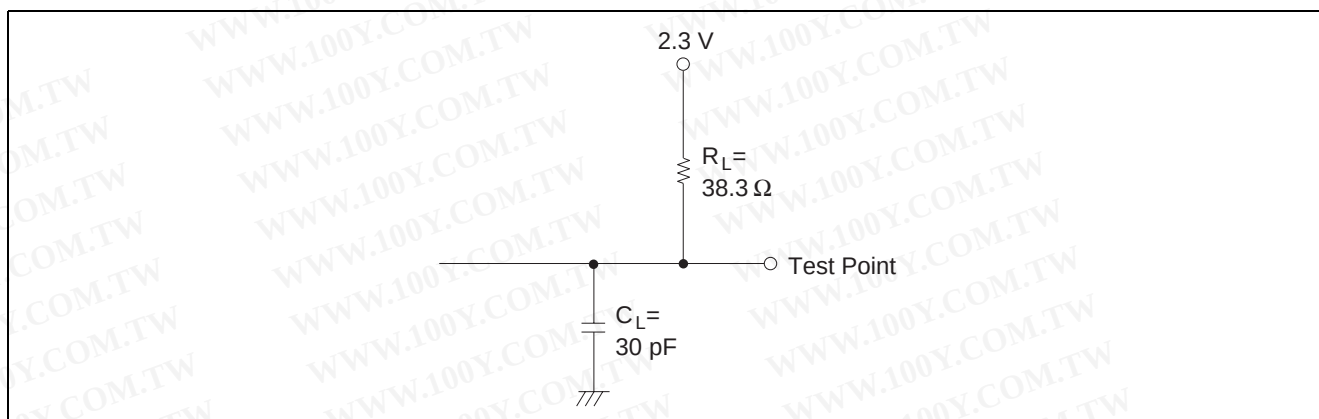
Item	Symbol	V _{CC}	Min	Max	Unit	Conditions
Input Voltage	V _{IH}	2	—	—	V	
	V _{IL}	—	—	0.8		
Input Clamp Voltage	V _{IK}	—	—	-1.5	V	I _I = -18 mA
Hysteresis	Bus	V _T ⁺ - V _T ⁻	0.4	—	V	
Output Voltage	Terminal	V _{OH}	2.7	—	V	I _{OH} = -800 µA
	Bus		2.5	—		I _{OH} = -5.2 mA
	Terminal	V _{OL}	—	0.5	V	I _{OL} = 16 mA
	Bus		—	0.5		I _{OL} = 48 mA
Input Current	Terminal	I _I	—	100	µA	V _I = 5.5 V
	Terminal And	I _{IH}	—	20		V _I = 2.7 V
	Control Inputs	I _{IL}	—	-100		V _I = 0.5 V
Voltage at Bus Port		V _{I/O (bus)}	2.5	3.7	V	Driver
			—	-1.5		Disabled
Current Into Bus Port	V _{CC} ON	I _{I/O (bus)}	-1.3	—	mA	Driver
			0	-3.2		Disabled
			—	+2.5		V _{I(bus)} = -1.5 V to 0.4 V
			—	-3.2		V _{I(bus)} = 0.4 V to 2.5 V
			0	2.5		V _{I(bus)} = 2.5 V to 3.7 V
			0.7	2.5		V _{I(bus)} = 3.7 V to 5 V
	V _{CC} OFF		—	40	µA	V _{CC} = 0, V _{I(bus)} = 5 V to 5.5 V
Short Circuit	Terminal	I _{OS}	-15	-75	mA	
Output Current	Bus		-25	-125		
Supply Voltage	I _{CC}	—	—	100	mA	No Load TE, DC, low
Bus port Capacitance	C _{I/O (bus)}	—	30	—	pF	V _{CC} = 5 V or 0 V, V _{I/O} = 0 to 2 V, f = 1 MHz

Note: 1. V_{CC} = 5 V, Ta = 25°CSwitching Characteristics (V_{CC} = 5 V, Ta = 25°C)

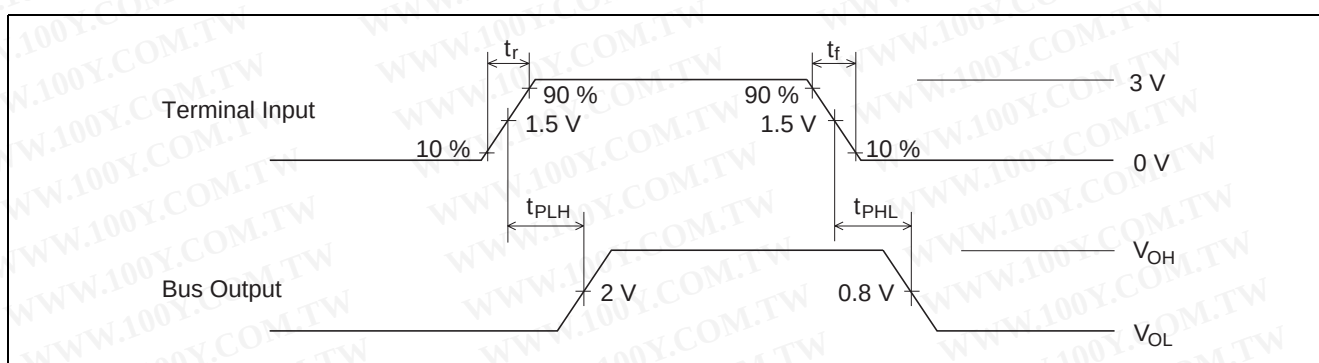
Item	Symbol	Input	Output	Min	Typ	Max	Unit	Test Circuit	Test Conditions
Propagation Delay Time	t _{PLH}	Terminal	BUS	—	14	20	ns	1	C _L = 30 pF R _L = 38.3 Ω to 2.3 V
	t _{PHL}			—	14	20			
	t _{PLH}	BUS	Terminal	—	12	20		2	C _L = 30 pF R _L = 240 Ω to 5 V
	t _{PHL}			—	16	22			
Output Enable Time	t _{ZH}	TE DC	BUS	—	—	60		3	C _L = 15 pF R _L = 480 Ω to 0 V
Output Disable Time	t _{HZ}			—	—	45			
Output Enable Time	t _{ZL}			—	—	60			C _L = 15 pF R _L = 38.3 Ω to 2.3 V
Output Disable Time	t _{LZ}			—	—	55			
Output Enable Time	t _{ZH}	TE DC	Terminal	—	—	55		4	C _L = 15 pF R _L = 3 kΩ to 0 V
Output Disable Time	t _{HZ}			—	—	50			
Output Enable Time	t _{ZL}			—	—	45			C _L = 15 pF R _L = 280 Ω to 5 V
Output Disable Time	t _{LZ}			—	—	55			

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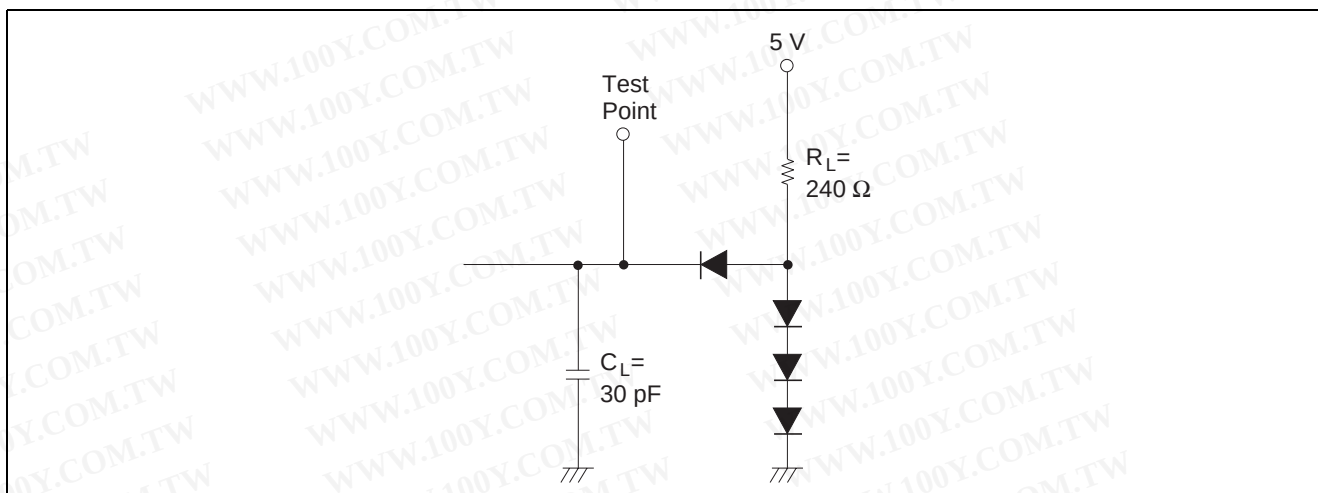
Switching Time Test Method

1. t_{PLH} , t_{PHL} 

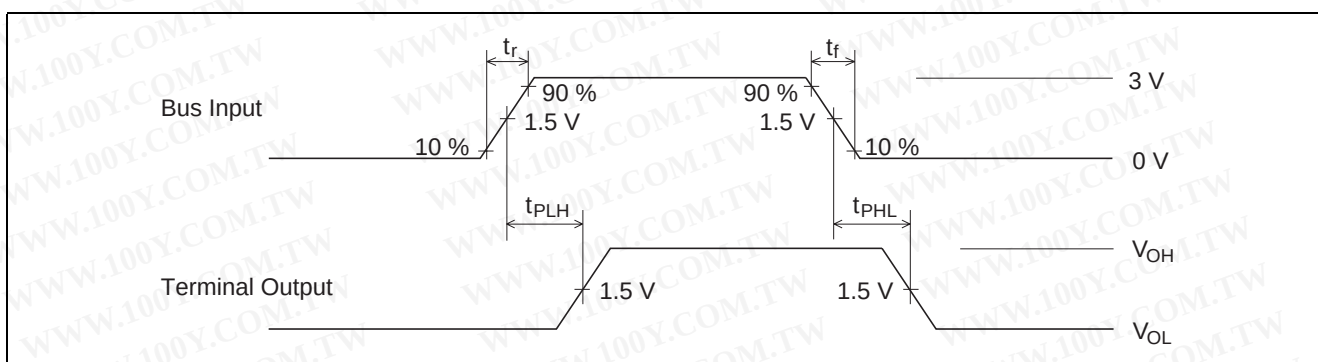
Waveforms-1



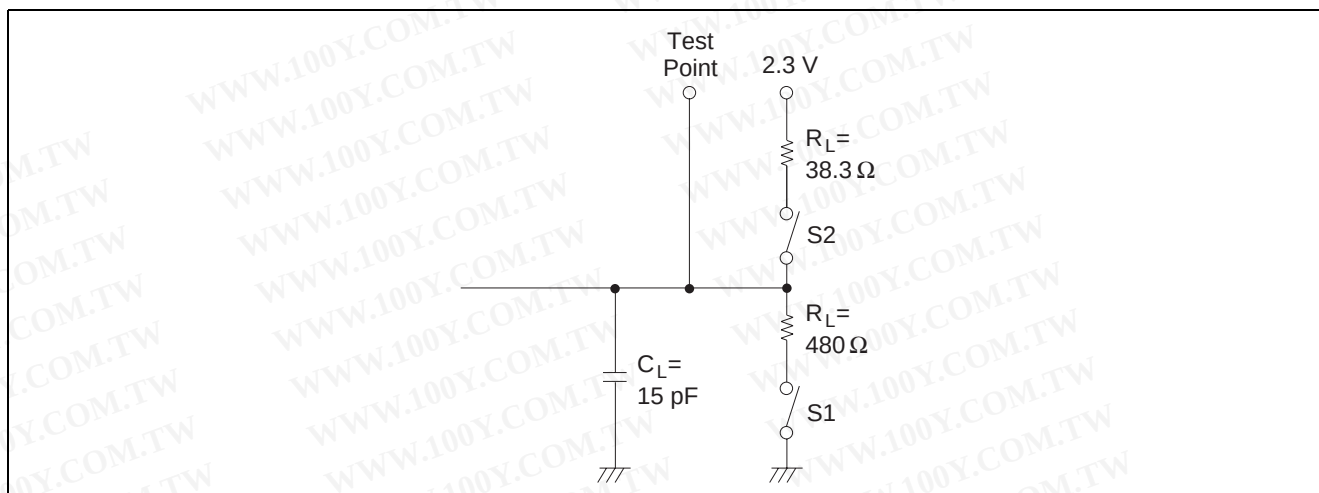
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2. t_{PLH} , t_{PHL} 

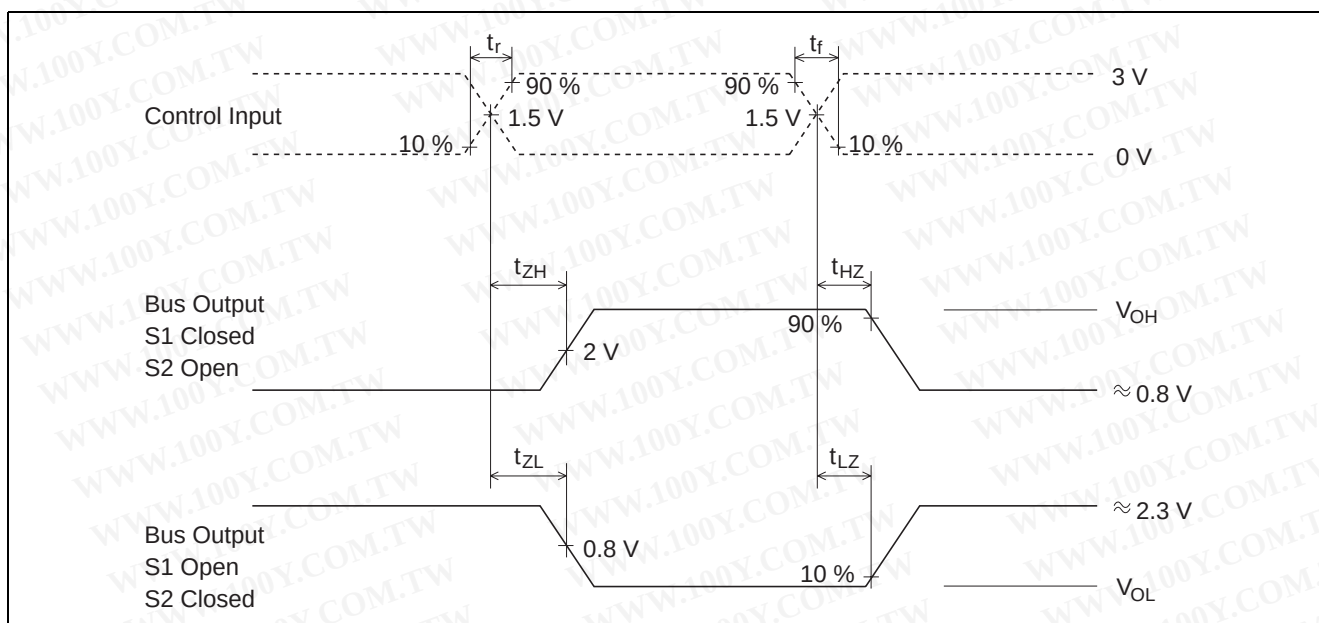
Waveforms-2



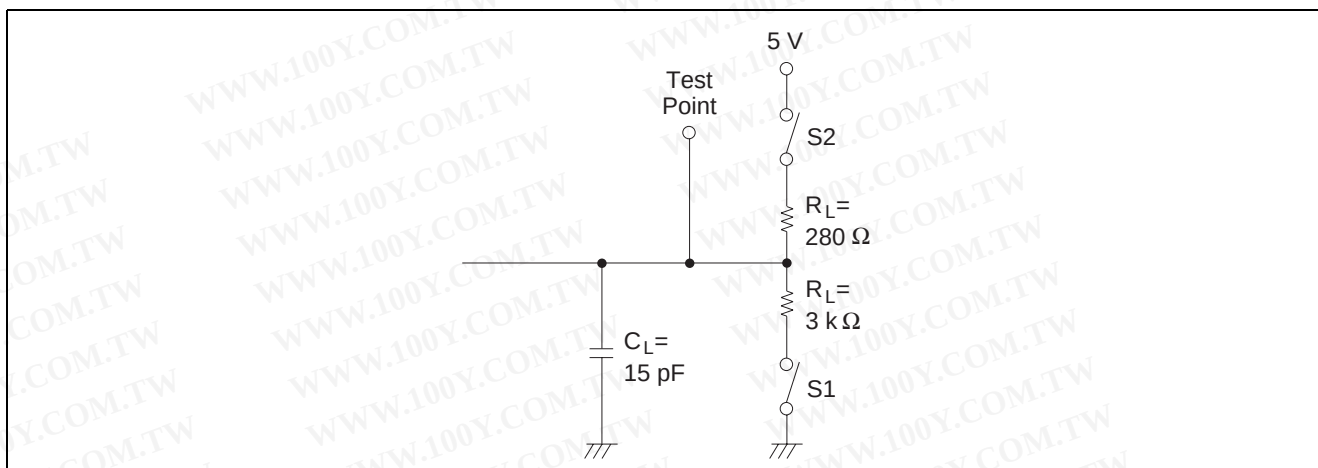
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3. t_{ZH} , t_{HZ} , t_{ZL} , t_{LZ} 

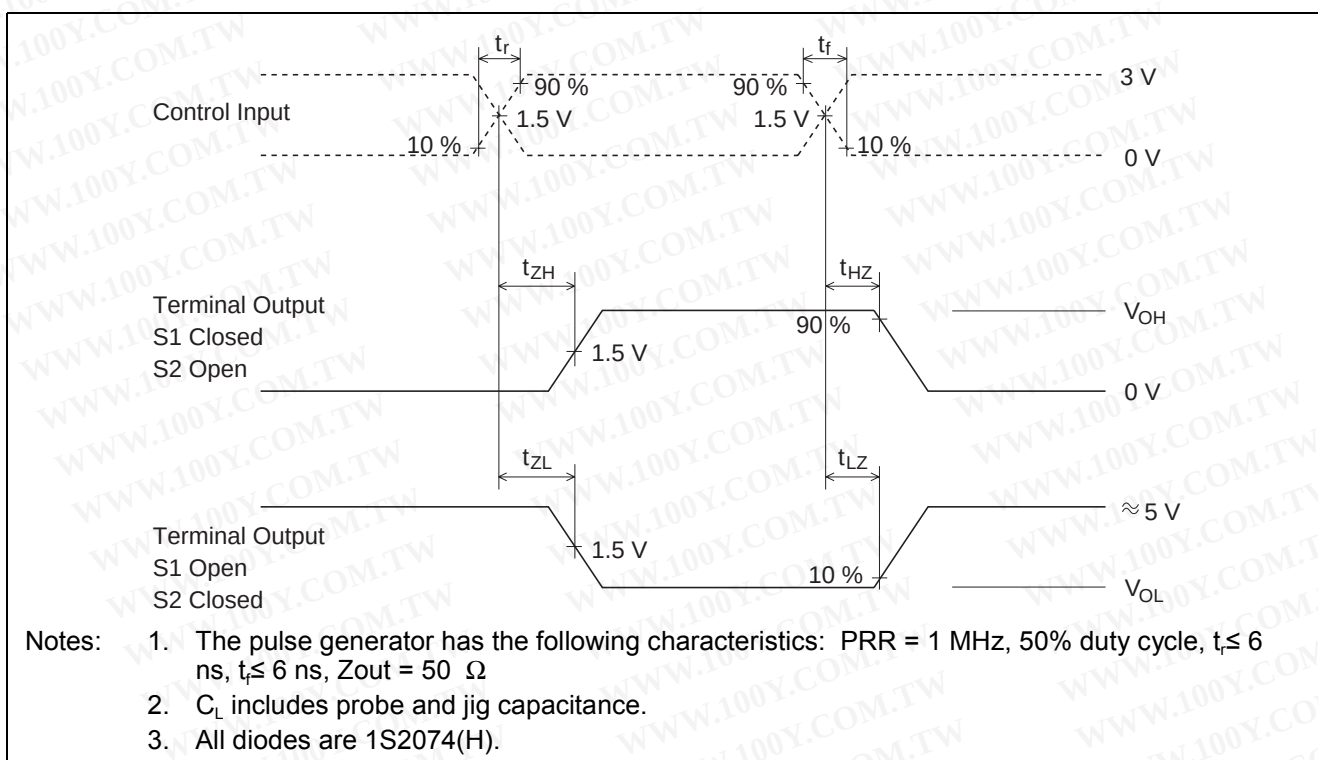
Waveforms-3



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4. t_{ZH} , t_{HZ} , t_{ZL} , t_{LZ} 

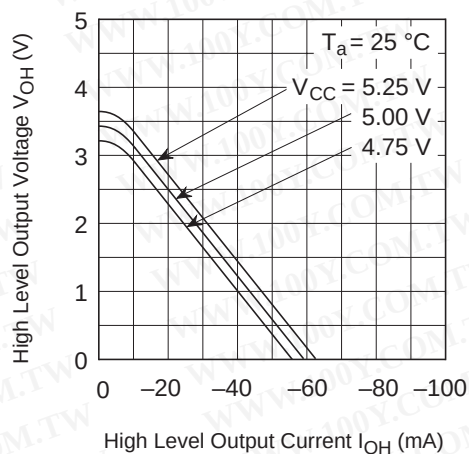
Waveforms-4



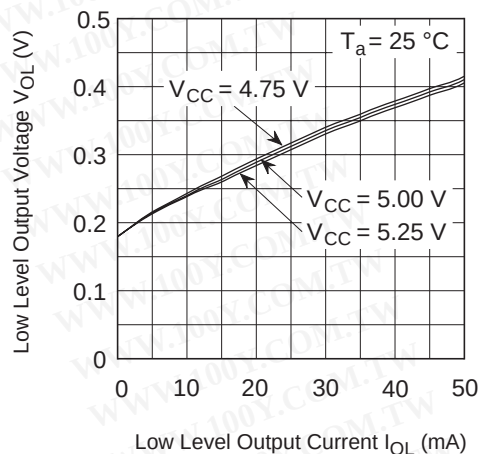
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Characteristics Of Driver And Receiver

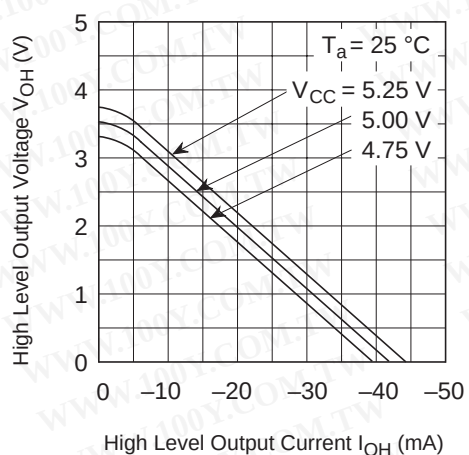
(a) Driver Output



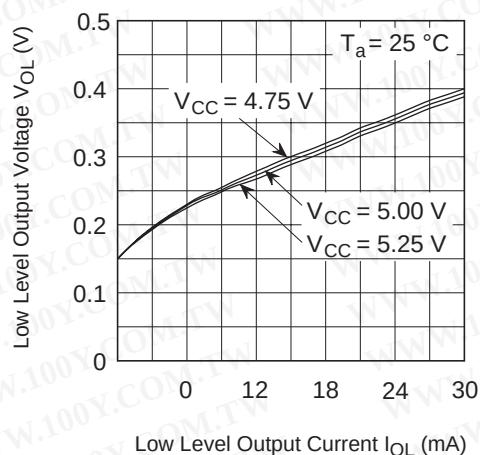
(b) Driver Output



(c) Receiver Output

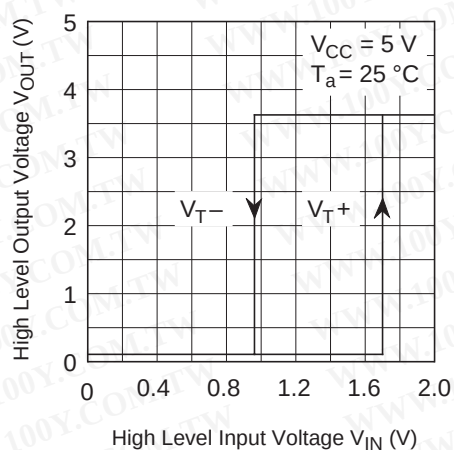


(d) Receiver Output



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(e) Input / Output Characteristics at Receiver

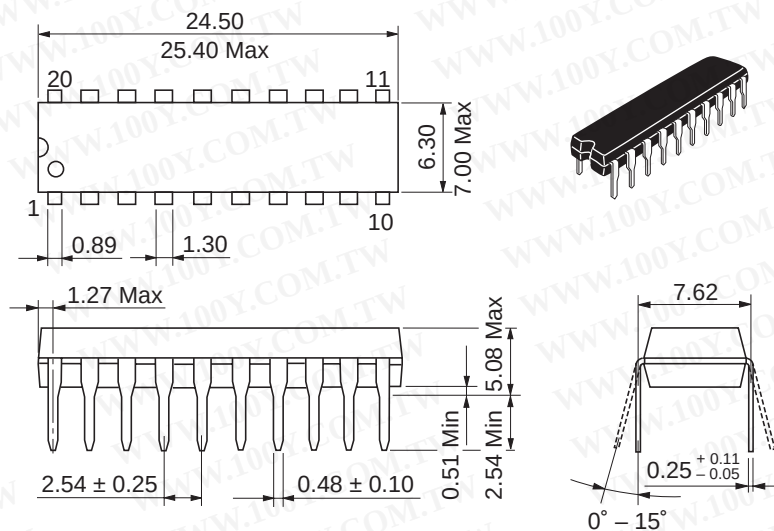


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Package Dimensions

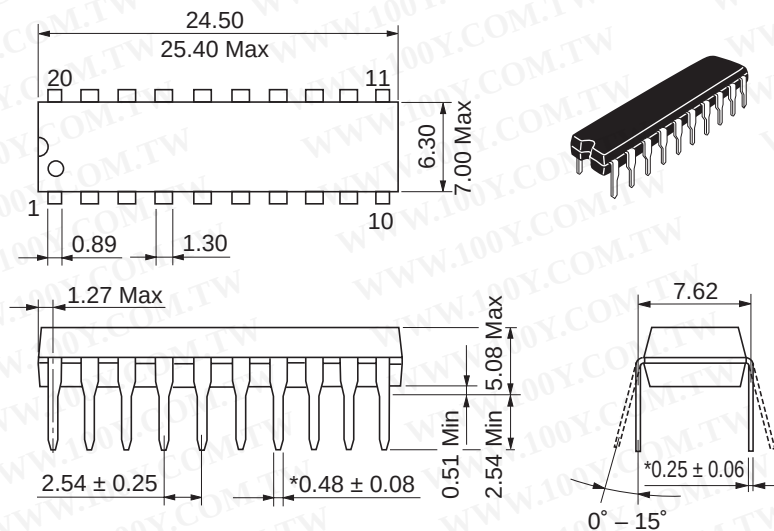
As of January, 2003

Unit: mm



Package Code	DP-20N
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

Unit: mm



*Ni/Pd/AU Plating

Package Code	DP-20NEV
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

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