



# TNY274-280

## TinySwitch-III Family

Energy Efficient, Offline Switcher with Enhanced Flexibility and Extended Power Range

### Product Highlights

#### Lowest System Cost with Enhanced Flexibility

- Simple ON/OFF control, no loop compensation needed
- Selectable current limit through BP/M capacitor value
  - Higher current limit extends peak power or, in open frame applications, maximum continuous power
  - Lower current limit improves efficiency in enclosed adapters/chargers
  - Allows optimum *TinySwitch-III* choice by swapping devices with no other circuit redesign
- Tight P<sub>f</sub> parameter tolerance reduces system cost
  - Maximizes MOSFET and magnetics power delivery
  - Minimizes max overload power, reducing cost of transformer, primary clamp & secondary components
- ON-time extension – extends low line regulation range/hold-up time to reduce input bulk capacitance
- Self-biased: no bias winding or bias components
- Frequency jittering reduces EMI filter costs
- Pin-out simplifies heatsinking to the PCB
- SOURCE pins are electrically quiet for low EMI

#### Enhanced Safety and Reliability Features

- Accurate hysteretic thermal shutdown protection with automatic recovery eliminates need for manual reset
- Improved auto-restart delivers <3% of maximum power in short circuit and open loop fault conditions
- Output overvoltage shutdown with optional Zener
- Line undervoltage detect threshold set using a single optional resistor
- Very low component count enhances reliability and enables single-sided printed circuit board layout
- High bandwidth provides fast turn on with no overshoot and excellent transient load response
- Extended creepage between DRAIN and all other pins improves field reliability

#### EcoSmart® – Extremely Energy Efficient

- Easily meets all global energy efficiency regulations
- No-load <150 mW at 265 VAC without bias winding, <50 mW with bias winding
- ON/OFF control provides constant efficiency down to very light loads – ideal for mandatory CEC regulations and 1 W PC standby requirements

#### Applications

- Chargers/adapters for cell/cordless phones, PDAs, digital cameras, MP3/portable audio, shavers, etc.

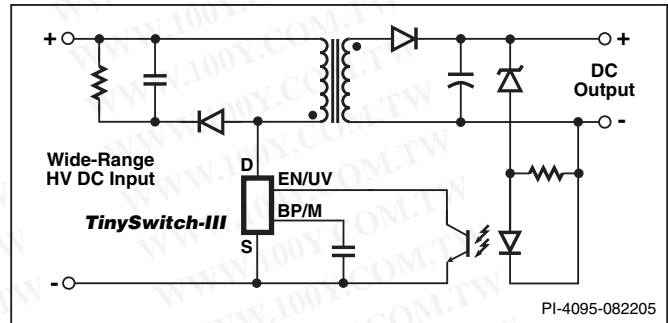


Figure 1. Typical Standby Application.

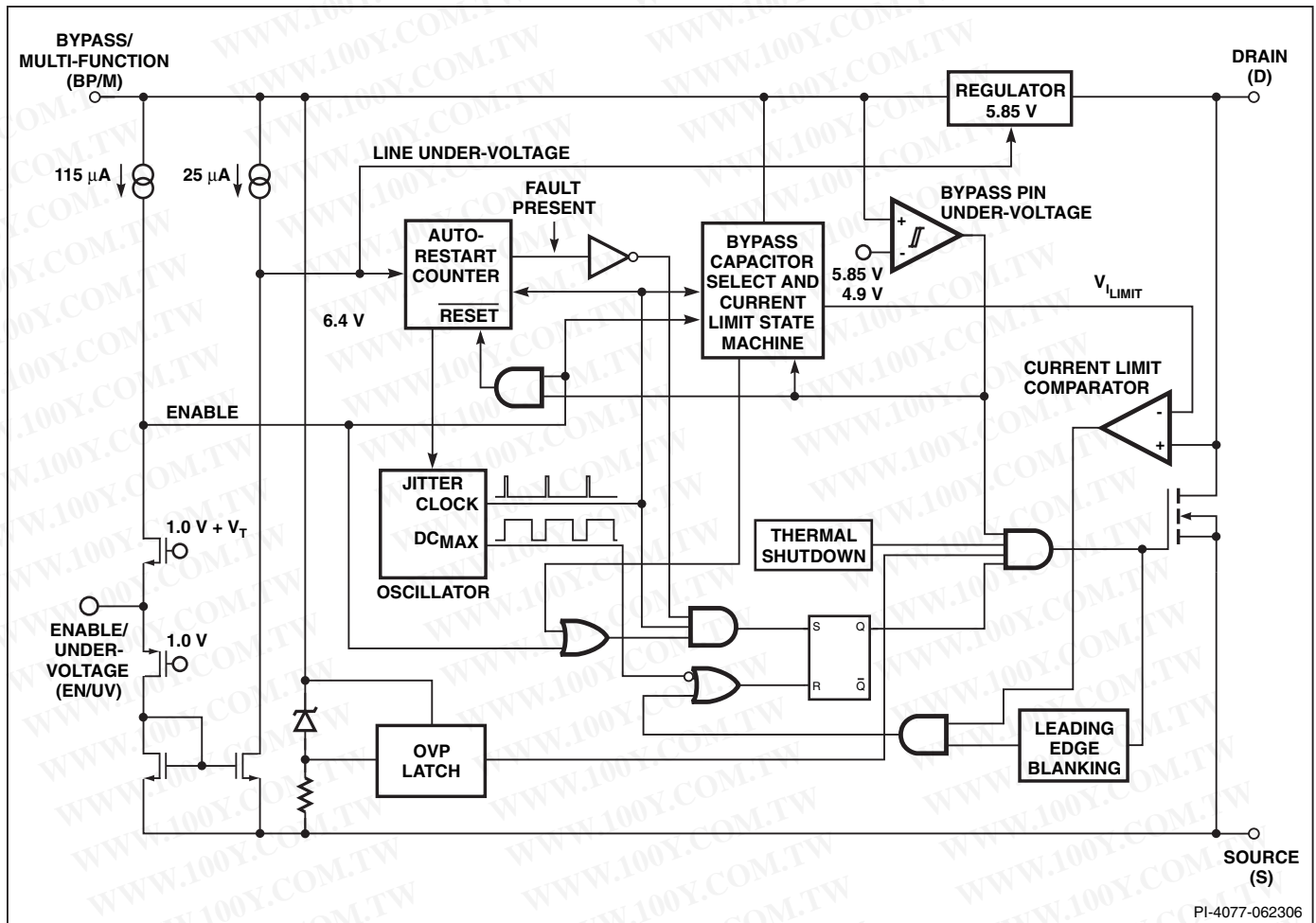
OUTPUT POWER TABLE				
PRODUCT <sup>3</sup>	230 VAC ±15%		85-265 VAC	
	Adapter <sup>1</sup>	Peak or Open Frame <sup>2</sup>	Adapter <sup>1</sup>	Peak or Open Frame <sup>2</sup>
TNY274 P or G	6 W	11 W	5 W	8.5 W
TNY275 P or G	8.5 W	15 W	6 W	11.5 W
TNY276 P or G	10 W	19 W	7 W	15 W
TNY277 P or G	13 W	23.5 W	8 W	18 W
TNY278 P or G	16 W	28 W	10 W	21.5 W
TNY279 P or G	18 W	32 W	12 W	25 W
TNY280 P or G	20 W	36.5 W	14 W	28.5 W

Table 1. Notes: 1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at 50 °C ambient. Use of an external heatsink will increase power capability 2. Minimum peak power capability in any design or minimum continuous power in an open frame design (see Key Application Considerations). 3. Packages: P: DIP-8C, G: SMD-8C. See Part Ordering Information.

- PC Standby and other auxiliary supplies
- DVD/PVR and other low power set top decoders
- Supplies for appliances, industrial systems, metering, etc.

### Description

*TinySwitch-III* incorporates a 700 V power MOSFET, oscillator, high voltage switched current source, current limit (user selectable) and thermal shutdown circuitry. The IC family uses an ON/OFF control scheme and offers a design flexible solution with a low system cost and extended power capability.



PI-4077-062306

Figure 2. Functional Block Diagram.

## Pin Functional Description

### DRAIN (D) Pin:

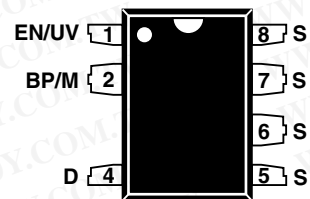
This pin is the power MOSFET drain connection. It provides internal operating current for both startup and steady-state operation.

### BYPASS/MULTI-FUNCTION (BP/M) Pin:

This pin has multiple functions:

1. It is the connection point for an external bypass capacitor for the internally generated 5.85 V supply.
2. It is a mode selector for the current limit value, depending on the value of the capacitance added. Use of a 0.1  $\mu\text{F}$  capacitor results in the standard current limit value. Use of a 1  $\mu\text{F}$  capacitor results in the current limit being reduced to that of the next smaller device size. Use of a 10  $\mu\text{F}$  capacitor results in the current limit being increased to that of the next larger device size for TNY275-280.
3. It provides a shutdown function. When the current into the bypass pin exceeds  $I_{SD}$ , the device latches off until the BP/M voltage drops below 4.9 V, during a power down. This can be used to provide an output overvoltage function

### P Package (DIP-8C) G Package (SMD-8C)



PI-4078-080905

Figure 3. Pin Configuration.

with a Zener connected from the BP/M pin to a bias winding supply.

### ENABLE/UNDERVOLTAGE (EN/UV) Pin:

This pin has dual functions: enable input and line undervoltage sense. During normal operation, switching of the power



MOSFET is controlled by this pin. MOSFET switching is terminated when a current greater than a threshold current is drawn from this pin. Switching resumes when the current being pulled from the pin drops to less than a threshold current. A modulation of the threshold current reduces group pulsing. The threshold current is between 75  $\mu\text{A}$  and 115  $\mu\text{A}$ .

The EN/UV pin also senses line undervoltage conditions through an external resistor connected to the DC line voltage. If there is no external resistor connected to this pin, *TinySwitch-III* detects its absence and disables the line undervoltage function.

**SOURCE (S) Pin:**

This pin is internally connected to the output MOSFET source for high voltage power return and control circuit common.

**TinySwitch-III Functional Description**

*TinySwitch-III* combines a high voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (pulse width modulator) controllers, it uses a simple ON/OFF control to regulate the output voltage.

The controller consists of an oscillator, enable circuit (sense and logic), current limit state machine, 5.85 V regulator, BYPASS/MULTI-FUNCTION pin undervoltage, overvoltage circuit, and current limit selection circuitry, over-temperature protection, current limit circuit, leading edge blanking, and a 700 V power MOSFET. *TinySwitch-III* incorporates additional circuitry for line undervoltage sense, auto-restart, adaptive switching cycle on-time extension, and frequency jitter. Figure 2 shows the functional block diagram with the most important features.

**Oscillator**

The typical oscillator frequency is internally set to an average of 132 kHz. Two signals are generated from the oscillator: the

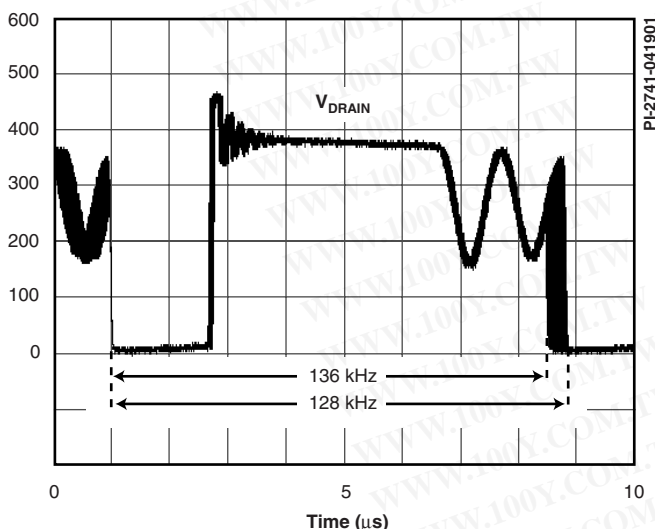


Figure 4. Frequency Jitter.

maximum duty cycle signal ( $DC_{MAX}$ ) and the clock signal that indicates the beginning of each cycle.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 8 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 4 illustrates the frequency jitter.

**Enable Input and Current Limit State Machine**

The enable input circuit at the EN/UV pin consists of a low impedance source follower output set at 1.2 V. The current through the source follower is limited to 115  $\mu\text{A}$ . When the current out of this pin exceeds the threshold current, a low logic level (disable) is generated at the output of the enable circuit, until the current out of this pin is reduced to less than the threshold current. This enable circuit output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled). If low, the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the EN/UV pin voltage or current during the remainder of the cycle are ignored.

The current limit state machine reduces the current limit by discrete amounts at light loads when *TinySwitch-III* is likely to switch in the audible frequency range. The lower current limit raises the effective switching frequency above the audio range and reduces the transformer flux density, including the associated audible noise. The state machine monitors the sequence of enable events to determine the load condition and adjusts the current limit level accordingly in discrete amounts.

Under most operating conditions (except when close to no-load), the low impedance of the source follower keeps the voltage on the EN/UV pin from going much below 1.2 V in the disabled state. This improves the response time of the optocoupler that is usually connected to this pin.

**5.85 V Regulator and 6.4 V Shunt Voltage Clamp**

The 5.85 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.85 V by drawing a current from the voltage on the DRAIN pin whenever the MOSFET is off. The BYPASS/MULTI-FUNCTION pin is the internal supply voltage node. When the MOSFET is on, the device operates from the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows *TinySwitch-III* to operate continuously from current it takes from the DRAIN pin. A bypass capacitor value of 0.1  $\mu\text{F}$  is sufficient for both high frequency decoupling and energy storage.



In addition, there is a 6.4 V shunt regulator clamping the BYPASS/MULTI-FUNCTION pin at 6.4 V when current is provided to the BYPASS/MULTI-FUNCTION pin through an external resistor. This facilitates powering of *TinySwitch-III* externally through a bias winding to decrease the no-load consumption to well below 50 mW.

**BYPASS/MULTI-FUNCTION Pin Undervoltage**

The BYPASS/MULTI-FUNCTION pin undervoltage circuitry disables the power MOSFET when the BYPASS/MULTI-FUNCTION pin voltage drops below 4.9 V in steady state operation. Once the BYPASS/MULTI-FUNCTION pin voltage drops below 4.9 V in steady state operation, it must rise back to 5.85 V to enable (turn-on) the power MOSFET.

**Over Temperature Protection**

The thermal shutdown circuitry senses the die temperature. The threshold is typically set at 142 °C with 75 °C hysteresis. When the die temperature rises above this threshold the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point it is re-enabled. A large hysteresis of 75 °C (typical) is provided to prevent overheating of the PC board due to a continuous fault condition.

**Current Limit**

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold ( $I_{LIMIT}$ ), the power MOSFET is turned off for the remainder of that cycle. The current limit state machine reduces the current limit threshold by discrete amounts under medium and light loads.

The leading edge blanking circuit inhibits the current limit comparator for a short time ( $t_{LEB}$ ) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

**Auto-Restart**

In the event of a fault condition such as output overload, output short circuit, or an open loop condition, *TinySwitch-III* enters into auto-restart operation. An internal counter clocked by the oscillator is reset every time the EN/UV pin is pulled low. If the EN/UV pin is not pulled low for 64 ms, the power MOSFET switching is normally disabled for 2.5 seconds (except in the case of line undervoltage condition, in which case it is disabled until the condition is removed). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. Figure 5 illustrates auto-restart circuit operation in the presence of an output short circuit.

In the event of a line undervoltage condition, the switching of the power MOSFET is disabled beyond its normal 2.5 seconds until the line undervoltage condition ends.

**Adaptive Switching Cycle On-Time Extension**

Adaptive switching cycle on-time extension keeps the cycle on until current limit is reached, instead of prematurely terminating after the  $DC_{MAX}$  signal goes low. This feature reduces the minimum input voltage required to maintain regulation, extending hold-up time and minimizing the size of bulk capacitor required. The on-time extension is disabled during the startup of the power supply, until the power supply output reaches regulation.

**Line Undervoltage Sense Circuit**

The DC line voltage can be monitored by connecting an external resistor from the DC line to the EN/UV pin. During power up or when the switching of the power MOSFET is disabled in auto-restart, the current into the EN/UV pin must exceed 25  $\mu A$  to initiate switching of the power MOSFET. During power up, this is accomplished by holding the BYPASS/MULTI-FUNCTION pin to 4.9 V while the line undervoltage condition exists. The BYPASS/MULTI-FUNCTION pin then rises from 4.9 V to 5.85 V when the line undervoltage condition goes away. When the switching of the power MOSFET is disabled in auto-restart mode and a line undervoltage condition exists, the auto-restart counter is stopped. This stretches the disable time beyond its normal 2.5 seconds until the line undervoltage condition ends.

The line undervoltage circuit also detects when there is no external resistor connected to the EN/UV pin (less than  $\sim 2 \mu A$  into the pin). In this case the line undervoltage function is disabled.

***TinySwitch-III* Operation**

*TinySwitch-III* devices operate in the current limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the  $DC_{MAX}$  limit is reached. Since the highest current limit level and frequency of a *TinySwitch-III* design are constant, the power delivered to the

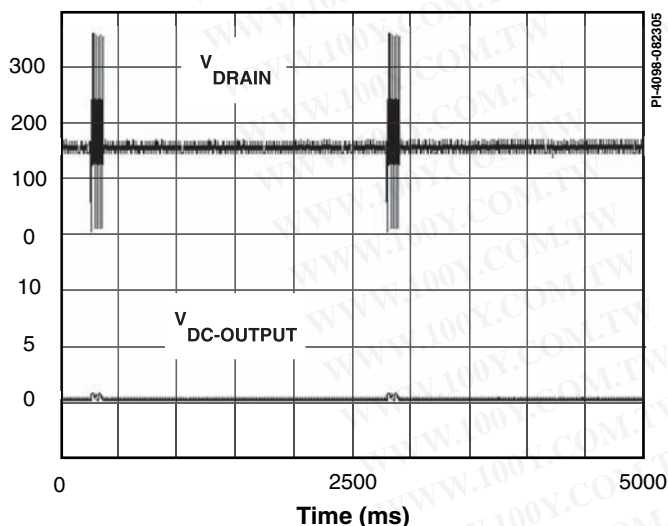


Figure 5. Auto-Restart Operation.



load is proportional to the primary inductance of the transformer and peak primary current squared. Hence, designing the supply involves calculating the primary inductance of the transformer for the maximum output power required. If the *TinySwitch-III* is appropriately chosen for the power level, the current in the calculated inductance will ramp up to current limit before the  $DC_{MAX}$  limit is reached.

**Enable Function**

*TinySwitch-III* senses the EN/UV pin to determine whether or

not to proceed with the next switching cycle. The sequence of cycles is used to determine the current limit. Once a cycle is started, it always completes the cycle (even when the EN/UV pin changes state half way through the cycle). This operation results in a power supply in which the output voltage ripple is determined by the output capacitor, amount of energy per switch cycle and the delay of the feedback.

The EN/UV pin signal is generated on the secondary by comparing the power supply output voltage with a reference voltage. The EN/UV pin signal is high when the power supply output voltage is less than the reference voltage.

In a typical implementation, the EN/UV pin is driven by an optocoupler. The collector of the optocoupler transistor is connected to the EN/UV pin and the emitter is connected to the SOURCE pin. The optocoupler LED is connected in series with a Zener diode across the DC output voltage to be regulated. When the output voltage exceeds the target regulation voltage level (optocoupler LED voltage drop plus Zener voltage), the optocoupler LED will start to conduct, pulling the EN/UV pin low. The Zener diode can be replaced by a TL431 reference circuit for improved accuracy.

**ON/OFF Operation with Current Limit State Machine**

The internal clock of the *TinySwitch-III* runs all the time. At the beginning of each clock cycle, it samples the EN/UV pin to decide whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine sets the current limit to reduced values.

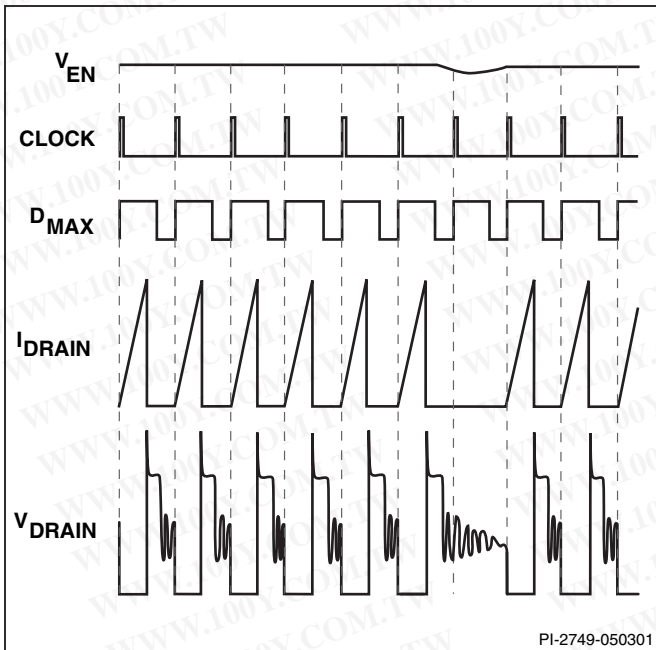


Figure 6. Operation at Near Maximum Loading.

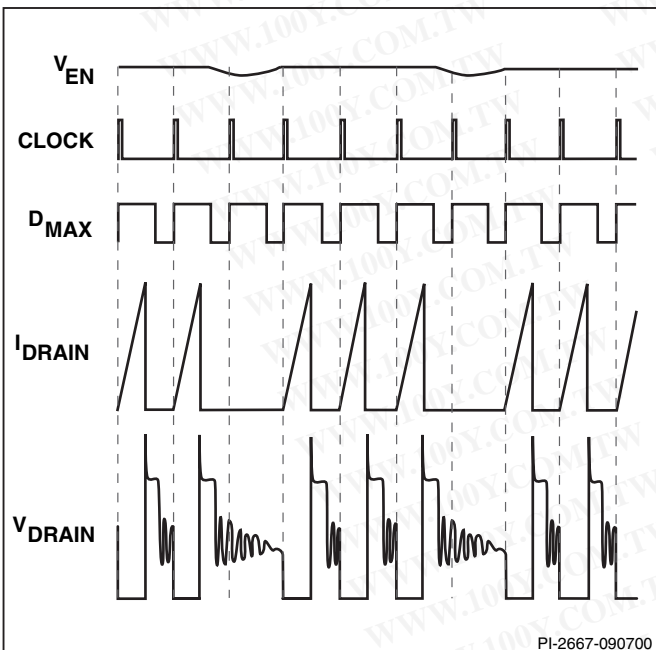


Figure 7. Operation at Moderately Heavy Loading.

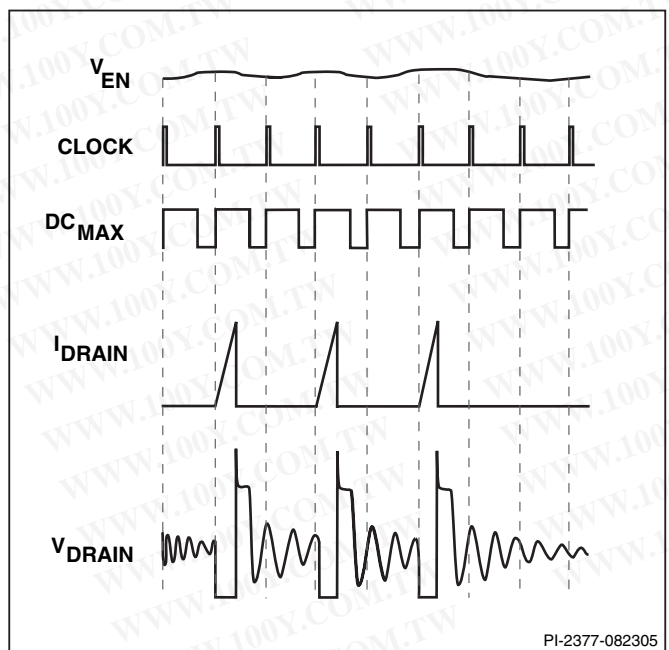


Figure 8. Operation at Medium Loading.



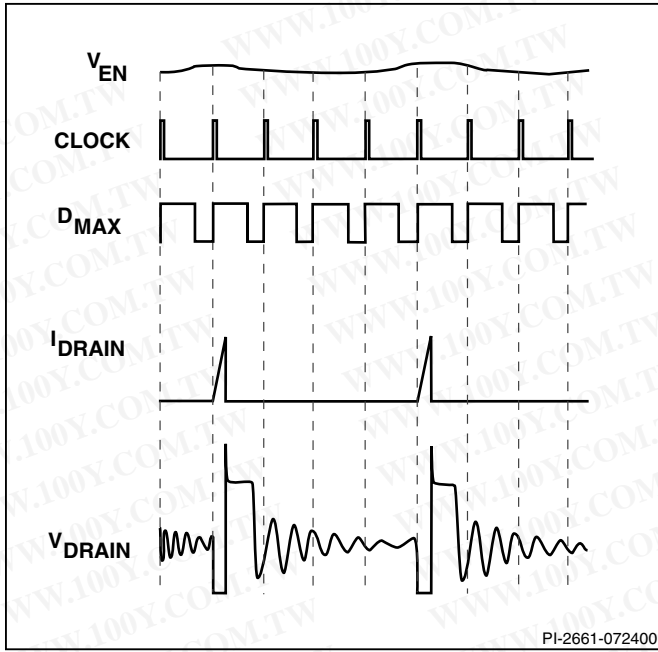


Figure 9. Operation at Very Light Load.

At near maximum load, *TinySwitch-III* will conduct during nearly all of its clock cycles (Figure 6). At slightly lower load, it will “skip” additional cycles in order to maintain voltage regulation at the power supply output (Figure 7). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 8). At very light loads, the current limit will be reduced even further (Figure 9). Only a small percentage of cycles will occur to satisfy the power consumption of the power supply.

The response time of the ON/OFF control scheme is very fast compared to PWM control. This provides tight regulation and excellent transient response.

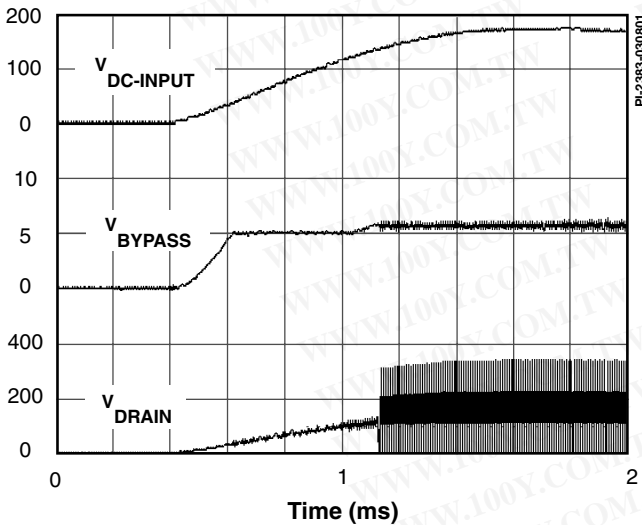


Figure 10. Power Up with Optional External UV Resistor (4 MΩ) Connected to EN/UV Pin.

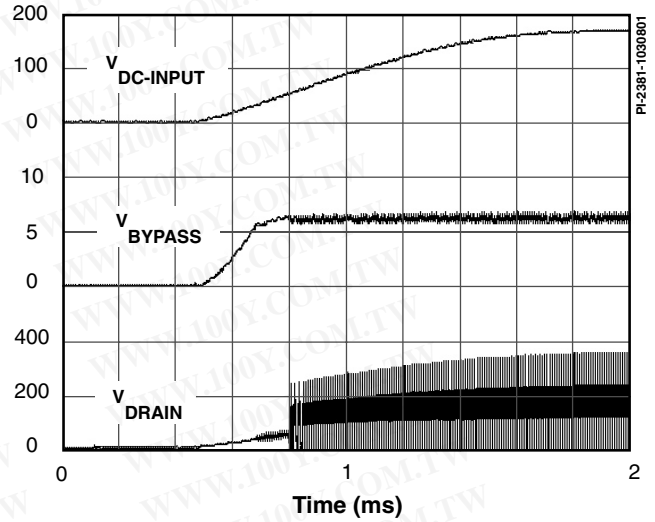


Figure 11. Power Up Without Optional External UV Resistor Connected to EN/UV Pin.

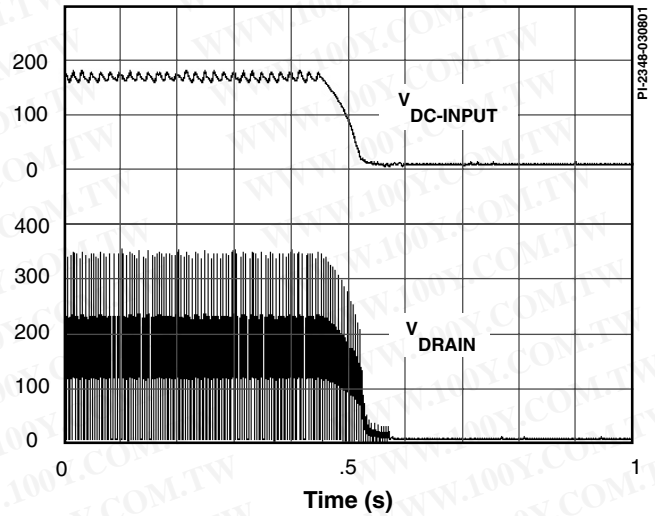


Figure 12. Normal Power Down Timing (without UV).

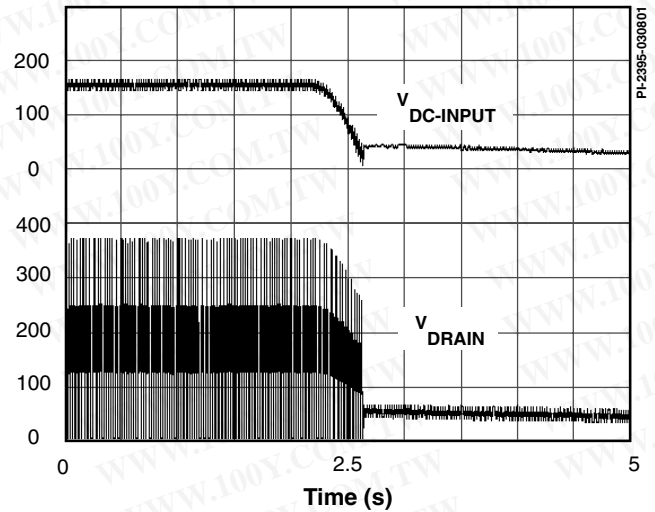


Figure 13. Slow Power Down Timing with Optional External (4 MΩ) UV Resistor Connected to EN/UV Pin.



### Power Up/Down

The *TinySwitch-III* requires only a 0.1  $\mu\text{F}$  capacitor on the BYPASS/MULTI-FUNCTION pin to operate with standard current limit. Because of its small size, the time to charge this capacitor is kept to an absolute minimum, typically 0.6 ms. The time to charge will vary in proportion to the BYPASS/MULTI-FUNCTION pin capacitor value when selecting different current limits. Due to the high bandwidth of the ON/OFF feedback, there is no overshoot at the power supply output. When an external resistor (4  $\text{M}\Omega$ ) is connected from the positive DC input to the EN/UV pin, the power MOSFET switching will be delayed during power up until the DC line voltage exceeds the threshold (100 V). Figures 10 and 11 show the power up timing waveform in applications with and without an external resistor (4  $\text{M}\Omega$ ) connected to the EN/UV pin.

Under startup and overload conditions, when the conduction time is less than 400 ns, the device reduces the switching frequency to maintain control of the peak drain current.

During power down, when an external resistor is used, the power MOSFET will switch for 64 ms after the output loses regulation. The power MOSFET will then remain off without any glitches since the undervoltage function prohibits restart when the line voltage is low.

Figure 12 illustrates a typical power down timing waveform. Figure 13 illustrates a very slow power down timing waveform as in standby applications. The external resistor (4  $\text{M}\Omega$ ) is connected to the EN/UV pin in this case to prevent unwanted restarts.

No bias winding is needed to provide power to the chip because it draws the power directly from the DRAIN pin (see

Functional Description above). This has two main benefits. First, for a nominal application, this eliminates the cost of a bias winding and associated components. Secondly, for battery charger applications, the current-voltage characteristic often allows the output voltage to fall close to zero volts while still delivering power. *TinySwitch-III* accomplishes this without a forward bias winding and its many associated components. For applications that require very low no-load power consumption (50 mW), a resistor from a bias winding to the BYPASS/MULTI-FUNCTION pin can provide the power to the chip. The minimum recommended current supplied is 1 mA. The BYPASS/MULTI-FUNCTION pin in this case will be clamped at 6.4 V. This method will eliminate the power draw from the DRAIN pin, thereby reducing the no-load power consumption and improving full-load efficiency.

### Current Limit Operation

Each switching cycle is terminated when the DRAIN current reaches the current limit of the device. Current limit operation provides good line ripple rejection and relatively constant power delivery independent of input voltage.

### BYPASS/MULTI-FUNCTION Pin Capacitor

The BYPASS/MULTI-FUNCTION pin can use a ceramic capacitor as small as 0.1  $\mu\text{F}$  for decoupling the internal power supply of the device. A larger capacitor size can be used to adjust the current limit. For TNY275-280, a 1  $\mu\text{F}$  BP/M pin capacitor will select a lower current limit equal to the standard current limit of the next smaller device and a 10  $\mu\text{F}$  BP/M pin capacitor will select a higher current limit equal to the standard current limit of the next larger device. The higher current limit level of the TNY280 is set to 850 mA typical. The TNY274 MOSFET does not have the capability for increased current limit so this feature is not available in this device.

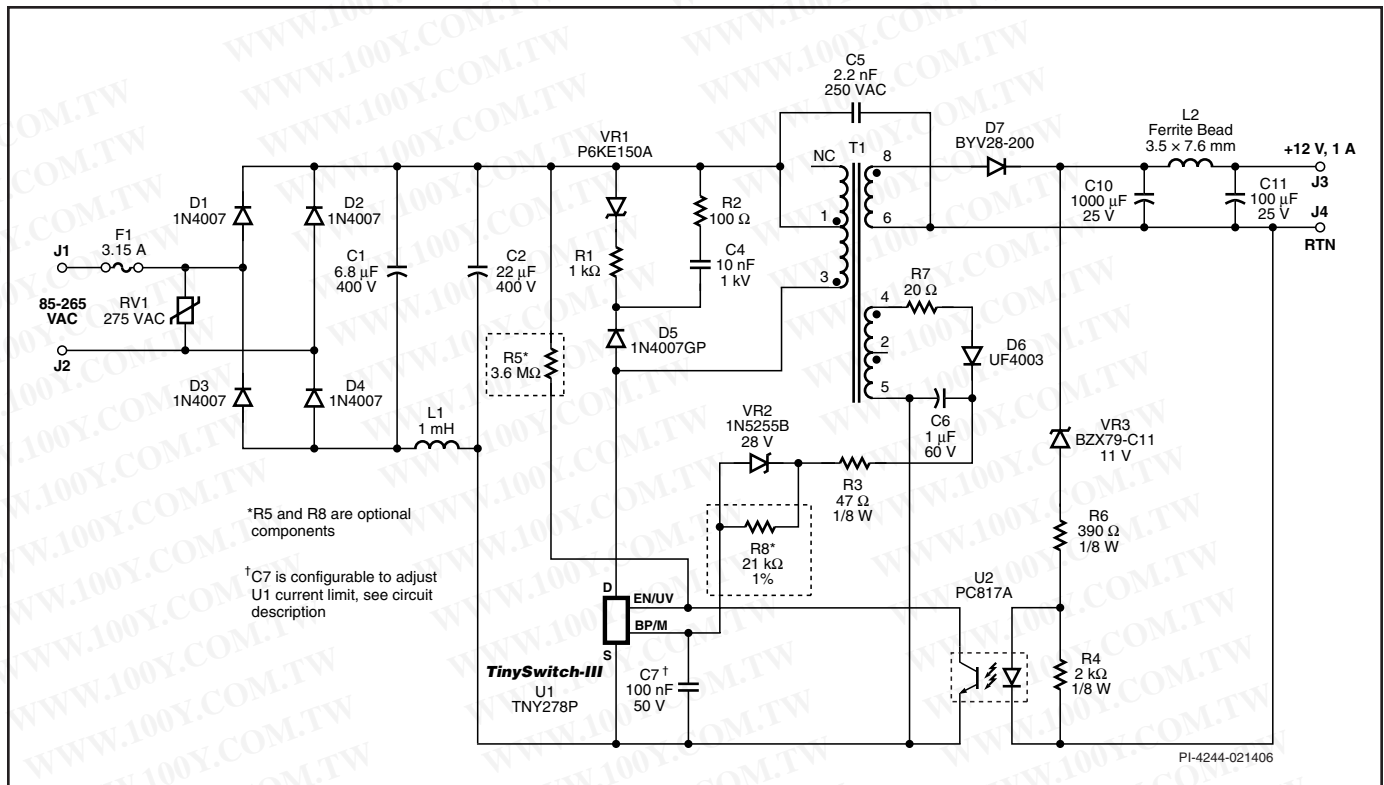


Figure 14. TNY278P, 12 V, 1 A Universal Input Power Supply.

## Applications Example

The circuit shown in Figure 14 is a low cost, high efficiency, flyback power supply designed for 12 V, 1 A output from universal input using the TNY278.

The supply features undervoltage lockout, primary sensed output overvoltage latching shutdown protection, high efficiency (>80%), and very low no-load consumption (<50 mW at 265 VAC). Output regulation is accomplished using a simple zener reference and optocoupler feedback.

The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated MOSFET in U1. Diode D5, C2, R1, R2, and VR1 comprise the clamp circuit, limiting the leakage inductance turn-off voltage spike on the DRAIN pin to a safe value. The use of a combination of a Zener clamp and parallel RC optimizes both EMI and energy efficiency. Resistor R2 allows the use of a slow recovery, low cost, rectifier diode by limiting the reverse current through D5. The selection of a slow diode also improves efficiency and conducted EMI but should be a glass passivated type, with a specified recovery time of  $\leq 2 \mu\text{s}$ .

The output voltage is regulated by the Zener diode VR3. When the output voltage exceeds the sum of the Zener and optocoupler

LED forward drop, current will flow in the optocoupler LED. This will cause the transistor of the optocoupler to sink current. When this current exceeds the ENABLE pin threshold current the next switching cycle is inhibited. When the output voltage falls below the feedback threshold, a conduction cycle is allowed to occur and, by adjusting the number of enabled cycles, output regulation is maintained. As the load reduces, the number of enabled cycles decreases, lowering the effective switching frequency and scaling switching losses with load. This provides almost constant efficiency down to very light loads, ideal for meeting energy efficiency requirements.

As the *TinySwitch-III* devices are completely self-powered, there is no requirement for an auxiliary or bias winding on the transformer. However by adding a bias winding, the output overvoltage protection feature can be configured, protecting the load against open feedback loop faults.

When an overvoltage condition occurs, such that bias voltage exceeds the sum of VR2 and the BYPASS/MULTIFUNCTION (BP/M) pin voltage (28 V+5.85 V), current begins to flow into the BP/M pin. When this current exceeds  $I_{SD}$  the internal latching shutdown circuit in *TinySwitch-III* is activated. This condition is reset when the BP/M pin voltage drops below 2.6 V after removal of the AC input. In the example shown, on opening the loop, the OVP trips at an output of 17 V.

For lower no-load input power consumption, the bias winding may also be used to supply the *TinySwitch-III* device. Resistor R8 feeds current into the BP/M pin, inhibiting the internal high voltage current source that normally maintains the BP/M pin capacitor voltage (C7) during the internal MOSFET off time. This reduces the no-load consumption of this design from 140 mW to 40 mW at 265 VAC.

Undervoltage lockout is configured by R5 connected between the DC bus and EN/UV pin of U1. When present, switching is inhibited until the current in the EN/UV pin exceeds 25  $\mu$ A. This allows the startup voltage to be programmed within the normal operating input voltage range, preventing glitching of the output under abnormal low voltage conditions and also on removal of the AC input.

In addition to the simple input pi filter (C1, L1, C2) for differential mode EMI, this design makes use of *E-Shield™* shielding techniques in the transformer to reduce common mode EMI displacement currents, and R2 and C4 as a damping network to reduce high frequency transformer ringing. These techniques, combined with the frequency jitter of TNY278, give excellent conducted and radiated EMI performance with this design achieving >12 dB $\mu$ V of margin to EN55022 Class B conducted EMI limits.

For design flexibility the value of C7 can be selected to pick one of the 3 current limits options in U1. This allows the designer to select the current limit appropriate for the application.

- Standard current limit ( $I_{LIMIT}$ ) is selected with a 0.1  $\mu$ F BP/M pin capacitor and is the normal choice for typical enclosed adapter applications.
- When a 1  $\mu$ F BP/M pin capacitor is used, the current limit is reduced ( $I_{LIMITred}$  or  $I_{LIMIT}-1$ ) offering reduced RMS device currents and therefore improved efficiency, but at the expense of maximum power capability. This is ideal for thermally challenging designs where dissipation must be minimized.
- When a 10  $\mu$ F BP/M pin capacitor is used, the current limit is increased ( $I_{LIMITinc}$  or  $I_{LIMIT}+1$ ), extending the power capability for applications requiring higher peak power or continuous power where the thermal conditions allow.

Further flexibility comes from the current limits between adjacent *TinySwitch-III* family members being compatible. The reduced current limit of a given device is equal to the standard current limit of the next smaller device and the increased current limit is equal to the standard current limit of the next larger device.

## Key Application Considerations

### *TinySwitch-III* Design Considerations

#### Output Power Table

The data sheet output power table (Table 1) represents the minimum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 100 V or higher for 85 VAC input, or 220 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be sized to meet these criteria for AC input designs.
2. Efficiency of 75%.
3. Minimum data sheet value of P<sub>f</sub>.
4. Transformer primary inductance tolerance of  $\pm 10\%$ .
5. Reflected output voltage ( $V_{OR}$ ) of 135 V.
6. Voltage only output of 12 V with a fast PN rectifier diode.
7. Continuous conduction mode operation with transient  $K_p^*$  value of 0.25.
8. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
9. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heatsink is used to keep the SOURCE pin temperature at or below 110 °C.
10. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.

\*Below a value of 1,  $K_p$  is the ratio of ripple to peak primary current. To prevent reduced power capability due to premature termination of switching cycles a transient  $K_p$  limit of  $\geq 0.25$  is recommended. This prevents the initial current limit ( $I_{INIT}$ ) from being exceeded at MOSFET turn on.

For reference, Table 2 provides the minimum practical power delivered from each family member at the three selectable current limit values. This assumes open frame operation (not thermally limited) and otherwise the same conditions as listed above. These numbers are useful to identify the correct current limit to select for a given device and output power requirement.

#### Overvoltage Protection

The output overvoltage protection provided by *TinySwitch-III* uses an internal latch that is triggered by a threshold current of approximately 5.5 mA into the BP/M pin. In addition to an internal filter, the BP/M pin capacitor forms an external filter providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and BP/M pins of the device.



OUTPUT POWER TABLE						
PRODUCT	230 VAC ±15%			85-265 VAC		
	$I_{LIMIT-1}$	$I_{LIMIT}$	$I_{LIMIT+1}$	$I_{LIMIT-1}$	$I_{LIMIT}$	$I_{LIMIT+1}$
TNY274 P or G	9	10.9	9.1	7.1	8.5	7.1
TNY275 P or G	10.8	12	15.1	8.4	9.3	11.8
TNY276 P or G	11.8	15.3	19.4	9.2	11.9	15.1
TNY277 P or G	15.1	19.6	23.7	11.8	15.3	18.5
TNY278 P or G	19.4	24	28	15.1	18.6	21.8
TNY279 P or G	23.7	28.4	32.2	18.5	22	25.2
TNY280 P or G	28	32.7	36.6	21.8	25.4	28.5

Table 2. Minimum Practical Power at Three Selectable Current Limit Levels.

For best performance of the OVP function, it is recommended that a relatively high bias winding voltage is used, in the range of 15 V-30 V. This minimizes the error voltage on the bias winding due to leakage inductance and also ensures adequate voltage during no-load operation from which to supply the BP/M pin for reduced no-load consumption.

Selecting the Zener diode voltage to be approximately 6 V above the bias winding voltage (28 V for 22 V bias winding) gives good OVP performance for most designs, but can be adjusted to compensate for variations in leakage inductance. Adding additional filtering can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the bias winding diode and/or the OVP Zener as shown by R7 and R3 in Figure 14. The resistor in series with the OVP Zener also limits the maximum current into the BP/M pin.

**Reducing No-load Consumption**

As *TinySwitch-III* is self-powered from the BP/M pin capacitor, there is no need for an auxillary or bias winding to be provided on the transformer for this purpose. Typical no-load consumption when self-powered is <150 mW at 265 VAC input. The addition of a bias winding can reduce this down to <50 mW by supplying the *TinySwitch-III* from the lower bias voltage and inhibiting the internal high voltage current source. To achieve this, select the value of the resistor (R8 in Figure 14) to provide the data sheet DRAIN supply current. In practice, due to the reduction of the bias voltage at low load, start with a value equal to 40% greater than the data sheet maximum current, and then increase the value of the resistor to give the lowest no-load consumption.

**Audible Noise**

The cycle skipping mode of operation used in *TinySwitch-III* can generate audio frequency components in the transformer. To limit this audible noise generation the transformer should be designed such that the peak core flux density is below 3000 Gauss (300 mT). Following this guideline and using the

standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

Ceramic capacitors that use dielectrics such as Z5U, when used in clamp circuits, may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction, for example a film type.

***TinySwitch-III* Layout Considerations**

**Layout**

See Figure 15 for a recommended circuit board layout for *TinySwitch-III*.

**Single Point Grounding**

Use a single point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

**Bypass Capacitor (C<sub>BP</sub>)**

The BP/M pin capacitor should be located as near as possible to the BP/M and SOURCE pins.

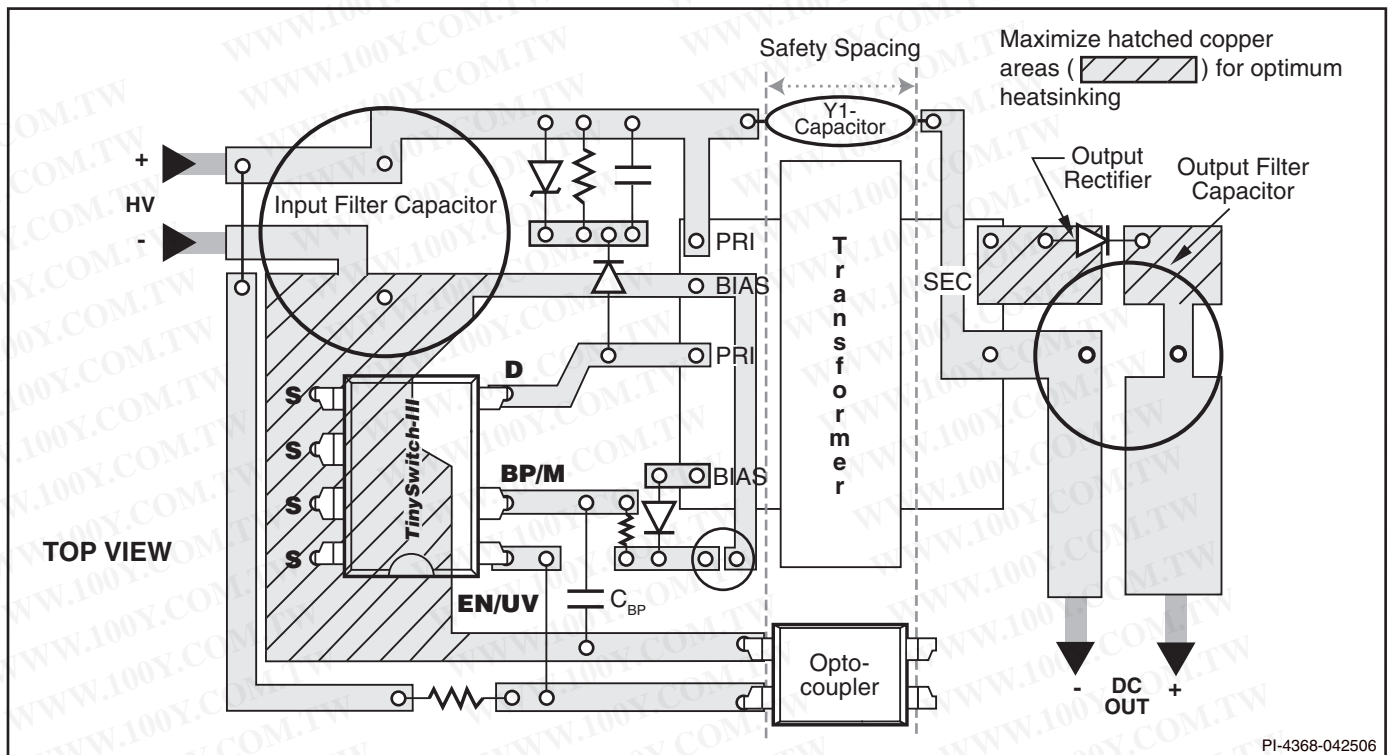
**EN/UV Pin**

Keep traces connected to the EN/UV pin short and, as far as is practical, away from all other traces and nodes above source potential including, but not limited to, the BYPASS and DRAIN pins.

**Primary Loop Area**

The area of the primary loop that connects the input filter capacitor, transformer primary and *TinySwitch-III* together should be kept as small as possible.





PI-4368-042506

Figure 15. Recommended Circuit Board Layout for TinySwitch-III with Undervoltage Lock Out Resistor.

### Primary Clamp Circuit

A clamp is used to limit peak voltage on the DRAIN pin at turn off. This can be achieved by using an RCD clamp or a Zener (~200 V) and diode clamp across the primary winding. In all cases, to minimize EMI, care should be taken to minimize the circuit path from the clamp components to the transformer and *TinySwitch-III*.

### Thermal Considerations

The four SOURCE pins are internally connected to the IC lead frame and provide the main path to remove heat from the device. Therefore all the SOURCE pins should be connected to a copper area underneath the *TinySwitch-III* to act not only as a single point ground, but also as a heatsink. As this area is connected to the quiet source node, this area should be maximized for good heatsinking. Similarly for axial output diodes, maximize the PCB area connected to the cathode.

### Y-Capacitor

The placement of the Y-capacitor should be directly from the primary input filter capacitor positive terminal to the common/return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the *TinySwitch-III* device. Note – if an input  $\pi$  (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

### Optocoupler

Place the optocoupler physically close to the *TinySwitch-III* to minimizing the primary-side trace lengths. Keep the high current, high voltage drain and clamp traces away from the optocoupler to prevent noise pick up.

### Output Diode

For best performance, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor, should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for heatsinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

### PC Board Leakage Currents

*TinySwitch-III* is designed to optimize energy efficiency across the power range and particularly in standby/no-load conditions. Current consumption has therefore been minimized to achieve this performance. The EN/UV pin undervoltage feature for example has a low threshold (~1  $\mu$ A) to detect whether an undervoltage resistor is present.

Parasitic leakage currents into the EN/UV pin are normally well below this 1  $\mu$ A threshold when PC board assembly is in a well controlled production facility. However, high humidity conditions together with board and/or package contamination,



either from no-clean flux or other contaminants, can reduce the surface resistivity enough to allow parasitic currents  $>1 \mu\text{A}$  to flow into the EN/UV pin. These currents can flow from higher voltage exposed solder pads close to the EN/UV pin such as the BP/M pin solder pad preventing the design from starting up. Designs that make use of the undervoltage lockout feature by connecting a resistor from the high voltage rail to the EN/UV pin are not affected.

If the contamination levels in the PC board assembly facility are unknown, the application is open frame or operates in a high pollution degree environment and the design does not make use of the undervoltage lockout feature, then an optional 390 k $\Omega$  resistor should be added from EN/UV pin to SOURCE pin to ensure that the parasitic leakage current into the EN/UV pin is well below 1  $\mu\text{A}$ .

Note that typical values for surface insulation resistance (SIR) where no-clean flux has been applied according to the suppliers' guidelines are  $\gg 10 \text{ M}\Omega$  and do not cause this issue.

### Quick Design Checklist

As with any power supply design, all *TinySwitch-III* designs should be verified on the bench to make sure that component specifications are not exceeded under worst case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that  $V_{\text{DS}}$  does not exceed 650 V at highest input voltage and peak (overload) output power. The 50 V margin to the 700 V  $BV_{\text{DSS}}$  specification gives margin for design variation.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at startup. Repeat under steady state conditions and verify that the leading edge current spike event is below  $I_{\text{LIMIT(Min)}}$  at the end of the  $t_{\text{LEB(Min)}}$ . Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for *TinySwitch-III*, transformer, output diode, and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the  $R_{\text{DS(ON)}}$  of *TinySwitch-III* as specified in the data sheet. Under low line, maximum power, a maximum *TinySwitch-III* SOURCE pin temperature of 110 °C is recommended to allow for these variations.

### Design Tools

Up-to-date information on design tools is available at the Power Integrations website: [www.powerint.com](http://www.powerint.com).

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

**ABSOLUTE MAXIMUM RATINGS<sup>(1,5)</sup>**

DRAIN Voltage .....	-0.3 V to 700 V	Lead Temperature <sup>(4)</sup> .....	260 °C
DRAIN Peak Current: TNY274.....	400 (750) mA <sup>(2)</sup>	<b>Notes:</b>	
TNY275.....	560 (1050) mA <sup>(2)</sup>	1. All voltages referenced to SOURCE, T <sub>A</sub> = 25 °C.	
TNY276.....	720 (1350) mA <sup>(2)</sup>	2. The higher peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.	
TNY277.....	880 (1650) mA <sup>(2)</sup>	3. Normally limited by internal circuitry.	
TNY278.....	1040 (1950) mA <sup>(2)</sup>	4. 1/16 in. from case for 5 seconds.	
TNY279 .....	1200 (2250) mA <sup>(2)</sup>	5. Maximum ratings specified may be applied one at a time, without causing permanent damage to the product.	
TNY280 .....	1360 (2550) mA <sup>(2)</sup>	Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.	
EN/UV Voltage .....	-0.3 V to 9 V		
EN/UV Current .....	100 mA		
BP/M Voltage .....	-0.3 V to 9 V		
Storage Temperature .....	-65 °C to 150 °C		
Operating Junction Temperature <sup>(3)</sup> .....	-40 °C to 150 °C		

**THERMAL IMPEDANCE**

Thermal Impedance: P or G Package:	<b>Notes:</b>
(θ <sub>JA</sub> ) .....	1. Measured on the SOURCE pin close to plastic interface.
(θ <sub>JC</sub> ) <sup>(1)</sup> .....	2. Soldered to 0.36 sq. in. (232 mm <sup>2</sup> ), 2 oz. (610 g/m <sup>2</sup> ) copper clad.
	3. Soldered to 1 sq. in. (645 mm <sup>2</sup> ), 2 oz. (610 g/m <sup>2</sup> ) copper clad.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
		SOURCE = 0 V; T <sub>J</sub> = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)				

**CONTROL FUNCTIONS**

Output Frequency in Standard Mode	f <sub>OSC</sub>	T <sub>J</sub> = 25 °C See Figure 4	Average	124	132	140	kHz
			Peak-to-peak Jitter		8		
Maximum Duty Cycle	DC <sub>MAX</sub>	S1 Open		62	65		%
EN/UV Pin Upper Turnoff Threshold Current	I <sub>DIS</sub>			-150	-115	-90	µA
EN/UV Pin Voltage	V <sub>EN</sub>	I <sub>EN/UV</sub> = 25 µA		1.8	2.2	2.6	V
		I <sub>EN/UV</sub> = -25 µA		0.8	1.2	1.6	
DRAIN Supply Current	I <sub>S1</sub>	EN/UV Current > I <sub>DIS</sub> (MOSFET Not Switching) See Note A			290		µA
	I <sub>S2</sub>	EN/UV Open (MOSFET Switching at f <sub>OSC</sub> ) See Note B	TNY274		275	360	µA
			TNY275		295	400	
			TNY276		310	430	
			TNY277		365	460	
			TNY278		445	540	
			TNY279		510	640	
TNY280		630	760				



Parameter	Symbol	Conditions		Min	Typ	Max	Units
		SOURCE = 0 V; T <sub>J</sub> = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)					
<b>CONTROL FUNCTIONS (cont.)</b>							
BP/M Pin Charge Current	I <sub>CH1</sub>	V <sub>BP/M</sub> = 0 V, T <sub>J</sub> = 25 °C See Note C, D	TNY274	-6	-3.8	-1.8	mA
			TNY275-279	-8.3	-5.4	-2.5	
			TNY280	-9.7	-6.8	-3.9	
	I <sub>CH2</sub>	V <sub>BP/M</sub> = 4 V, T <sub>J</sub> = 25 °C See Note C, D	TNY274	-4.1	-2.3	-1	
			TNY275-279	-5	-3.5	-1.5	
			TNY280	-6.6	-4.6	-2.1	
BP/M Pin Voltage	V <sub>BP/M</sub>	See Note C	5.6	5.85	6.15	V	
BP/M Pin Voltage Hysteresis	V <sub>BP/MH</sub>		0.80	0.95	1.20	V	
BP/M Pin Shunt Voltage	V <sub>SHUNT</sub>	I <sub>BP</sub> = 2 mA	6.0	6.4	6.7	V	
EN/UV Pin Line Undervoltage Threshold	I <sub>LUV</sub>	T <sub>J</sub> = 25 °C	22.5	25	27.5	μA	
<b>CIRCUIT PROTECTION</b>							
Standard Current Limit (BP/M Capacitor = 0.1 μF) See Note D	I <sub>LIMIT</sub>	di/dt = 50 mA/μs T <sub>J</sub> = 25 °C See Note E	TNY274P	233	250	267	mA
			TNY274G	233	250	273	
		di/dt = 55 mA/μs T <sub>J</sub> = 25 °C See Note E	TNY275P	256	275	294	
			TNY275G	256	275	300	
		di/dt = 70 mA/μs T <sub>J</sub> = 25 °C See Note E	TNY276P	326	350	374	
			TNY276G	326	350	382	
		di/dt = 90 mA/μs T <sub>J</sub> = 25 °C See Note E	TNY277P	419	450	481	
			TNY277G	419	450	491	
		di/dt = 110 mA/μs T <sub>J</sub> = 25 °C See Note E	TNY278P	512	550	588	
			TNY278G	512	550	600	
		di/dt = 130 mA/μs T <sub>J</sub> = 25 °C See Note E	TNY279P	605	650	695	
			TNY279G	605	650	709	
		di/dt = 150 mA/μs T <sub>J</sub> = 25 °C See Note E	TNY280P	698	750	802	
			TNY280G	698	750	818	



Parameter	Symbol	Conditions		Min	Typ	Max	Units			
		SOURCE = 0 V; T <sub>J</sub> = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)								
<b>CIRCUIT PROTECTION (cont.)</b>										
Reduced Current Limit (BP/M Capacitor = 1 μF) See Note D	I <sub>LIMITred</sub>	di/dt = 50 mA/μs T <sub>J</sub> = 25 °C See Note E	TNY274P	196	210	233	mA			
			TNY274G	196	210	237				
		di/dt = 55 mA/μs T <sub>J</sub> = 25 °C See Note E	TNY275P	233	250	277				
			TNY275G	233	250	283				
		di/dt = 70 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY276P	256	275	305				
			TNY276G	256	275	311				
		di/dt = 90 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY277P	326	350	388				
			TNY277G	326	350	396				
		di/dt = 110 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY278P	419	450	499				
			TNY278G	419	450	509				
		di/dt = 130 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY279P	512	550	610				
			TNY279G	512	550	622				
		di/dt = 150 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY280P	605	650	721				
			TNY280G	605	650	735				
		Increased Current Limit (BP/M Capacitor = 10 μF) See Note D	I <sub>LIMITinc</sub>	di/dt = 50 mA/μs T <sub>J</sub> = 25 °C See Notes E, F	TNY274P	196		210	233	mA
					TNY274G	196		210	237	
di/dt = 55 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY275P			326	350	388				
	TNY275G			326	350	396				
di/dt = 70 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY276P			419	450	499				
	TNY276G			419	450	509				
di/dt = 90 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY277P			512	550	610				
	TNY277G			512	550	622				
di/dt = 110 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY278P			605	650	721				
	TNY278G			605	650	735				
di/dt = 130 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY279P			698	750	833				
	TNY279G			698	750	848				
di/dt = 150 mA/μs T <sub>J</sub> = 25 °C See Notes E	TNY280P			791	850	943				
	TNY280G			791	850	961				



Parameter	Symbol	Conditions		Min	Typ	Max	Units
		SOURCE = 0 V; T <sub>J</sub> = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)					
<b>CIRCUIT PROTECTION (cont.)</b>							
Power Coefficient	I <sup>2</sup> <sub>f</sub>	Standard Current Limit, I <sup>2</sup> <sub>f</sub> = I <sub>LIMIT(TYP)</sub> <sup>2</sup> × f <sub>OSC(TYP)</sub>	TNY274-280P	0.9 × I <sup>2</sup> <sub>f</sub>	I <sup>2</sup> <sub>f</sub>	1.12 × I <sup>2</sup> <sub>f</sub>	A <sup>2</sup> Hz
			TNY274-280G	0.9 × I <sup>2</sup> <sub>f</sub>	I <sup>2</sup> <sub>f</sub>	1.16 × I <sup>2</sup> <sub>f</sub>	
		Reduced Current Limit, I <sup>2</sup> <sub>f</sub> = I <sub>LIMITred(TYP)</sub> <sup>2</sup> × f <sub>OSC(TYP)</sub>	TNY274-280P	0.9 × I <sup>2</sup> <sub>f</sub>	I <sup>2</sup> <sub>f</sub>	1.16 × I <sup>2</sup> <sub>f</sub>	
			TNY274-280G	0.9 × I <sup>2</sup> <sub>f</sub>	I <sup>2</sup> <sub>f</sub>	1.20 × I <sup>2</sup> <sub>f</sub>	
		Increased Current Limit, I <sup>2</sup> <sub>f</sub> = I <sub>LIMITinc(TYP)</sub> <sup>2</sup> × f <sub>OSC(TYP)</sub>	TNY274-280P	0.9 × I <sup>2</sup> <sub>f</sub>	I <sup>2</sup> <sub>f</sub>	1.16 × I <sup>2</sup> <sub>f</sub>	
			TNY274-280G	0.9 × I <sup>2</sup> <sub>f</sub>	I <sup>2</sup> <sub>f</sub>	1.20 × I <sup>2</sup> <sub>f</sub>	
Initial Current Limit	I <sub>INIT</sub>	See Figure 19 T <sub>J</sub> = 25 °C, See Note G		0.75 × I <sub>LIMIT(MIN)</sub>			mA
Leading Edge Blanking Time	t <sub>LEB</sub>	T <sub>J</sub> = 25 °C See Note G		170	215		ns
Current Limit Delay	t <sub>ILD</sub>	T <sub>J</sub> = 25 °C See Note G, H			150		ns
Thermal Shut-down Temperature	T <sub>SD</sub>			135	142	150	°C
Thermal Shut-down Hysteresis	T <sub>SDH</sub>				75		°C
BP/M Pin Shut-down Threshold Current	I <sub>SD</sub>			4	6.5	9	mA
BP/M Pin Power up Reset Threshold Voltage	V <sub>BP/M(RESET)</sub>			1.6	2.6	3.6	V
<b>OUTPUT</b>							
ON-State Resistance	R <sub>DS(ON)</sub>	TNY274 I <sub>D</sub> = 25 mA	T <sub>J</sub> = 25 °C		28	32	Ω
			T <sub>J</sub> = 100 °C		42	48	
		TNY275 I <sub>D</sub> = 28 mA	T <sub>J</sub> = 25 °C		19	22	
			T <sub>J</sub> = 100 °C		29	33	
		TNY276 I <sub>D</sub> = 35 mA	T <sub>J</sub> = 25 °C		14	16	
			T <sub>J</sub> = 100 °C		21	24	

Parameter	Symbol	Conditions		Min	Typ	Max	Units
		SOURCE = 0 V; T <sub>J</sub> = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)					
<b>OUTPUT (cont.)</b>							
ON-State Resistance	R <sub>DS(ON)</sub>	TNY277 I <sub>D</sub> = 45 mA	T <sub>J</sub> = 25 °C		7.8	9.0	Ω
			T <sub>J</sub> = 100 °C		11.7	13.5	
		TNY278 I <sub>D</sub> = 55 mA	T <sub>J</sub> = 25 °C		5.2	6.0	
			T <sub>J</sub> = 100 °C		7.8	9.0	
		TNY279 I <sub>D</sub> = 65 mA	T <sub>J</sub> = 25 °C		3.9	4.5	
			T <sub>J</sub> = 100 °C		5.8	6.7	
TNY280 I <sub>D</sub> = 75 mA	T <sub>J</sub> = 25 °C		2.6	3.0			
	T <sub>J</sub> = 100 °C		3.9	4.5			
OFF-State Drain Leakage Current	I <sub>DSS1</sub>	V <sub>BP/M</sub> = 6.2 V V <sub>EN/UV</sub> = 0 V V <sub>DS</sub> = 560 V T <sub>J</sub> = 125 °C See Note I	TNY274-276			50	μA
			TNY277-278			100	
			TNY279-280			200	
	I <sub>DSS2</sub>	V <sub>BP/M</sub> = 6.2 V V <sub>EN/UV</sub> = 0 V	V <sub>DS</sub> = 375 V, T <sub>J</sub> = 50 °C See Note G, I		15		
Breakdown Voltage	BV <sub>DSS</sub>	V <sub>BP</sub> = 6.2 V, V <sub>EN/UV</sub> = 0 V, See Note J, T <sub>J</sub> = 25 °C		700			V
DRAIN Supply Voltage				50			V
Auto-Restart ON-Time at f <sub>OSC</sub>	t <sub>AR</sub>	T <sub>J</sub> = 25 °C See Note K			64		ms
Auto-Restart Duty Cycle	DC <sub>AR</sub>	T <sub>J</sub> = 25 °C			3		%

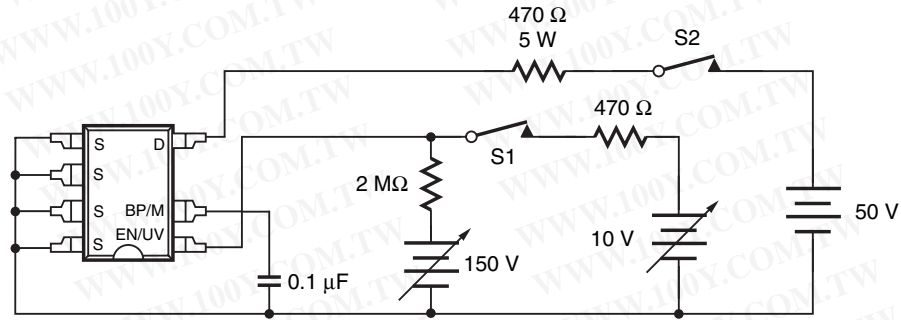
**NOTES:**

- A.  $I_{S1}$  is an accurate estimate of device controller current consumption at no-load, since operating frequency is so low under these conditions. Total device consumption at no-load is the sum of  $I_{S1}$  and  $I_{DSS2}$ .
- B. Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BP/M pin current at 6.1 V.
- C. BP/M pin is not intended for sourcing supply current to external circuitry.
- D. To ensure correct current limit it is recommended that nominal 0.1  $\mu\text{F}$  / 1  $\mu\text{F}$  / 10  $\mu\text{F}$  capacitors are used. In addition, the BP/M capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BP/M Pin Cap Value	Tolerance Relative to Nominal Capacitor Value	
	Min	MAX
0.1 $\mu\text{F}$	-60%	+100%
1 $\mu\text{F}$	-50%	+100%
10 $\mu\text{F}$	-50%	NA

- E. For current limit at other di/dt values, refer to Figure 23.
- F. TNY274 does not set an increased current limit value, but with a 10  $\mu\text{F}$  BP/M pin capacitor the current limit is the same as with a 1  $\mu\text{F}$  BP/M pin capacitor (reduced current limit value).
- G. This parameter is derived from characterization.
- H. This parameter is derived from the change in current limit measured at 1X and 4X of the di/dt shown in the  $I_{LIMIT}$  specification.
- I.  $I_{DSS1}$  is the worst case OFF state leakage specification at 80% of  $BV_{DSS}$  and maximum operating junction temperature.  $I_{DSS2}$  is a typical specification under worst case application conditions (rectified 265 VAC) for no-load consumption calculations.
- J. Breakdown voltage may be checked against minimum  $BV_{DSS}$  specification by ramping the DRAIN pin voltage up to but not exceeding minimum  $BV_{DSS}$ .
- K. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency).

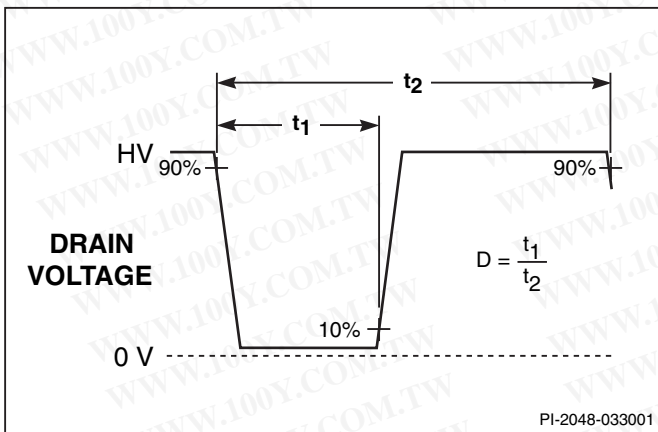




**NOTE:** This test circuit is not applicable for current limit or output characteristic measurements.

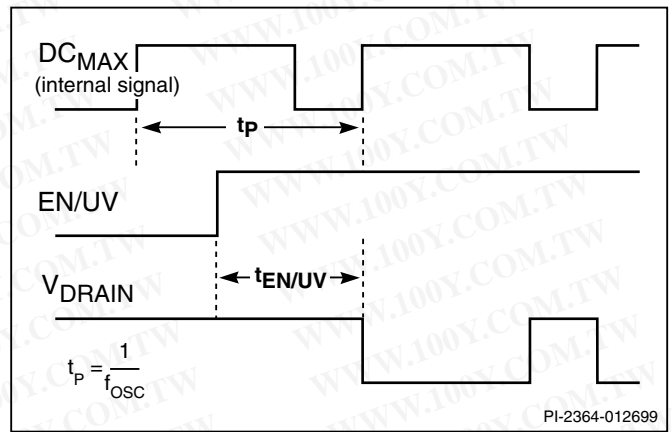
PI-4079-080905

Figure 16. General Test Circuit.



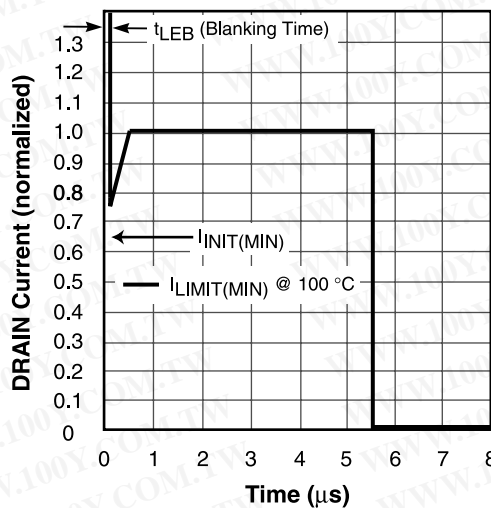
PI-2048-033001

Figure 17. Duty Cycle Measurement.



PI-2364-012699

Figure 18. Output Enable Timing.



PI-4279-013006

Figure 19. Current Limit Envelope.



## Typical Performance Characteristics

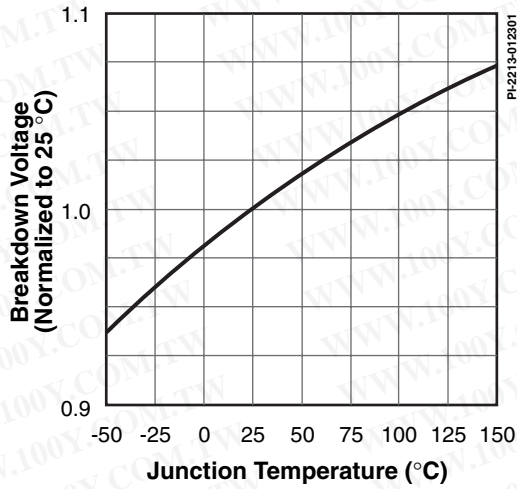


Figure 20. Breakdown vs. Temperature.

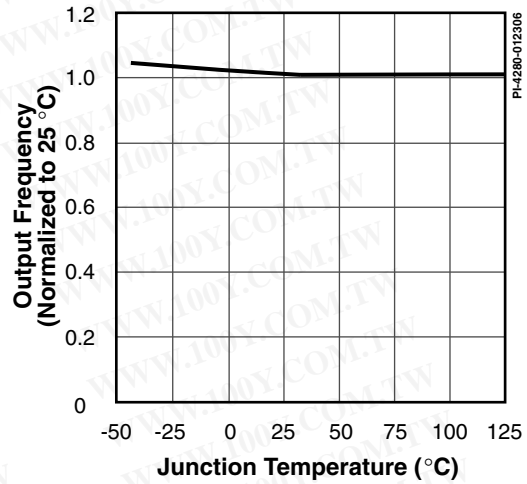


Figure 21. Frequency vs. Temperature.

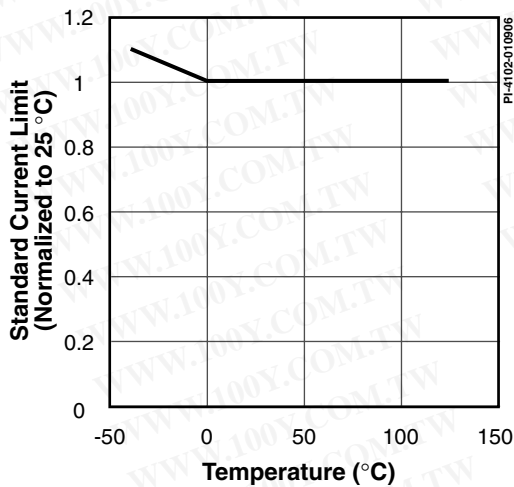


Figure 22. Standard Current Limit vs. Temperature.

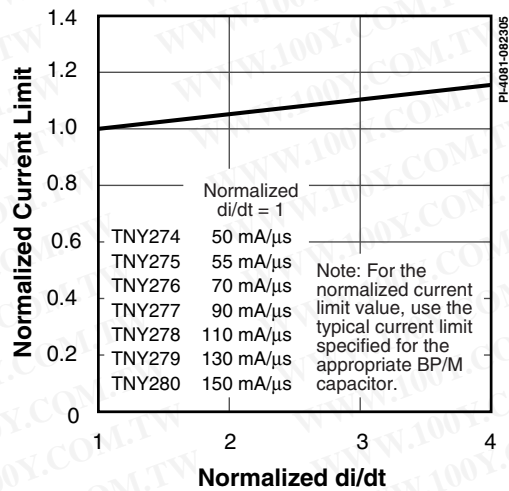


Figure 23. Current Limit vs. di/dt.

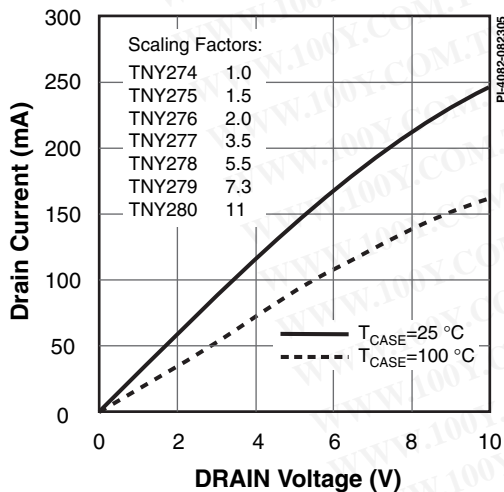


Figure 24. Output Characteristic.

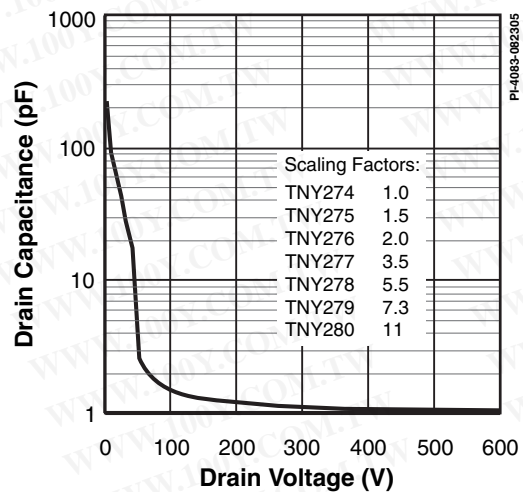


Figure 25.  $C_{oss}$  vs. Drain Voltage.



Typical Performance Characteristics (cont.)

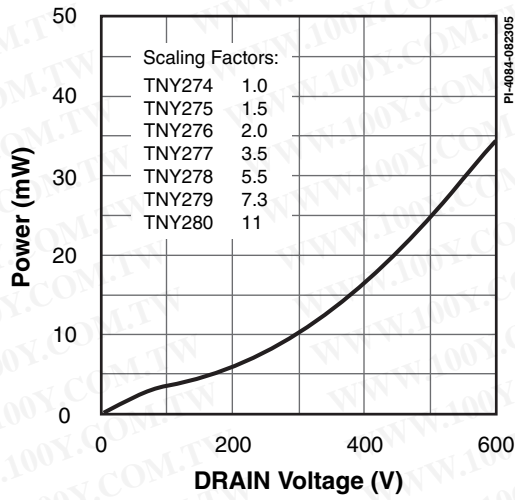


Figure 26. Drain Capacitance Power.

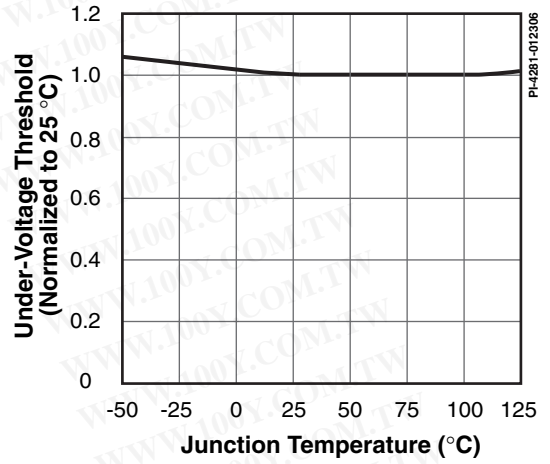
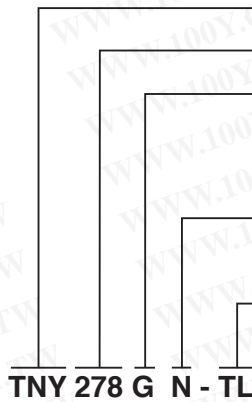


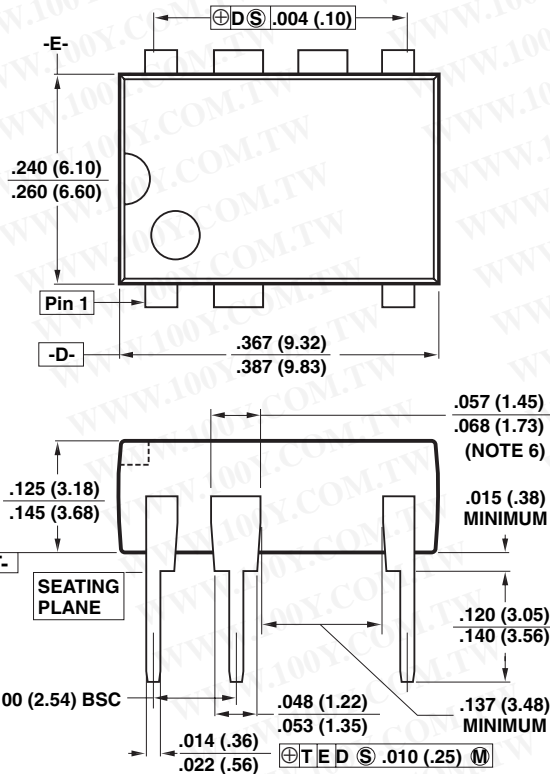
Figure 27. Undervoltage Threshold vs. Temperature.

**PART ORDERING INFORMATION**



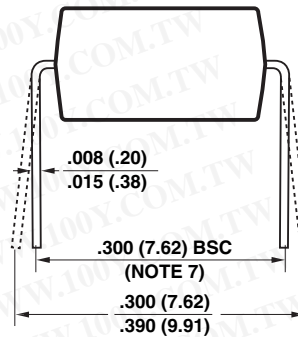
<b>TinySwitch Product Family</b>	
<b>Series Number</b>	
<b>Package Identifier</b>	
G	Plastic Surface Mount SMD-8C
P	Plastic DIP-8C
<b>Lead Finish</b>	
N	Pure Matte Tin (Pb-Free)
<b>Tape &amp; Reel and Other Options</b>	
Blank	Standard Configurations
TL	Tape & Reel, 1000 pcs min./mult., G Package only

**DIP-8C**



**Notes:**

1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.



**P08C**

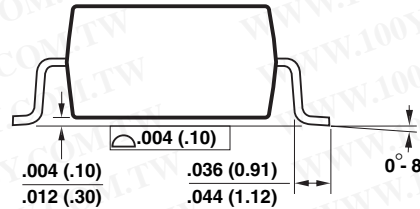
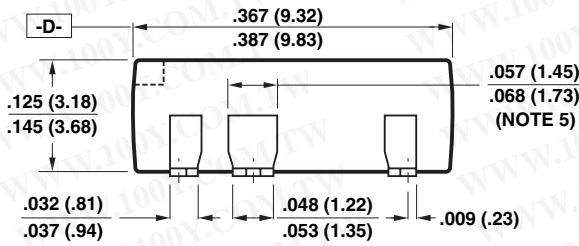
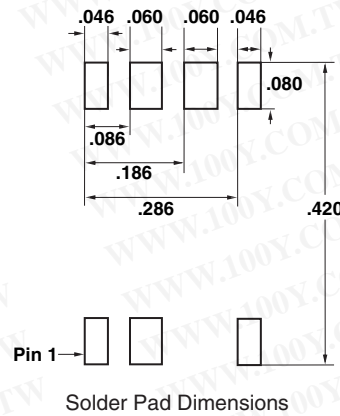
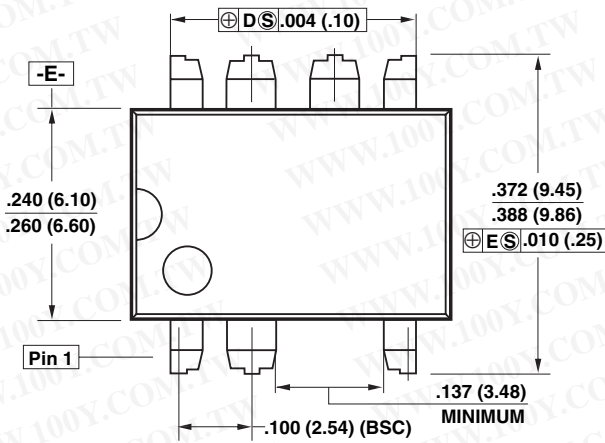
PI-3933-100504



SMD-8C

Notes:

1. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
2. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
3. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 3 is omitted.
4. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
5. Lead width measured at package body.
6. D and E are referenced datums on the package body.



G08C

PI-4015-013106

Revision	Notes	Date
D	Release final data sheet.	1/06
E	Corrected figure numbers and references.	2/06
F	Separated current limit and power coefficient values for G package and updated Figure 15. Added EN/UV and PC board leakage currents in Key Applications Considerations section.	4/06
G	Updated line undervoltage current threshold to 2 $\mu$ A.	6/06

**For the latest updates, visit our website: [www.powerint.com](http://www.powerint.com)**

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

**PATENT INFORMATION**

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at [www.powerint.com](http://www.powerint.com). Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

**LIFE SUPPORT POLICY**

POWER INTEGRATIONS' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF POWER INTEGRATIONS. As used herein:

1. A Life support device or system is one which, (i) is intended for surgical implant into the body, or (ii) supports or sustains life, and (iii) whose failure to perform, when properly used in accordance with instructions for use, can be reasonably expected to result in significant injury or death to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

The PI logo, **TOPSwitch**, **TinySwitch**, **LinkSwitch**, **DPA-Switch**, **PeakSwitch**, **Clamless**, **EcoSmart**, **E-Shield**, **Filterfuse**, **StackFET**, **PI Expert** and **PI FACTS** are trademarks of Power Integrations, Inc. Other trademarks are property of their respective companies. ©Copyright 2006, Power Integrations, Inc.

**Power Integrations Worldwide Sales Support Locations**

**WORLD HEADQUARTERS**

5245 Hellyer Avenue  
San Jose, CA 95138, USA.  
Main: +1-408-414-9200  
Customer Service:  
Phone: +1-408-414-9665  
Fax: +1-408-414-9765  
*e-mail: [usasales@powerint.com](mailto:usasales@powerint.com)*

**GERMANY**

Rueckertstrasse 3  
D-80336, Munich  
Germany  
Phone: +49-89-5527-3910  
Fax: +49-89-5527-3920  
*e-mail: [eurossales@powerint.com](mailto:eurossales@powerint.com)*

**JAPAN**

1st Bldg Shin-Yokohama  
2-12-20 Kohoku-ku,  
Yokohama-shi, Kanagawa  
ken, Japan 222-0033  
Phone: +81-45-471-1021  
Fax: +81-45-471-3717  
*e-mail: [japansales@powerint.com](mailto:japansales@powerint.com)*

**TAIWAN**

5F, No. 318, Nei Hu Rd., Sec. 1  
Nei Hu Dist.  
Taipei, Taiwan 114, R.O.C.  
Phone: +886-2-2659-4570  
Fax: +886-2-2659-4550  
*e-mail: [taiwansales@powerint.com](mailto:taiwansales@powerint.com)*

**CHINA (SHANGHAI)**

Rm 807-808A  
Pacheer Commercial Centre,  
555 Nanjing Rd. West  
Shanghai, P.R.C. 200041  
Phone: +86-21-6215-5548  
Fax: +86-21-6215-2468  
*e-mail: [chinasales@powerint.com](mailto:chinasales@powerint.com)*

**INDIA**

#1, 14th Main Road  
Vasanthanagar  
Bangalore-560052 India  
Phone: +91-80-41138020  
Fax: +91-80-41138023  
*e-mail: [indiasales@powerint.com](mailto:indiasales@powerint.com)*

**KOREA**

RM 602, 6FL  
Korea City Air Terminal B/D, 159-6  
Samsung-Dong, Kangnam-Gu,  
Seoul, 135-728, Korea  
Phone: +82-2-2016-6610  
Fax: +82-2-2016-6630  
*e-mail: [koreasales@powerint.com](mailto:koreasales@powerint.com)*

**UNITED KINGDOM**

1st Floor, St. James's House  
East Street, Farnham  
Surrey GU9 7TJ  
United Kingdom  
Phone: +44 (0) 1252-730-140  
Fax: +44 (0) 1252-727-689  
*e-mail: [eurossales@powerint.com](mailto:eurossales@powerint.com)*

**CHINA (SHENZHEN)**

Rm 2206-2207, Block A,  
Electronics Science & Technology Bldg.  
2070 Shennan Zhong Rd.  
Shenzhen, Guangdong,  
China, 518031  
Phone: +86-755-8379-3243  
Fax: +86-755-8379-5828  
*e-mail: [chinasales@powerint.com](mailto:chinasales@powerint.com)*

**ITALY**

Via De Amicis 2  
20091 Bresso MI – Italy  
Phone: +39-028-928-6000  
Fax: +39-028-928-6009  
*e-mail: [eurossales@powerint.com](mailto:eurossales@powerint.com)*

**SINGAPORE**

51 Newton Road  
#15-08/10 Goldhill Plaza  
Singapore, 308900  
Phone: +65-6358-2160  
Fax: +65-6358-2015  
*e-mail: [singaporesales@powerint.com](mailto:singaporesales@powerint.com)*

**APPLICATIONS HOTLINE**  
World Wide +1-408-414-9660

**APPLICATIONS FAX**  
World Wide +1-408-414-9760



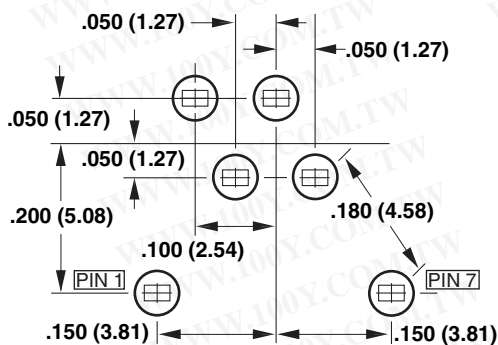
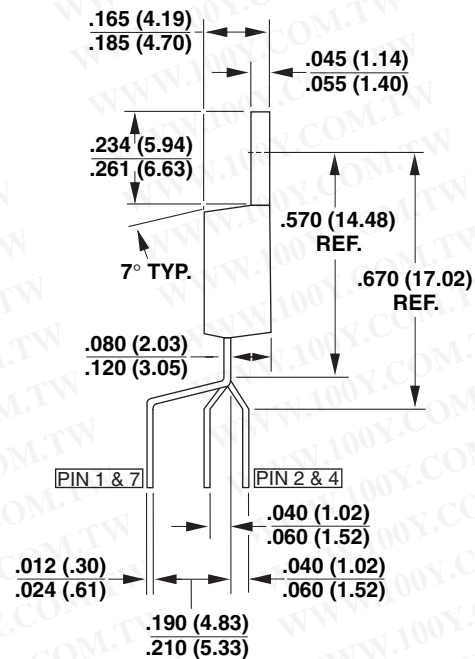
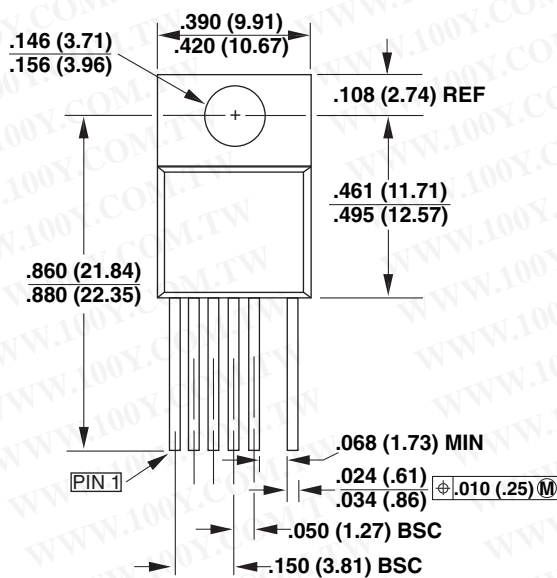
# Package Information

## Package Design Specifications, Tape & Reel and Assembly Information



### Package Design Specifications

#### TO-220-7C



Y07C

MOUNTING HOLE PATTERN

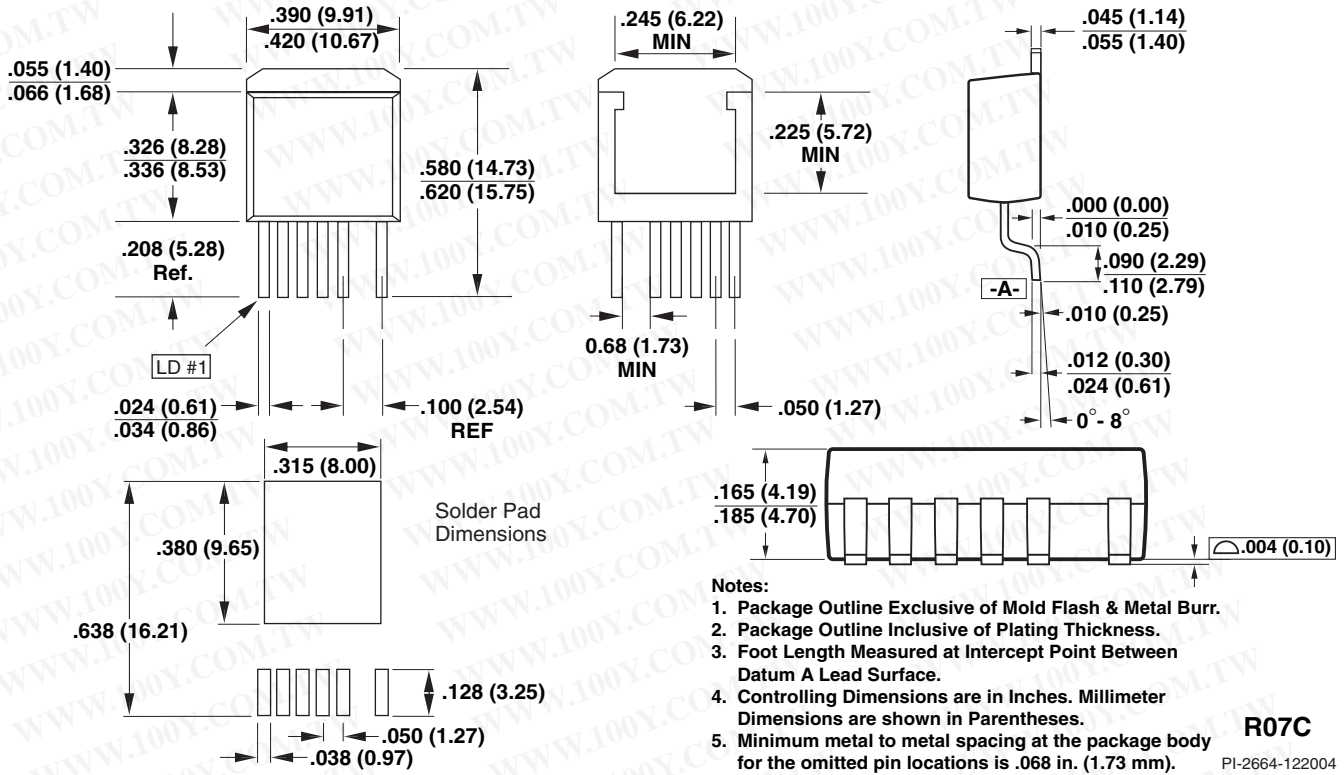
**Notes:**

1. Controlling dimensions are inches. Millimeter dimensions are shown in parentheses.
2. Pin numbers start with Pin 1, and continue from left to right when viewed from the front.
3. Dimensions do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15mm) on any side.
4. Minimum metal to metal spacing at the package body for omitted pin locations is .068 in. (1.73 mm).
5. Position of terminals to be measured at a location .25 (6.35) below the package body.
6. All terminals are solder plated.

PI-2644-122004

**PACKAGE INFORMATION**

**TO-263-7C**

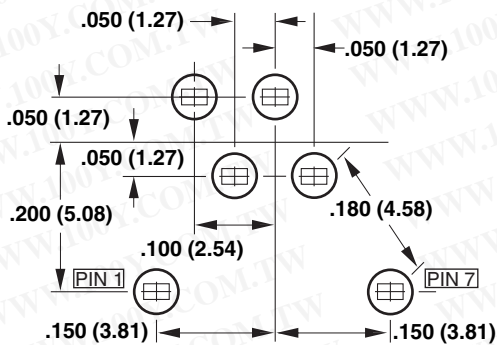
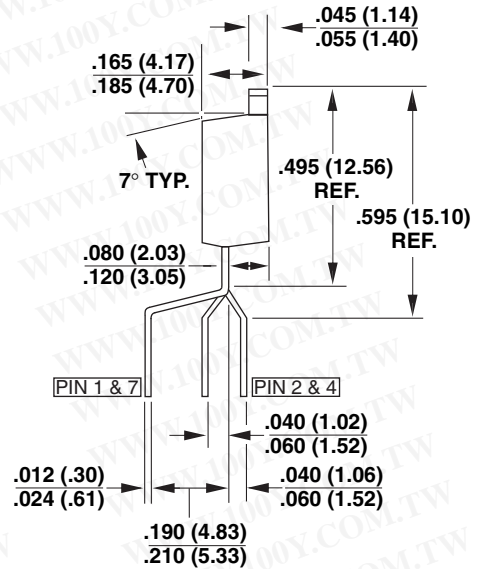
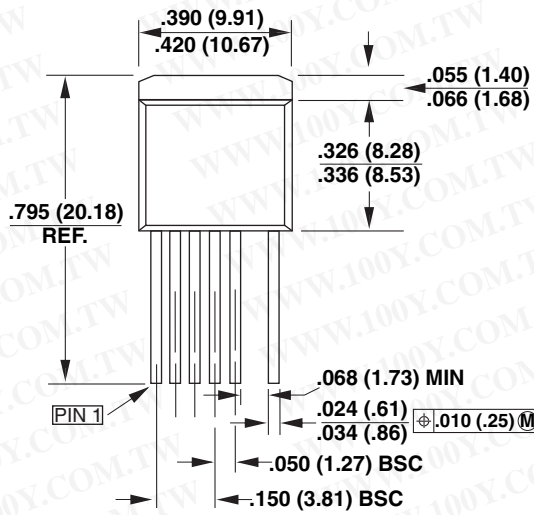


- Notes:**
1. Package Outline Exclusive of Mold Flash & Metal Burr.
  2. Package Outline Inclusive of Plating Thickness.
  3. Foot Length Measured at Intercept Point Between Datum A Lead Surface.
  4. Controlling Dimensions are in Inches. Millimeter Dimensions are shown in Parentheses.
  5. Minimum metal to metal spacing at the package body for the omitted pin locations is .068 in. (1.73 mm).

**R07C**

PI-2664-122004

TO-262-7C



F07C

MOUNTING HOLE PATTERN

Notes:

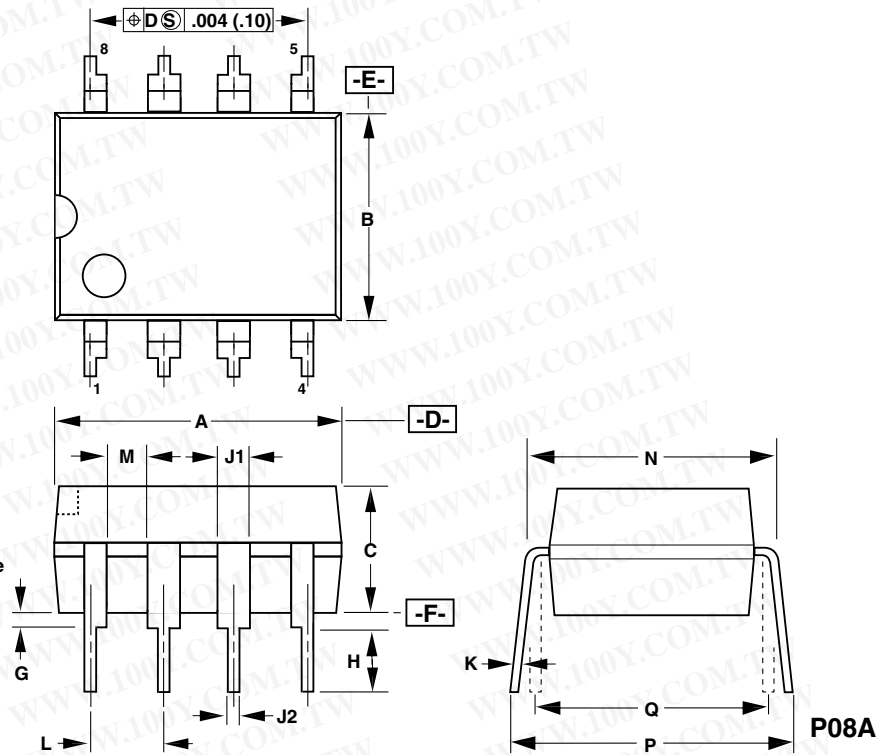
1. Controlling dimensions are inches. Millimeter dimensions are shown in parentheses.
2. Pin numbers start with Pin 1, and continue from left to right when viewed from the front.
3. Dimensions do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15mm) on any side.
4. Minimum metal to metal spacing at the package body for omitted pin locations is .068 inch (1.73 mm).
5. Position of terminals to be measured at a location .25 (6.35) below the package body.
6. All terminals are solder plated.

PI-2757-122004

# PACKAGE INFORMATION

## DIP-8

DIM	inches	mm
A	0.367-0.387	9.32-9.83
B	0.240-0.260	6.10-6.60
C	0.125-0.145	3.18-3.68
G	0.015-0.040	0.38-1.02
H	0.120-0.140	3.05-3.56
J1	0.057-0.068	1.45-1.73
J2	0.014-0.022	0.36-0.56
K	0.008-0.015	0.20-0.38
L	0.100 BSC	2.54 BSC
M	0.030 (MIN)	0.76 (MIN)
N	0.300-0.320	7.62-8.13
P	0.300-0.390	7.62-9.91
Q	0.300 BSC	7.62 BSC

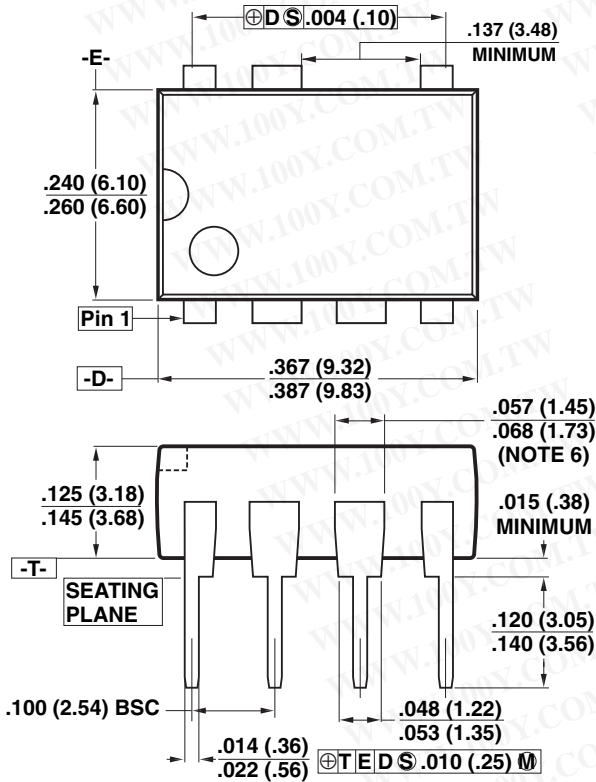


**Notes:**

1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85).
2. Controlling dimensions are inches.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums on the molded body.

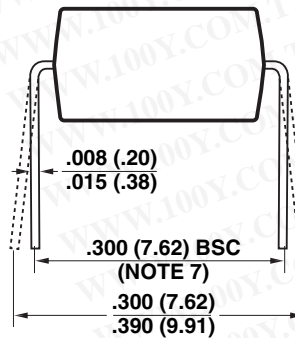
PI-2076-101102

## DIP-8B



**Notes:**

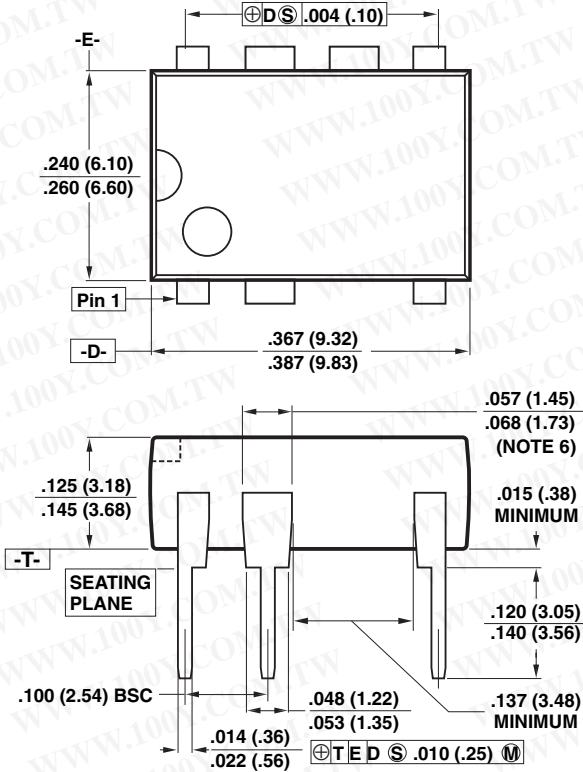
1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 6 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.



P08B

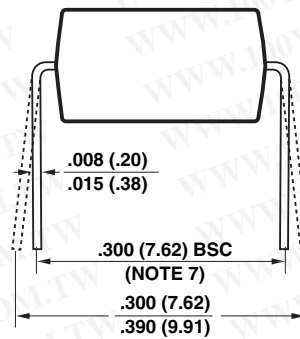
PI-2551-121504

DIP-8C



Notes:

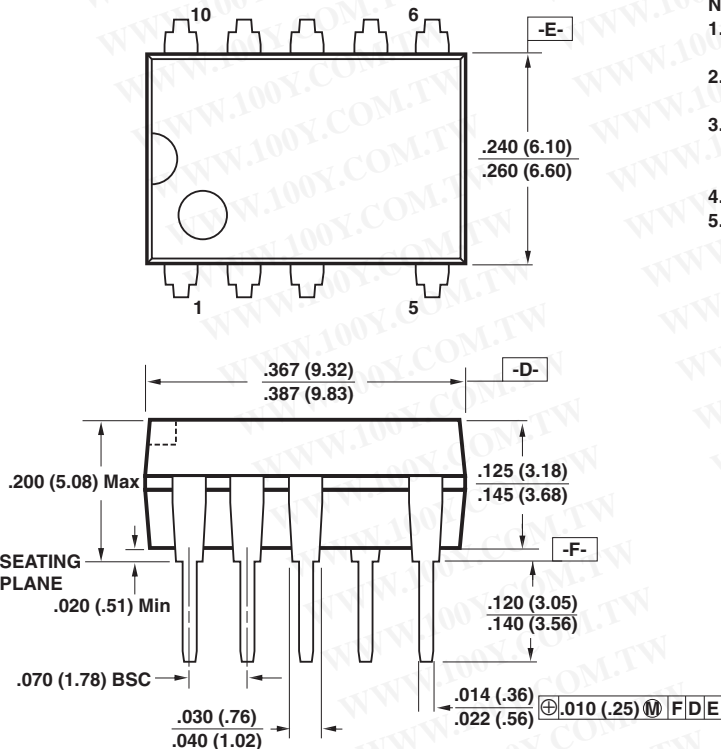
1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.



P08C

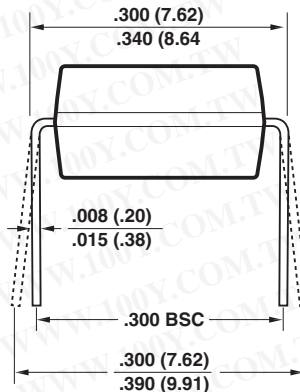
PI-3933-100504

SDIP-10C



Notes:

1. Package dimensions conform to JEDEC specification MS-019.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums.
5. Dimensioning and tolerancing conform to ASME Y14.5M-1994.

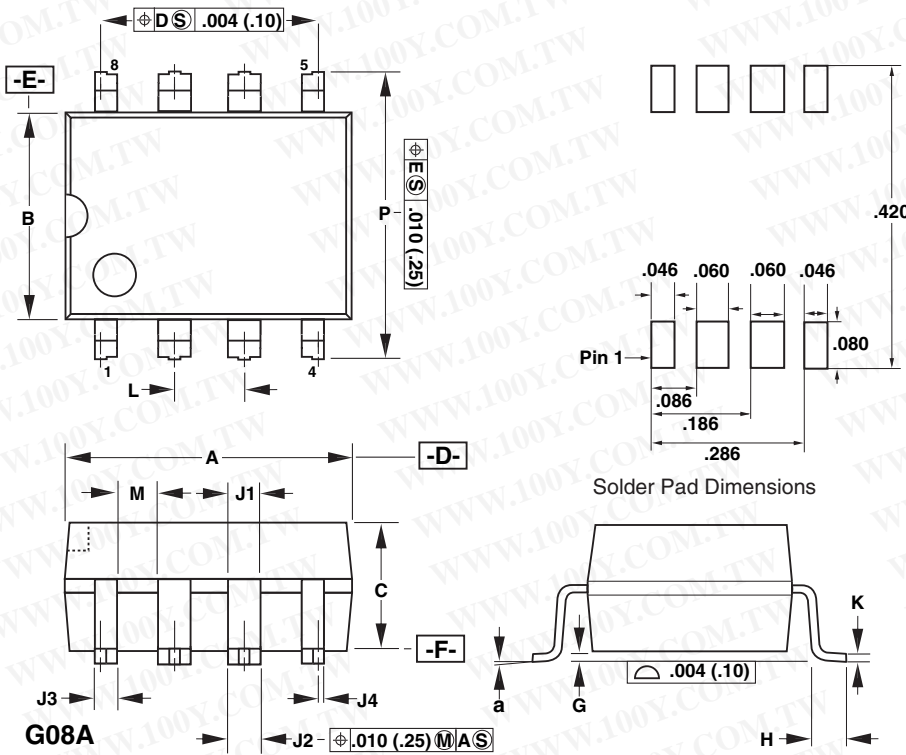


P10C

PI-4648-041107

# PACKAGE INFORMATION

## SMD-8

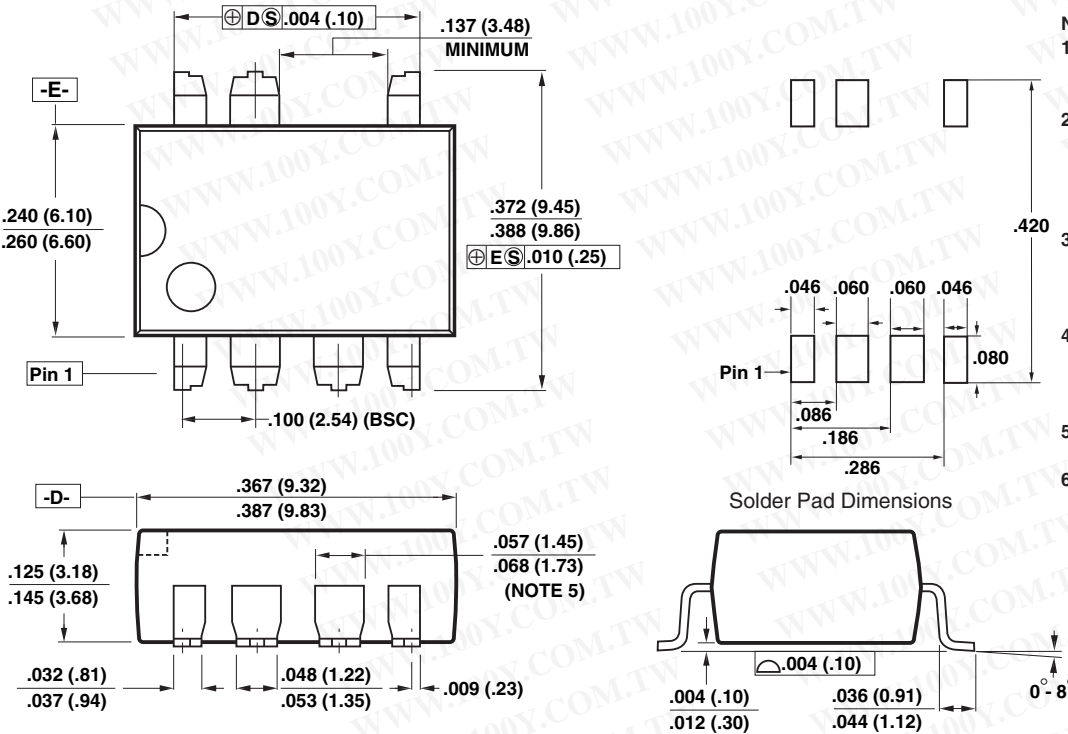


DIM	inches	mm
A	0.367-0.387	9.32-9.83
B	0.240-0.260	6.10-6.60
C	0.125-0.145	3.18-3.68
G	0.004-0.012	0.10-0.30
H	0.036-0.044	0.91-1.12
J1	0.057-0.068	1.45-1.73
J2	0.048-0.053	1.22-1.35
J3	0.032-0.037	0.81-0.94
J4	0.007-0.011	0.18-0.28
K	0.010-0.012	0.25-0.30
L	0.100 BSC	2.54 BSC
M	0.030 (MIN)	0.76 (MIN)
P	0.372-0.388	9.45-9.86
a	0-8°	0-8°

- Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB (issue B, 7/85) except for lead shape and size.
  2. Controlling dimensions are inches.
  3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
  4. D, E and F are reference datums on the molded body.

PI-2077-041003

## SMD-8B

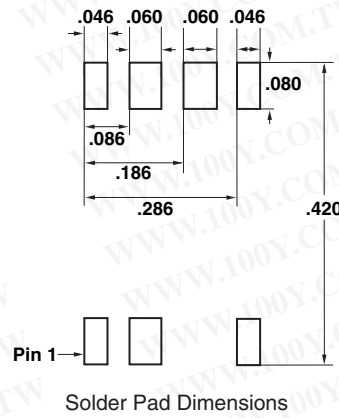
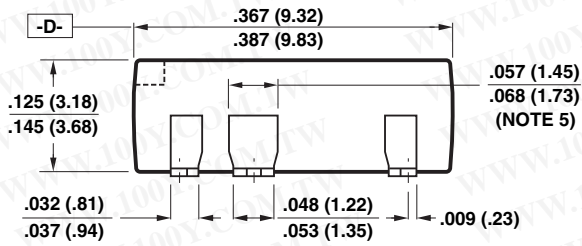
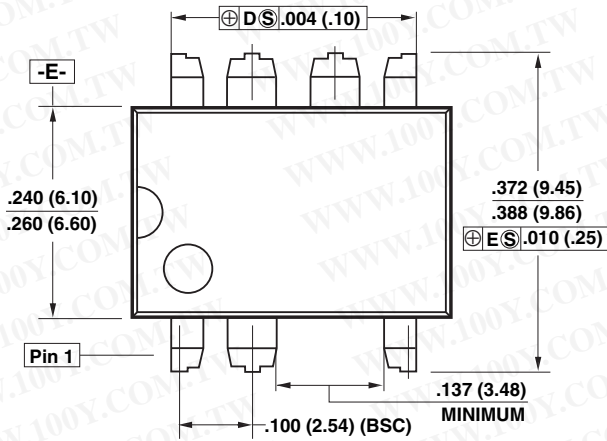


- Notes:
1. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
  2. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
  3. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 6 is omitted.
  4. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
  5. Lead width measured at package body.
  6. D and E are referenced datums on the package body.

G08B

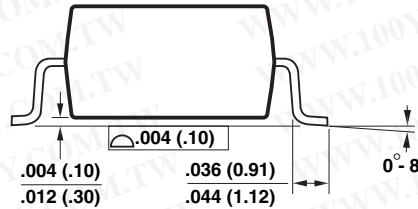
PI-2546-121504

SMD-8C



Notes:

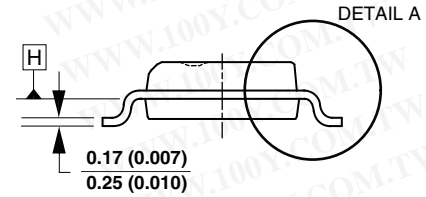
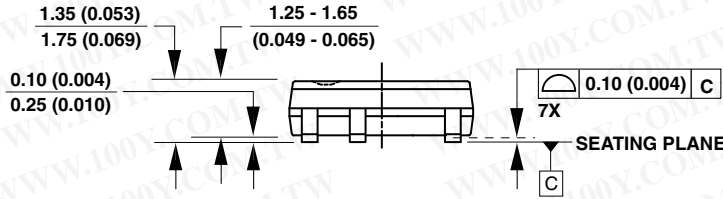
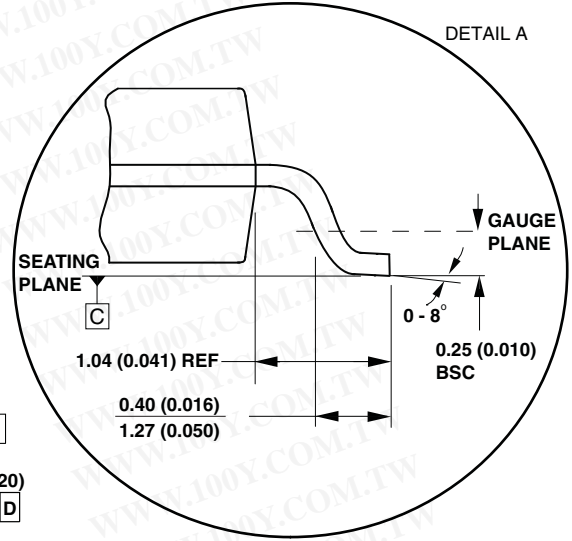
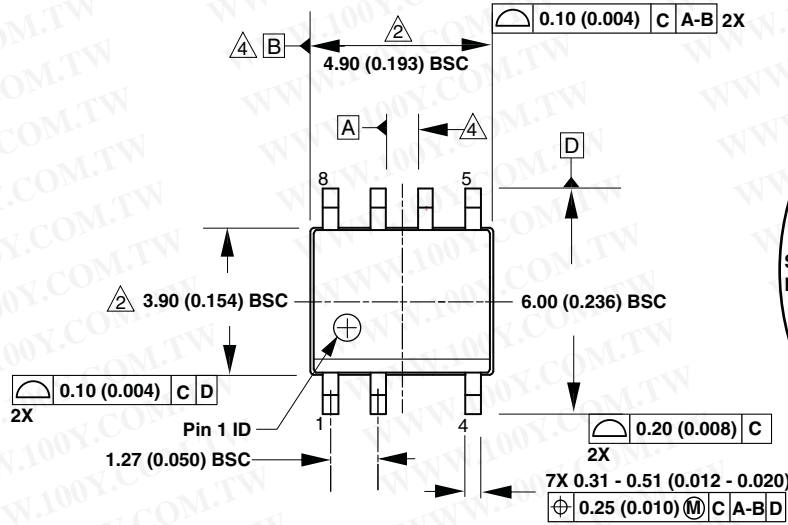
1. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
2. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
3. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 3 is omitted.
4. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
5. Lead width measured at package body.
6. D and E are referenced datums on the package body.



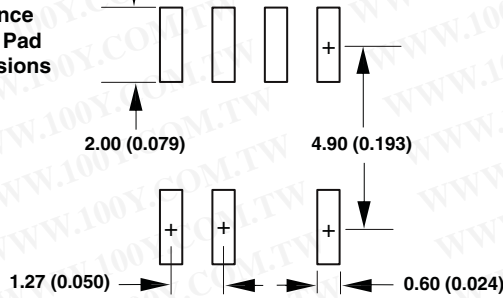
G08C

PI-4015-013106

SO-8C



Reference Solder Pad Dimensions



Notes:

- 1. JEDEC reference: MS-012.
- 2. Package outline exclusive of mold flash and metal burr.
- 3. Package outline inclusive of plating thickness.
- 4. Datums A and B to be determined at datum plane H.
- 5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-040207

## Tape & Reel Ordering Information

Power Integrations makes selected surface-mount parts available in tape and reel form for use with automatic pick-and-place equipment. Tape and reel specifications meet or exceed industry standard specification EIA-481.

### Ordering Information

Parts available in tape and reel form can be ordered by placing a T&R ordering suffix after the base part number. The ordering suffix is TL.

**Base Part #**  
TNY264G

**T&R Suffix**  
-TL

Please contact the factory for other options. Minimum order size is 1 reel per line item, and all orders will be in multiples of full reel quantities. The quantity per reel for each package type is shown in Table 1. Power Integrations normal terms and conditions apply.

### Electrical Specifications

Parts are subjected to the Power Integrations standard test flow, after which the parts are loaded into the tape cavities and sealed with a cover tape using standard anti-static handling procedures. The tape and cover are constructed of conductive modified polystyrene, providing a surface resistivity of  $\leq 10^6 \Omega/\text{square}$ . The reel is made of polystyrene with a topical anti-static coating, providing a surface resistivity of  $\leq 10^{11} \Omega/\text{square}$ .

PACKAGE	TAPE		REEL DIA	REEL QTY
	WIDTH (W)	PITCH (P)		
SMD-8	16 mm	12 mm	330 mm	1000
TO-263	24 mm	16 mm	330 mm	750
SO-8C	12 mm	8 mm	330 mm	2500

Table 1. Primary Tape & Reel Dimensions and Reel Quantities.

### Physical Specifications

Physical specifications of the tape, cover, and reel are governed by EIA-481. Physical dimensions of the tapes are given in Figure 2 and Table 2, and physical dimensions of the reels are given in Figure 3 and Table 3.

### Packaging for Shipment

Power Integrations supplies the following information on the side of each reel for ease of product identification:

- Power Integrations part number (MPN), including orientation suffix
- Encapsulation date code (D/C)
- Assembly lot identification (LOT)
- Quantity (QTY)
- Tape and reel packing date code (R/D)

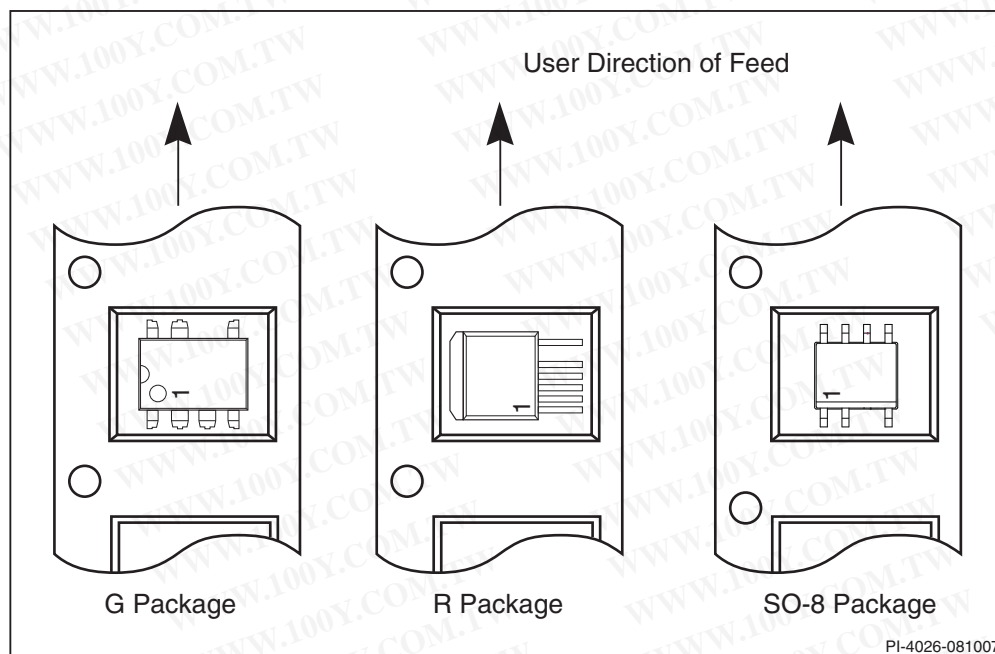


Figure 1. Part Orientation.

# PACKAGE INFORMATION

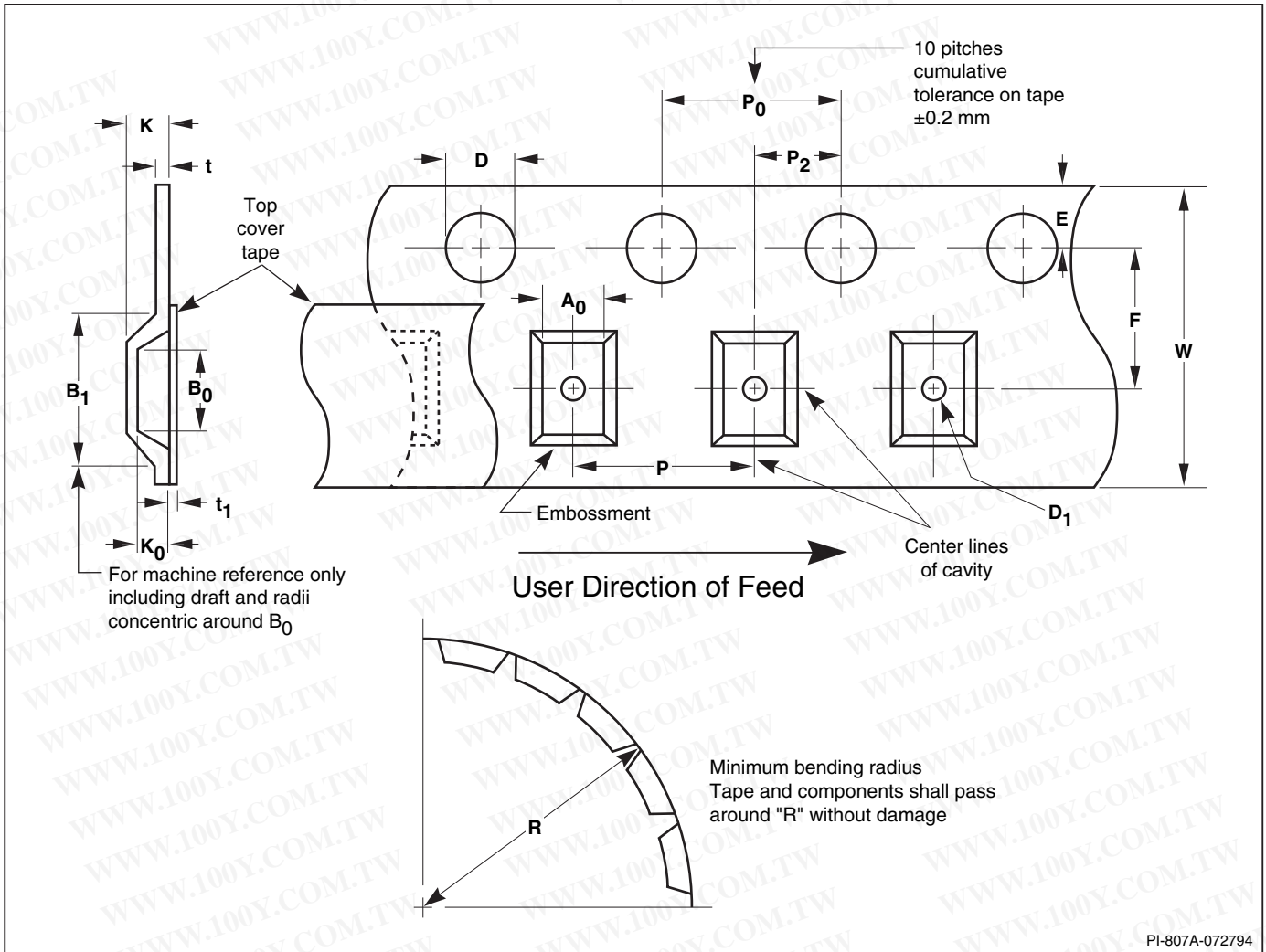
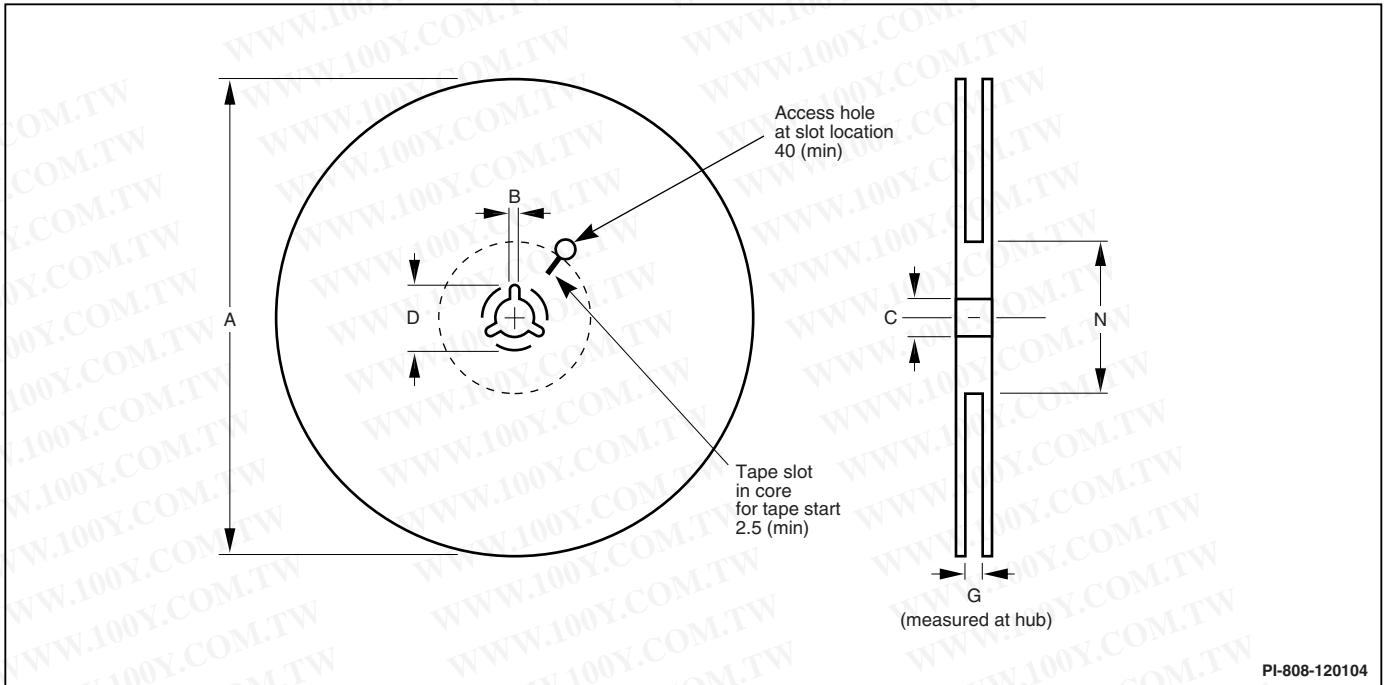


Figure 2. Tape Dimension Index.

Package Type	Tape Size	A <sub>0</sub>	B <sub>0</sub>	B <sub>1</sub>	D	D <sub>1</sub>	E	F	K
SMD-8	16 mm	10.1-10.3	10.0-10.2	12.1 (max)	1.5-1.6	1.5 (min)	1.65-1.85	7.40-7.60	6.5 (max)
TO-263	24 mm	10.9-11.1	16.2-16.4	16.9 (max)	1.5-1.6	1.5 (min)	1.65-1.85	11.40-11.60	5.9 (max)
SO-8C	12 mm	6.5-6.7	5.2-5.4	5.8 (max)	1.5-1.6	1.5 (min)	1.65-1.85	5.45-5.55	2.2 (max)

Package Type	Tape Size	K <sub>0</sub>	P	P <sub>0</sub>	P <sub>2</sub>	R	t	t <sub>1</sub>	W
SMD-8	16 mm	3.60-3.80	11.9-12.1	3.9-4.1	1.90-2.10	40 (min)	0.400 (max)	0.10 (max)	23.7-24.3
TO-263	24 mm	5.40-5.60	15.9-16.1	3.9-4.1	1.90-2.10	50 (min)	0.350 (max)	0.07 (max)	23.7-24.3
SO-8C	12 mm	1.60-1.80	7.90-8.10	3.8-4.2	1.95-2.05	50 (min)	0.35 (max)	0.05 (typ)	11.7-12.3

Table 2. Tape Dimensions (in mm).



PI-808-120104

Figure 3. Reel Dimension Index.

Package Type	Tape Size	A	B	C	D	G	N
SMD-8	16 mm	330 (max)	1.5 (min)	12.80-13.50	20.2 (min)	16	102 (ref)
TO-263	24 mm	330 (max)	1.5 (min)	12.80-13.50	20.2 (min)	24	102 (ref)
SO-8C	12 mm	330 (max)	1.5 (min)	12.80-13.50	20.2 (min)	12	102 (ref)

Table 3. Reel Dimensions (in mm).

## Pb-Free and RoHS Compliant Products

Power Integrations is committed to environmental, health and safety excellence and is actively complying with regulatory requirements regarding the removal of hazardous materials in manufacturing standards and processes. In response to concerns regarding the environmental impact of lead (Pb), a Pb-free solder finish is now available using 100% matte tin (Sn).

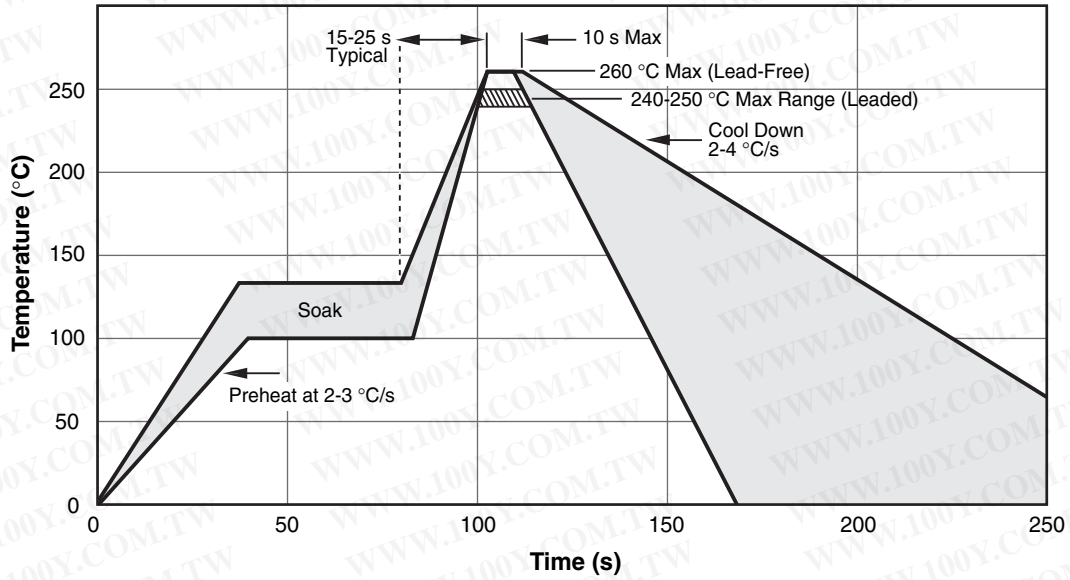
Pb-free packages offered by Power Integrations meet the requirements of the European law on the Restriction of Hazardous Substances (RoHS), which mandates the removal of lead and other hazardous substances cited in the directive.

All Pb-free and RoHS compliant products have passed qualification testing for moisture sensitivity, solderability, and whisker growth. Pb-free and RoHS compliant surface mount products also comply with the joint IPC/JEDEC industry standard on reflow solderability (J-STD-020C). More information on soldering is included below.

RoHS compliant and Pb-free products are designated by an N-suffix at the end of the part number (see the Part Ordering Information section of the product family data sheets).

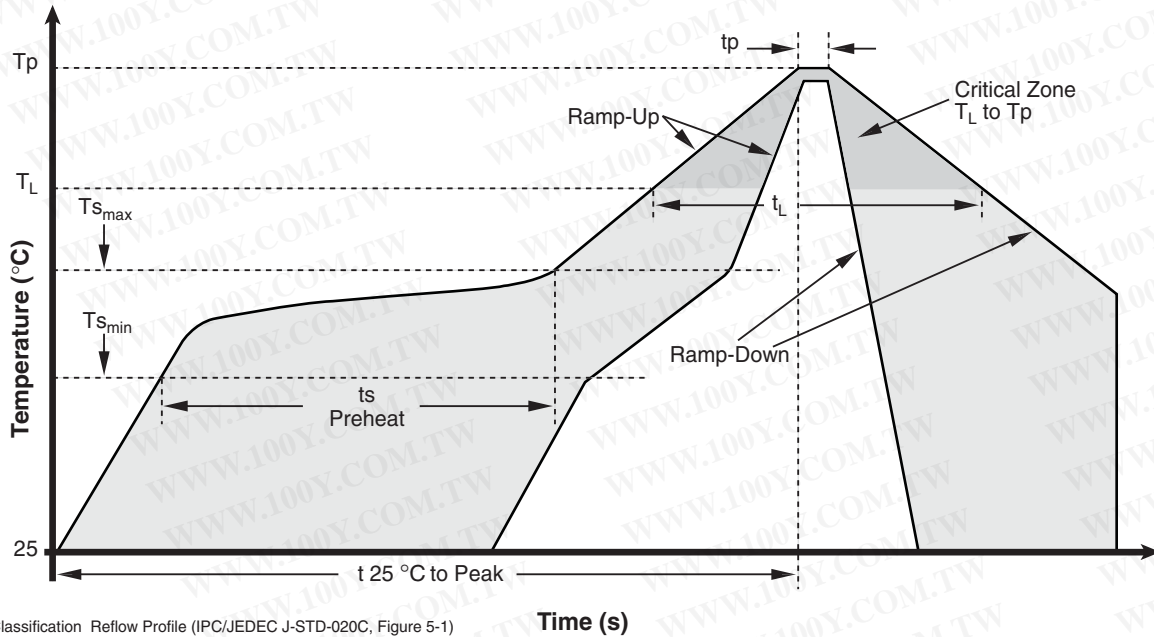
**Solder Temperature Profiles**

**TYPICAL WAVE SOLDER PROFILE FOR Sn-Pb AND Pb-FREE THROUGH-HOLE PACKAGES**



PI-3852-042706

**TYPICAL IR REFLOW PROFILE FOR LEAD-TIN AND Pb-FREE SURFACE MOUNT PACKAGES**



Classification Reflow Profile (IPC/JEDEC J-STD-020C, Figure 5-1)  
 Reproduced with permission by IPC and JEDEC, 2005

PI-3955-030107

Note 1: Pb-free packages are qualified for Sn-Pb assembly. Sn-Pb packages are not qualified for Pb-free assembly.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate ( $T_{s_{max}}$ to $T_p$ )	3 °C/second max.	3 °C/second max.
Preheat ± Temperature Min ( $T_{s_{min}}$ ) ± Temperature Max ( $T_{s_{max}}$ ) ± Time ( $t_{s_{min}}$ to $t_{s_{max}}$ )	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-180 seconds
Time maintained above: ± Temperature ( $T_L$ ) ± Time ( $t_L$ )	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak/Classification Temperature ( $T_p$ )	See Table 5	See Table 5
Time within 5 °C of actual Peak Temperature ( $t_p$ )	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table 4. Classification Reflow Profiles (per IPC/JEDEC J-STD-020C, Table 5.2)

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Package Type	MSL	Sn-Pb Eutectic Assembly	Pb-Free Assembly
SMD-8	4	225 +0/-5 °C	250 + 0 °C*
TO-263	4	225 +0/-5 °C	Not Available
*Tolerance: Process compatibility is up to and including the stated classification temperature (this means Peak reflow temperature + 0 °C. For example, 250 + 0 °C) at the rated MSL level.			

Table 5. Peak/Classification Temperature ( $T_p$ ) for PI Surface Mount Packages.

Note 1: Classification temperatures are in accordance with guidelines set forth in IPC/JEDEC J-STD-020C.

**Soldering Guidelines:**

1. Profiles shown are typical and will therefore vary with different soldering systems.
2. Density and types of components on the board, size and type of board, solder and flux being used, substrate material being used, equipment type/model and age are factors that can influence the profile.
3. Since the melting temperature of solder is higher than the rated temperature of the device, care should be taken that the device will get as little exposure as possible at the high temperature. Not doing so increases possibility of a device failure.

4. Limit high temperature exposure only to single side or one time and mostly to the leads area only.
5. Upon completion of soldering, gradual natural cooling should be observed for a minimum of three minutes. Using forced cooling will increase temperature gradient which increases mechanical stress leading to latent failure.

**PC Board Cleaning**

Power Integrations does not recommend the use of "no-clean" flux.

## Mounting Guidelines for TO-220 Package

### Maximum Torque:

The screw torque specification for the TO-220 packages used for Power Integrations products is 4 lbf · in or 0.45 N · m (4.6 kgf · cm) maximum.

### Mounting Guidelines:

The recommended fastener is a 6-32 screw using a rectangular washer to prevent damage to the tab. If a rectangular washer is not used, a round flat washer is required. The head of a machine screw is not flat enough to prevent damage. Without a washer, damage to the plastic case and semiconductor chip within may occur.

A smaller screw or larger heat sink hole can cause the tab to be deformed, cracking the package. Care must also be taken to prevent contact between the plastic package and the screw head or tool used to tighten it. Self-tapping screws may deform the heat sink causing poor thermal contact.

Rivets should not be used under any circumstances for TO-220 packages.

The mounting surface must be flat and without burrs. Otherwise, the TO-220 tab may be bent, causing damage to the IC chip.

Finally, the IC should be mounted to the heat sink before soldering the assembly to the PCB. Soldering the IC and heat sink to the PCB and then screwing them together will put unacceptable mechanical stress on the IC package.

勝特力材料 886-3-5753170  
勝特力电子(上海) 86-21-54151736  
勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)