

PH2925U

N-channel TrenchMOS™ ultra low level FET

Rev. 02 — 08 April 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low thermal resistance
- Low threshold voltage
- SO8 equivalent area footprint
- Low on-state resistance.

1.3 Applications

- DC-to-DC converters
- Portable appliances
- Switched-mode power supplies
- Notebook computers.

1.4 Quick reference data

- $V_{DS} \leq 25 \text{ V}$
- $I_D \leq 100 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$
- $R_{DSon} \leq 2.9 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT669 (LFAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBL286</p>	<p>MBB076</p>
4	gate (g)		
mb	mounting base; connected to drain (d)		

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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PH2925U	LFAK	Plastic single-ended surface mounted package; 4 leads	SOT669

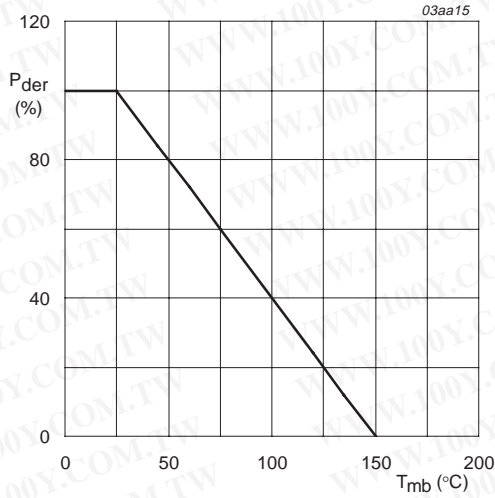
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

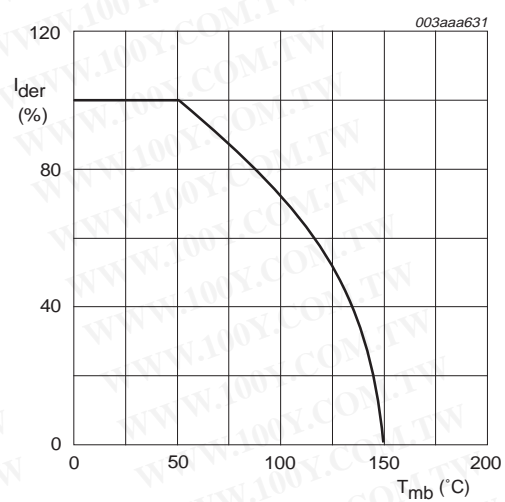
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	25	V
V_{GS}	gate-source voltage (DC)		-	± 10	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 4.5\text{ V};$ Figure 2 and 3	-	100	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 4.5\text{ V};$ Figure 2	-	71	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	150	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 70.7\text{ A};$ $t_p = 0.22\text{ ms}; V_{DD} \leq 25\text{ V}; V_{GS} = 10\text{ V};$ starting $T_j = 25\text{ °C}$	-	250	mJ

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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

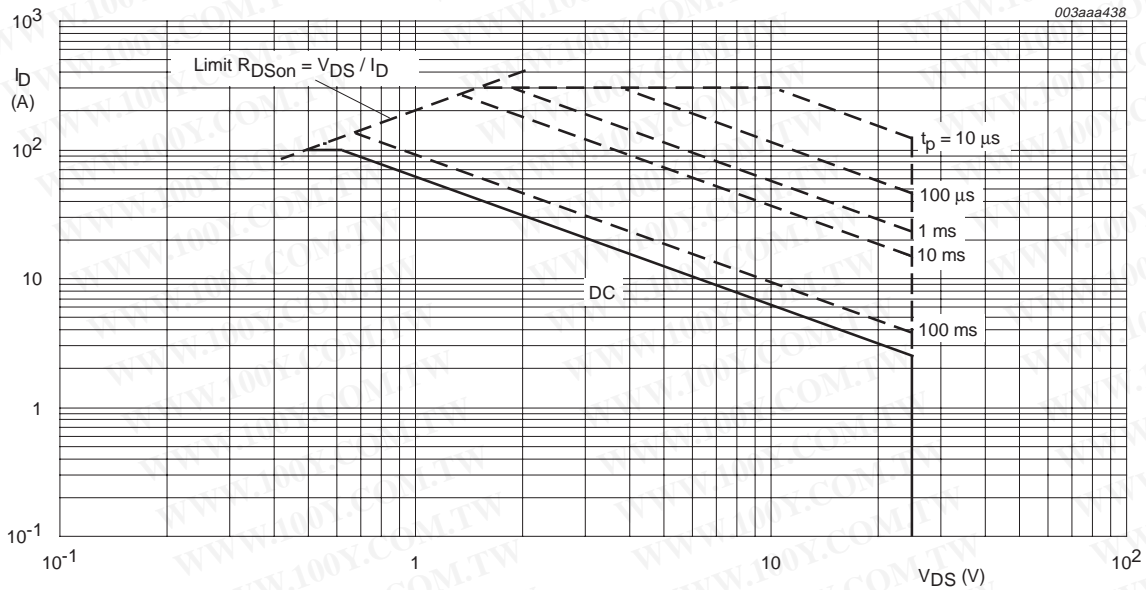
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

$V_{GS} \geq 4.5\text{ V}$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 4.5\text{ V}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

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5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

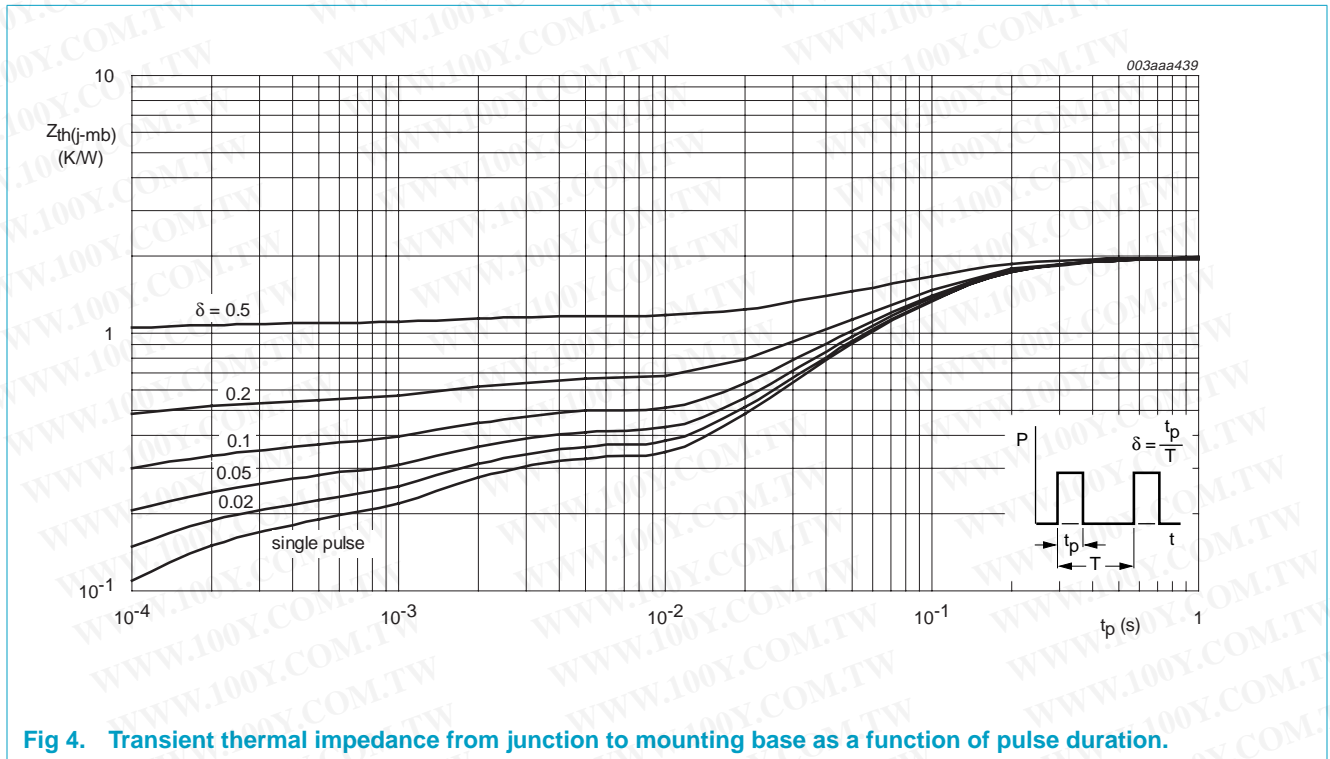


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

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6. Characteristics

Table 5: Characteristics
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ }^\circ\text{C}$	0.45	0.7	-	V
		$T_j = 150\text{ }^\circ\text{C}$	0.25	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 25\ \text{V}$; $V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ }^\circ\text{C}$	-	0.06	1	μA
		$T_j = 150\text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	20	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$; $I_D = 25\ \text{A}$; Figure 7 and 8				
		$T_j = 25\text{ }^\circ\text{C}$	-	2.3	2.9	m Ω
		$T_j = 150\text{ }^\circ\text{C}$	-	3.9	4.9	m Ω
		$V_{GS} = 2.5\ \text{V}$; $I_D = 25\ \text{A}$	-	3.2	3.7	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 50\ \text{A}$; $V_{DD} = 10\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; Figure 13	-	92	-	nC
Q_{gs}	gate-source charge		-	12	-	nC
Q_{gd}	gate-drain (Miller) charge		-	20.2	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 10\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	6150	-	pF
C_{oss}	output capacitance		-	1170	-	pF
C_{rss}	reverse transfer capacitance		-	814	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\ \text{V}$; $I_D = 25\ \text{A}$; $V_{GS} = 4.5\ \text{V}$; $R_G = 4.7\ \Omega$	-	30	-	ns
t_r	rise time		-	80	-	ns
$t_{d(off)}$	turn-off delay time		-	258	-	ns
t_f	fall time		-	114	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.72	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\ \text{A}$; $dI_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{DS} = 25\ \text{V}$; $V_{GS} = 0\ \text{V}$	-	60	-	ns

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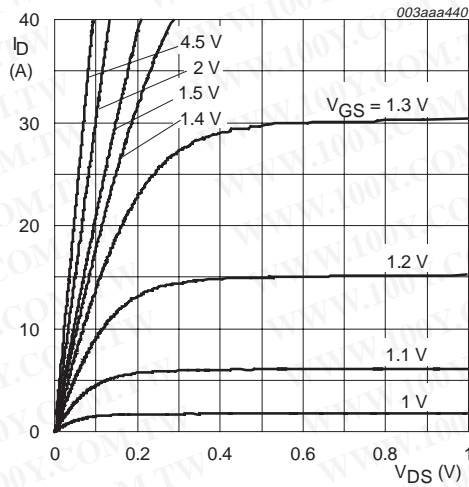


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.

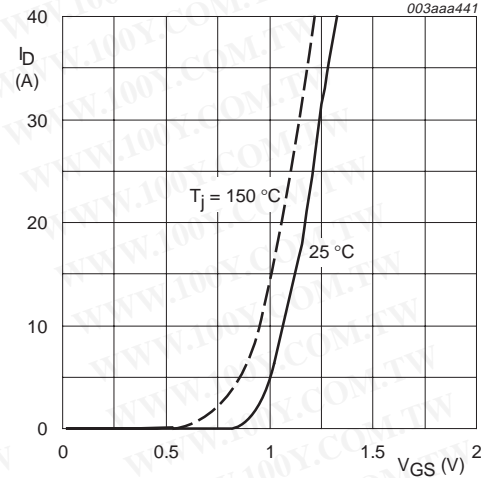


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.

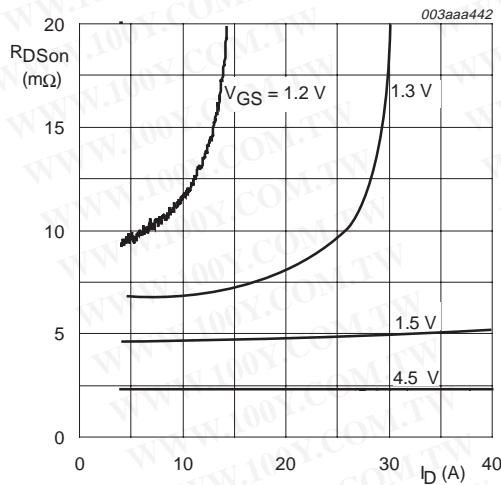


Fig 7. Drain-source on-state resistance as a function of drain current; typical values.

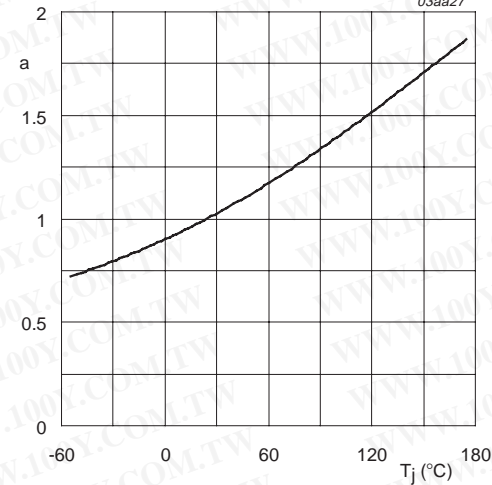
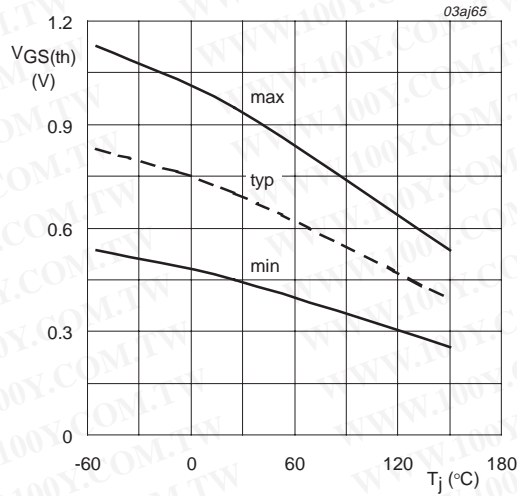


Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.

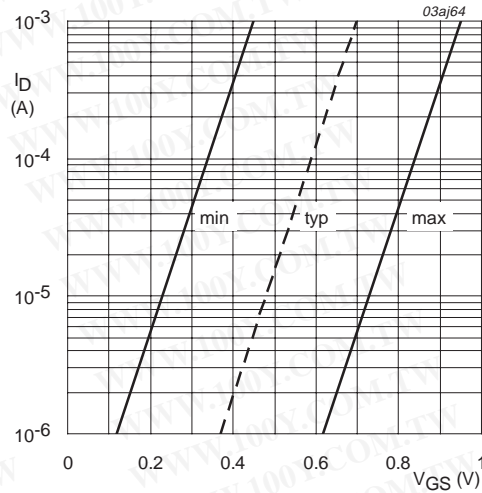
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

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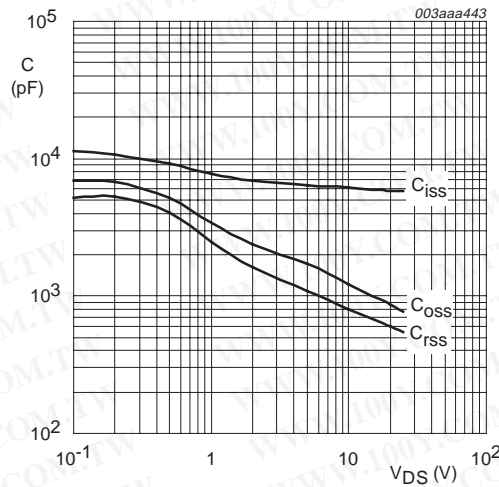
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

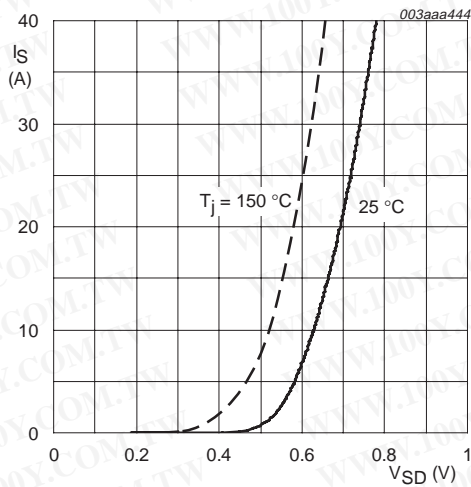
Fig 10. Sub-threshold drain current as a function of gate-source voltage.



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

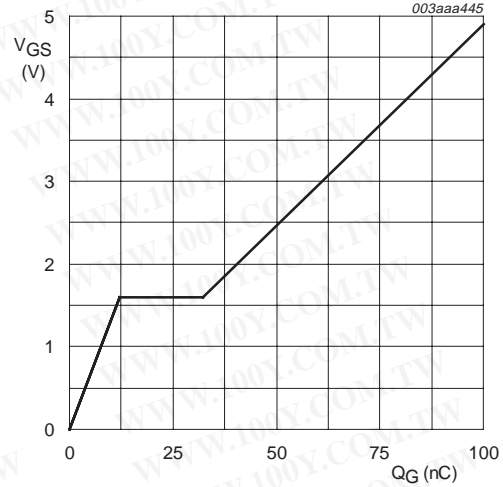
Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

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$T_j = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0\text{V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 50\text{A}$; $V_{DD} = 10\text{V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

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7. Package outline

Plastic single-ended surface mounted package (Philips version LFFPAK); 4 leads

SOT669

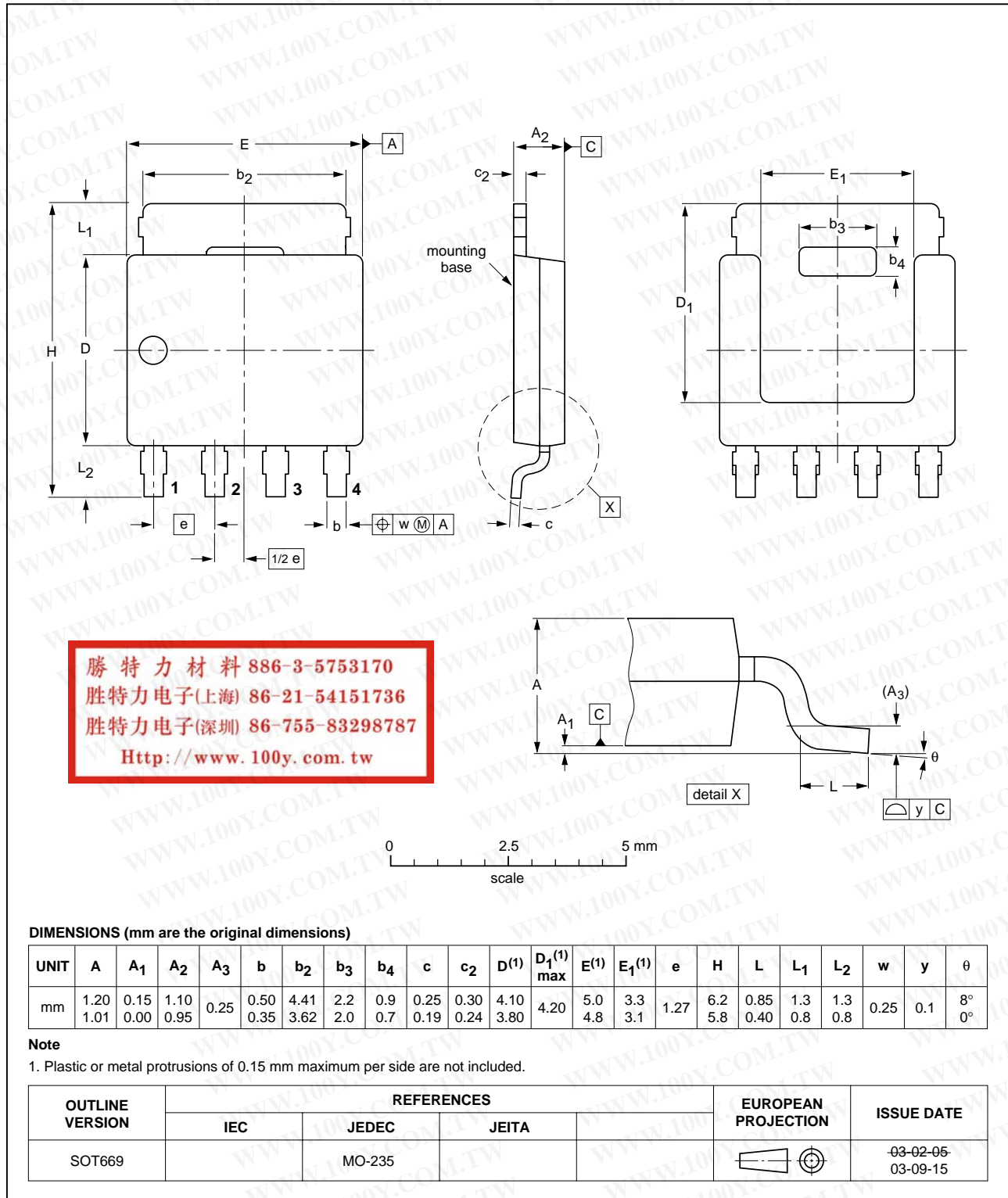


Fig 14. SOT669 (LFFPAK).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20040408	-	Product data (9397 750 13064). Modifications: <ul style="list-style-type: none"> • Section 3 “Ordering information” added • Correction to $E_{DS(AL)S}$ conditions Section 4 “Limiting values” • I_D data corrected in Section 1.4 “Quick reference data” • I_D and I_{DM} data corrected in Table 3 “Limiting values” • Correction to Figure 2 and Figure 3 • Correction to typical V_{SD} Section 6 “Characteristics” • t_r data corrected in Section 6 “Characteristics”
01	20030502	-	Product data (9397 750 11407).

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9. Data sheet status

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I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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