

2N7002E

N-channel TrenchMOS™ FET

Rev. 02 — 26 April 2005

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold compatible
- Surface-mounted package
- Very fast switching
- TrenchMOS™ technology

1.3 Applications

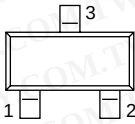
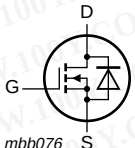
- Logic level translator
- High speed line driver

1.4 Quick reference data

- $V_{DS} \leq 60 \text{ V}$
- $I_D \leq 385 \text{ mA}$
- $R_{DS(on)} \leq 3 \Omega$
- $P_{tot} = 0.83 \text{ W}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	source (S)		
3	drain (D)		

SOT23

mbb076

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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
2N7002E	TO-236AB	plastic surface mounted package; 3 leads	SOT23

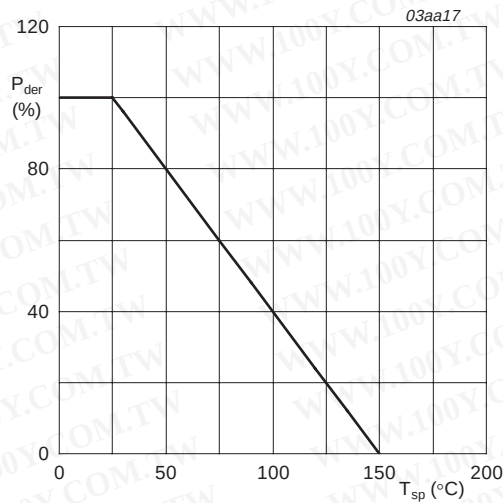
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

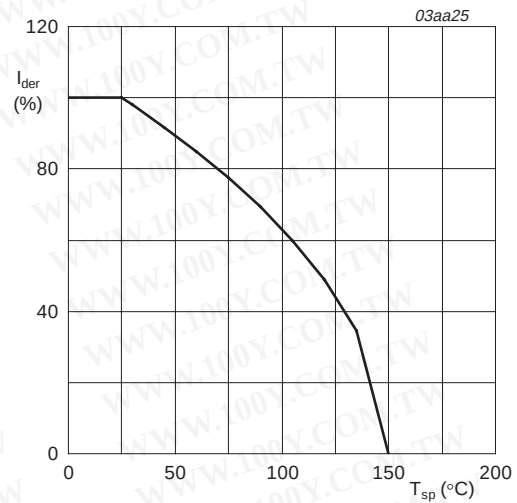
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage (DC)		-	± 30	V
V_{GSM}	peak gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$; pulsed; duty cycle = 25 %	-	± 40	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	385	mA
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	245	mA
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	1.5	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	0.83	W
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	385	mA
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	1.5	A

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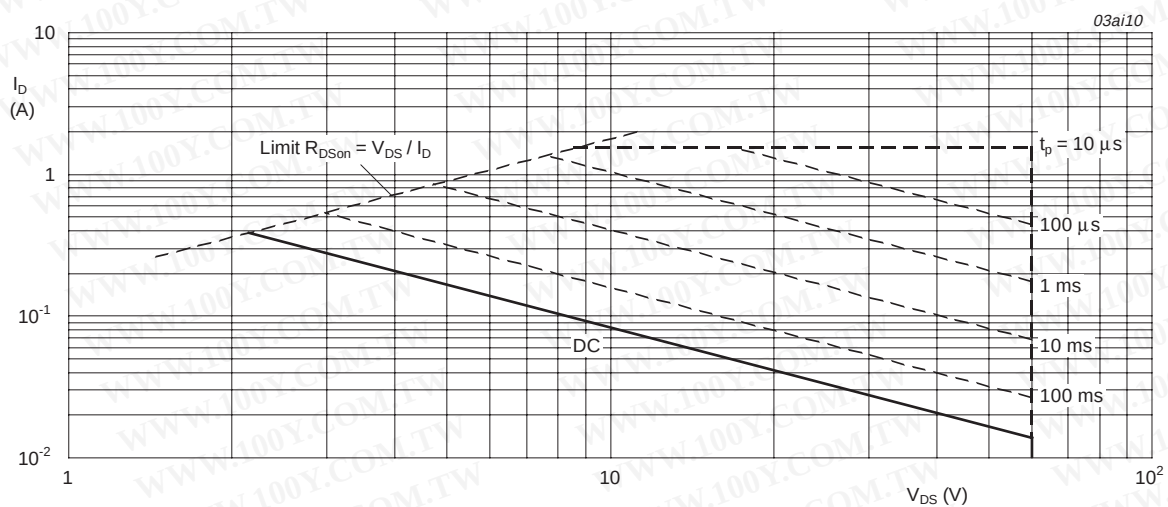
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



$T_{sp} = 25^\circ\text{C}$; I_{DM} is single pulse

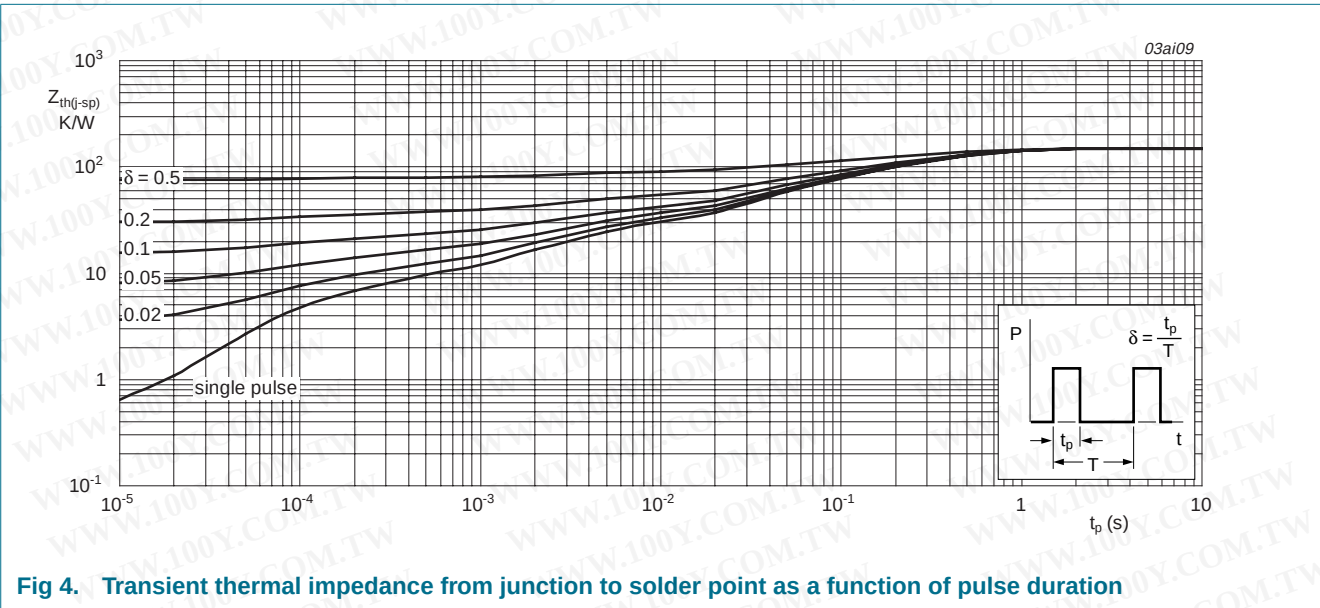
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	150	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	-	350	K/W



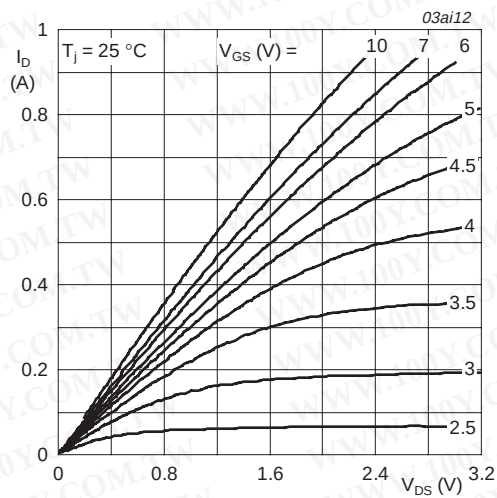
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6. Characteristics

Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

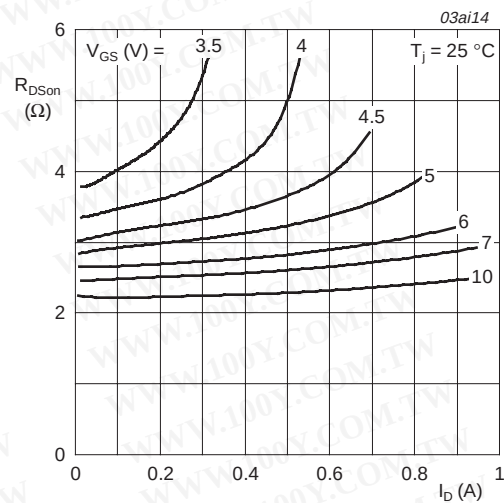
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	60	-	-	V
		$T_j = -55\text{ °C}$	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 and 10				
		$T_j = 25\text{ °C}$	1	2	3	V
		$T_j = 150\text{ °C}$	0.6	-	-	V
		$T_j = -55\text{ °C}$	-	-	3.5	V
I_{DSS}	drain-source leakage current	$V_{DS} = 48\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.01	1	μA
		$T_j = 150\text{ °C}$	-	-	10	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 500\text{ mA}$; Figure 6 and 8				
		$T_j = 25\text{ °C}$	-	2.3	3	Ω
		$T_j = 150\text{ °C}$	-	4.2	5.55	Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 75\text{ mA}$; Figure 6 and 8	-	3.1	4	Ω
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 200\text{ mA}$	100	300	-	mS
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 10\text{ V}$; $f = 1\text{ MHz}$;	-	25	40	pF
C_{oss}	output capacitance	Figure 11	-	18	30	pF
C_{rss}	reverse transfer capacitance		-	7.5	10	pF
t_{on}	turn-on delay time	$V_{DD} = 50\text{ V}$; $R_L = 250\text{ }\Omega$; $V_{GS} = 10\text{ V}$;	-	3	10	ns
t_{off}	turn-off delay time	$R_G = 50\text{ }\Omega$; $R_{GS} = 50\text{ }\Omega$	-	12	15	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 300\text{ mA}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.85	1.5	V
t_{rr}	reverse recovery time	$I_S = 300\text{ mA}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$;	-	30	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}$	-	30	-	nC

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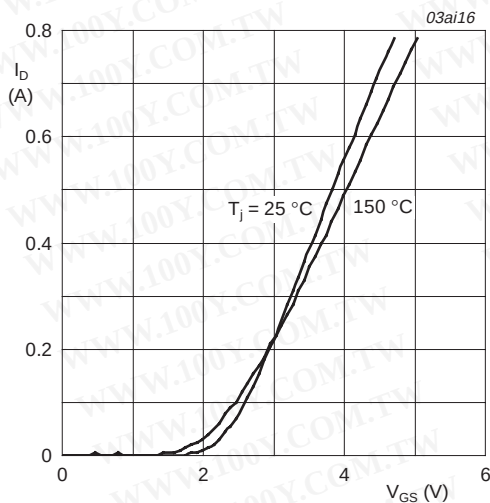
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



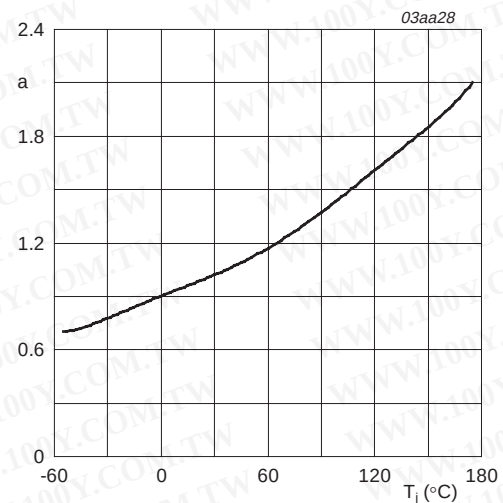
$T_j = 25\text{ °C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



$T_j = 25\text{ °C and } 150\text{ °C}; V_{DS} > I_D \times R_{DSon}$

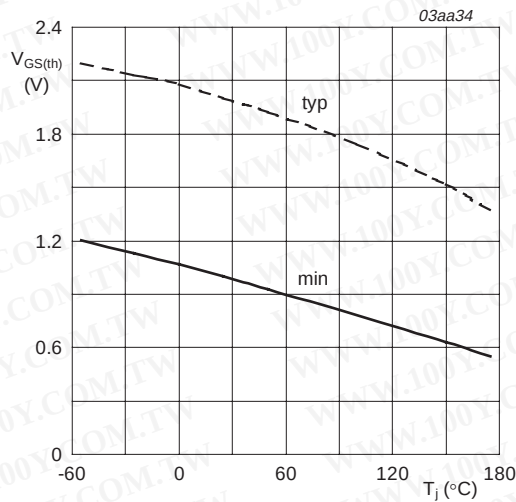
Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

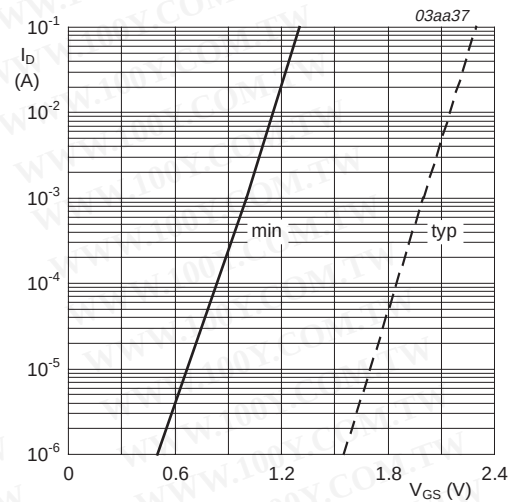
Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature

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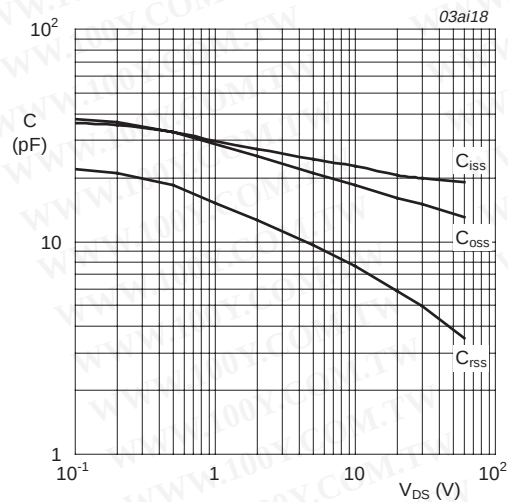
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



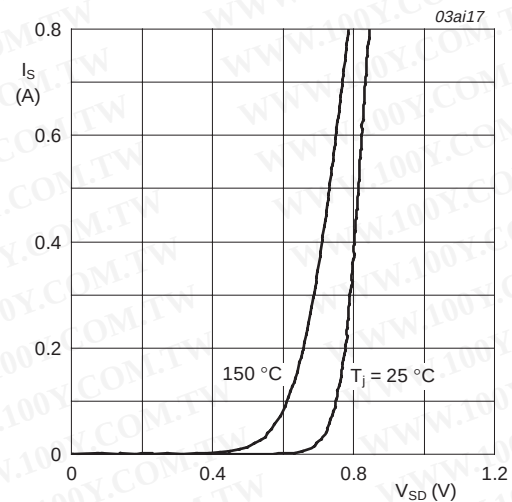
$T_J = 25 \text{ °C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_J = 25 \text{ °C and } 150 \text{ °C}$; $V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

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7. Package outline

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Plastic surface mounted package; 3 leads

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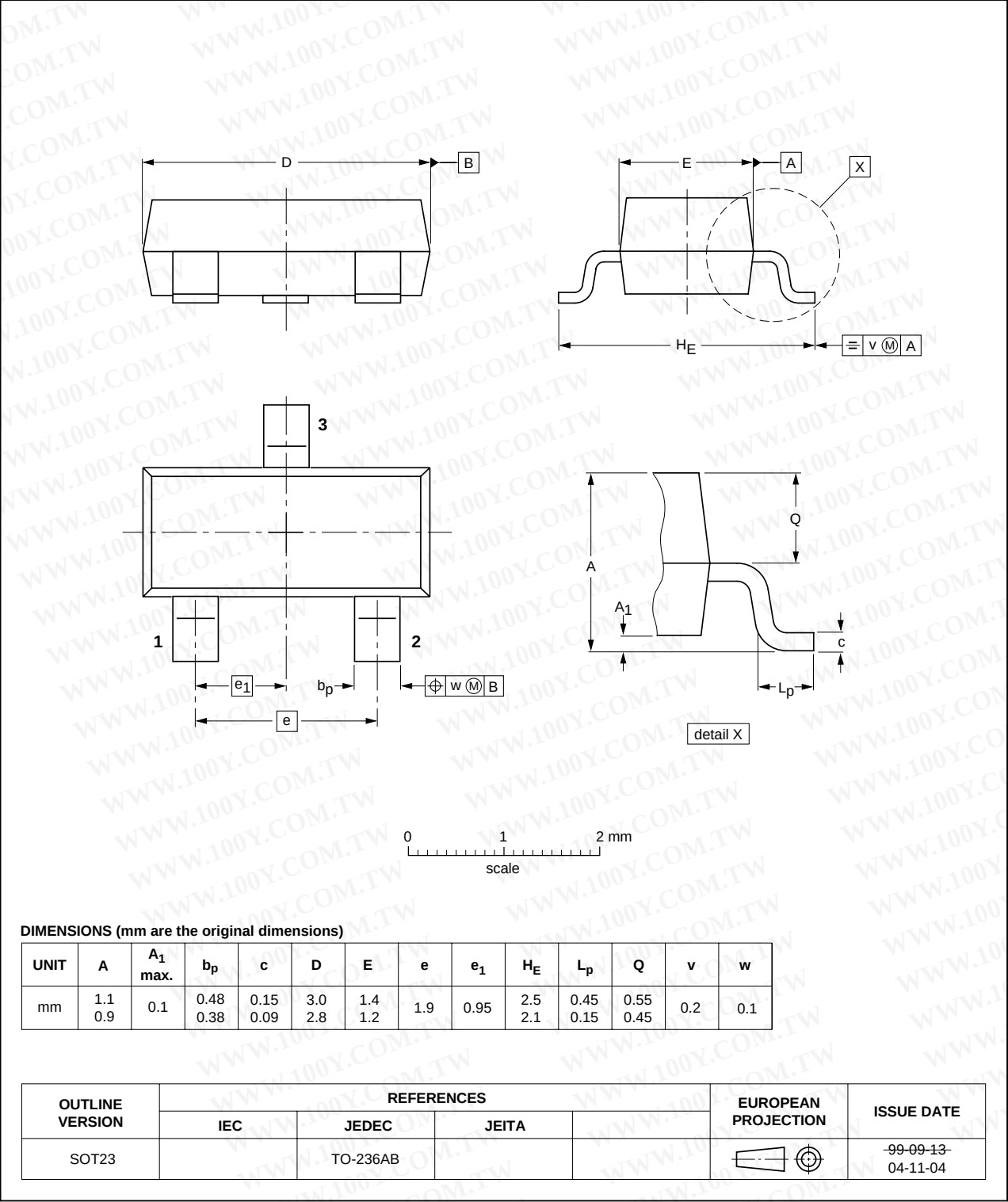


Fig 13. Package outline SOT23



8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
2N7002E_2	20050426	Product data sheet	-	9397 750 14944	2N7002E-01
Modifications:					
- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Table 5 "Characteristics" Addition of upper limit for $V_{GS(th)}$.					
2N7002E-01	20020211	Product data	-	9397 750 09095	-

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9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

10. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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13. Contact information

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