ANALOG DEVICES

Precision, Micropower Operational Amplifiers

OP193/OP293/OP493*

FEATURES

- Operates from +1.7 V to ±18 V
- Low Supply Current: 15 µA/Amplifier
- Low Offset Voltage: 75 µV
- Outputs Sink and Source: ±8 mA
- No Phase Reversal
- Single or Dual Supply Operation
- High Open-Loop Gain: 600 V/mV
- Unity-Gain Stable

APPLICATIONS

- Digital Scales
- Strain Gages
- Portable Medical Equipment
- Battery Powered Instrumentation
- Temperature Transducer Amplifier

GENERAL DESCRIPTION

The OP193 family of single-supply operational amplifiers features a combination of high precision, low supply current and the ability to operate at low voltages. For high performance in single supply systems the input and output ranges include ground, and the outputs swing from the negative rail to within 600 mV of the positive supply. For low voltage operation the OP193 family can operate down to 1.7 volts or ±0.85 volts.

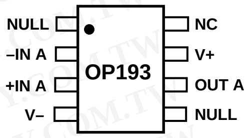
The combination of high accuracy and low power operation make the OP193 family useful for battery powered equipment. Its low current drain and low voltage operation allow it to continue performing long after other amplifiers have ceased functioning either because of battery drain or headroom.

The OP193 family is specified for single +2 volt through dual ±15 volt operation over the HOT (–40°C to +125°C) temperature range. They are available in plastic DIPs, plus SOIC surface mount packages.

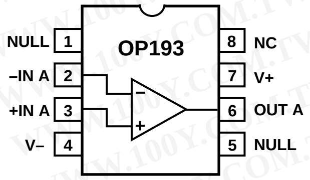
*Patent pending.

PIN CONFIGURATIONS

8-Lead SO (S Suffix)

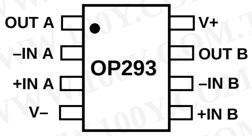


8-Lead Epoxy DIP (P Suffix)

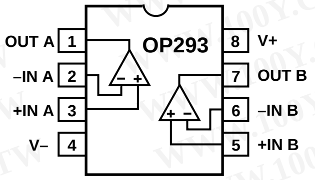


NC = NO CONNECT

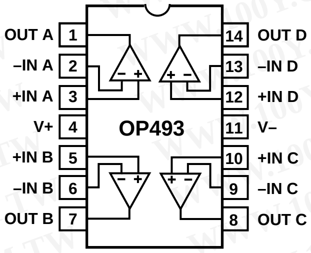
8-Lead SO (S Suffix)



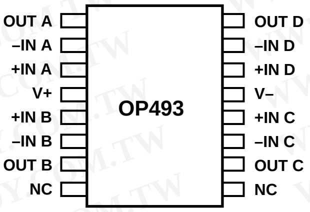
8-Lead Epoxy DIP (P Suffix)



14-Lead Epoxy DIP (P Suffix)



16-Lead Wide Body SOL (S Suffix)



NC = NO CONNECT

REV. A

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Tel: 617/329-4700 Fax: 617/326-8703

OP193/OP293/OP493–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

			“E” Grade			“F” Grade			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP193			75			150	µV
		OP193, –40°C ≤ T_A ≤ +125°C			175			250	µV
		OP293			100			250	µV
		OP293, –40°C ≤ T_A ≤ +125°C			200			350	µV
		OP493			125			275	µV
		OP493, –40°C ≤ T_A ≤ +125°C			225			375	µV
Input Bias Current	I_B	V_{CM} = 0 V, –40°C ≤ T_A ≤ +125°C			15			20	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V, –40°C ≤ T_A ≤ +125°C			2			4	nA
Input Voltage Range	V_{CM}		–14.9		+13.5	–14.9		+13.5	V
Common-Mode Rejection	CMRR	–14.9 ≤ V_{CM} ≤ +14 V	100	116		97	116		dB
		–14.9 ≤ V_{CM} ≤ +14 V, –40°C ≤ T_A ≤ +125°C	97			94			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, –10 V ≤ V_{OUT} ≤ +10 V	500			500			V/mV
		–40°C ≤ T_A ≤ +85°C	300			300			V/mV
		–40°C ≤ T_A ≤ +125°C		300			300		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, –10 V ≤ V_{OUT} ≤ +10 V	350			350			V/mV
		–40°C ≤ T_A ≤ +85°C	200			200			V/mV
		–40°C ≤ T_A ≤ +125°C		150			150		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, –10 V ≤ V_{OUT} ≤ +10 V	200			200			V/mV
		–40°C ≤ T_A ≤ +85°C	125			125			V/mV
		–40°C ≤ T_A ≤ +125°C		100			100		V/mV
Long Term Offset Voltage	V_{OS}	Note 1			150			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2		0.2	1.75				µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	I_L = 1 mA	+14.1	14.2		+14.1	14.2		V
		I_L = 1 mA, –40°C ≤ T_A ≤ +125°C	+14.0			+14.0			V
		I_L = 5 mA	+13.9	14.1		+13.9	14.1		V
Output Voltage Swing Low	V_{OL}	I_L = –1 mA		–14.7	–14.6		-14.7	–14.6	V
		I_L = –1 mA, –40°C ≤ T_A ≤ +125°C			–14.4			–14.4	V
		I_L = –5 mA		14.2	–14.1		14.2	–14.1	V
Short Circuit Current	I_{SC}			±25			±25		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±1.5 V to ±18 V	100	120		97	120		dB
		V_S = ±1.5 V to ±18 V, –40°C ≤ T_A ≤ +125°C	97			94			dB
Supply Current/Amplifier	I_{SY}	–40°C ≤ T_A ≤ +125°C, R_L = ∞, V_{OUT} = 0 V, V_S = ±18 V			30			30	µA
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		65			65		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		3			3		µV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		15			15		V/ms
Gain Bandwidth Product	GBP			35			35		kHz
Channel Separation		V_{OUT} = 10 V p-p, R_L = 2 kΩ, f = 1 kHz		120			120		dB

NOTES

[1] Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.

[2] Offset voltage drift is the average of the –40°C to +25°C delta and the +25°C to +125°C delta.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = 0.1 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	"E" Grade			"F" Grade			Units
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP193			75			150	µV
		OP193, –40°C ≤ T_A ≤ +125°C			175			250	µV
		OP293			100			250	µV
		OP293, –40°C ≤ T_A ≤ +125°C			200			350	µV
		OP493			125			275	µV
		OP493, –40°C ≤ T_A ≤ +125°C			225			375	µV
Input Bias Current	I_B	–40°C ≤ T_A ≤ +125°C			15			20	nA
Input Offset Current	I_{OS}	–40°C ≤ T_A ≤ +125°C			2			4	nA
Input Voltage Range	V_{CM}		0		4	0		4	V
Common-Mode Rejection	CMRR	0.1 ≤ V_{CM} ≤ +4 V	100	116		96	116		dB
		0.1 ≤ V_{CM} ≤ +4 V, –40°C ≤ T_A ≤ +125°C	92			92			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, 0.03 ≤ V_{OUT} ≤ +4.0 V	200			200			V/mV
		–40°C ≤ T_A ≤ +85°C	125			125			V/mV
		–40°C ≤ T_A ≤ +125°C		130			130		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.03 ≤ V_{OUT} ≤ +4.0 V	75			75			V/mV
		–40°C ≤ T_A ≤ +85°C	50			50			V/mV
		–40°C ≤ T_A ≤ +125°C		70			70		V/mV
Long Term Offset Voltage	V_{OS}	Note 1			150			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2		0.2	1.25				µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	I_L = 100 µA		4.4			4.4		V
		I_L = 1 mA	+4.1	4.4		+4.1	4.4		V
		I_L = 1 mA, –40°C ≤ T_A ≤ +125°C	+4.0			+4.0			V
		I_L = 5 mA	+4.0	4.4		+4.0	4.4		V
Output Voltage Swing Low	V_{OL}	I_L = –100 µA		140	160		140	160	mV
		I_L = –100 µA, –40°C ≤ T_A ≤ +125°C			220			220	mV
		No Load		5			5		mV
		I_L = –1 mA		280	400		280	400	mV
		I_L = –1 mA, –40°C ≤ T_A ≤ +125°C			500			500	mV
		I_L = –5 mA		700	900		700	900	mV
Short Circuit Current	I_{SC}			±8			±8		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±1.7 V to ±6.0 V	100	120		97	120		dB
		V_S = ±1.5 V to ±18 V, –40°C ≤ T_A ≤ +125°C	94			90			dB
Supply Current/Amplifier	I_{SY}	V_{CM} = 2.5 V, R_L = ∞		14.5			14.5		µA
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		65			65		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		3			3		µV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		12			12		V/ms
Gain Bandwidth Product	GBP			35			35		kHz

NOTES

[1] Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125°C, with an LTPD of 1.3.

[2] Offset voltage drift is the average of the –40°C to +25°C delta and the +25°C to +125°C delta.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_S = +3.0 V, V_{CM} = 0.1 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	"E" Grade Min	Typ	Max	"F" Grade Min	Typ	Max	Units
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP193			75			150	µV
		OP193, –40°C ≤ T_A ≤ +125°C			175			250	µV
		OP293			100			250	µV
		OP293, –40°C ≤ T_A ≤ +125°C			200			350	µV
		OP493			125			275	µV
		OP493, –40°C ≤ T_A ≤ +125°C			225			375	µV
Input Bias Current	I_B	–40°C ≤ T_A ≤ +125°C			15			20	nA
Input Offset Current	I_{OS}	–40°C ≤ T_A ≤ +125°C			2			4	nA
Input Voltage Range	V_{CM}		0		2	0		2	V
Common-Mode Rejection	CMRR	0.1 ≤ V_{CM} ≤ +2 V	97	116		94	116		dB
		0.1 ≤ V_{CM} ≤ +2 V,							
		–40°C ≤ T_A ≤ +125°C	90			87			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, 0.03 ≤ V_{OUT} ≤ 2 V	100			100			V/mV
		–40°C ≤ T_A ≤ +85°C	75			75			V/mV
		–40°C ≤ T_A ≤ +125°C		100			100		V/mV
Long Term Offset Voltage	V_{OS}	Note 1			150			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2		0.2	1.25				µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	I_L = 1 mA	+2.1	2.14		+2.1	2.14		V
		I_L = 1 mA,							
		–40°C ≤ T_A ≤ +125°C	1.9			1.9			V
		I_L = 5 mA	+1.9	2.1		+1.9	2.1		V
Output Voltage Swing Low	V_{OL}	I_L = –1 mA		280	400		280	400	mV
		I_L = –1 mA							
		–40°C ≤ T_A ≤ +125°C			500			500	mV
		I_L = –5 mA		700	900		700	900	mV
Short Circuit Current	I_{SC}			±8			±8		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = +1.7 V to +6 V,	100			97			
		–40°C ≤ T_A ≤ +125°C	94			90			dB
Supply Current/Amplifier	I_{SY}	V_{CM} = 1.5 V, R_L = ∞		14.5	22		14.5	22	µA
		–40°C ≤ T_A ≤ +125°C			22			22	µA
Supply Voltage Range	V_S		+2		±18	+2		±18	V
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		65			65		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		3			3		µV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		10			10		V/ms
Gain Bandwidth Product	GBP			25			25		kHz
Channel Separation		V_{OUT} = 10 V p-p,							
		R_L = 2 kΩ, f = 1 kHz		120			120		dB

NOTES

[1] Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125°C, with an LTPD of 1.3.

[2] Offset voltage drift is the average of the –40°C to +25°C delta and the +25°C to +125°C delta.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_S = +2.0 V, V_{CM} = 0.1 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	"E" Grade Min	"E" Grade Typ	"E" Grade Max	"F" Grade Min	"F" Grade Typ	"F" Grade Max	Units
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP193			75			150	μV
		OP193, $-40°C \le T_A \le +125°C$			175			250	μV
		OP293			100			250	μV
		OP293, $-40°C \le T_A \le +125°C$			175			350	μV
		OP493			125			275	μV
		OP493, $-40°C \le T_A \le +125°C$			225			375	μV
Input Bias Current	I_B	$-40°C \le T_A \le +125°C$			15			20	nA
Input Offset Current	I_{OS}	$-40°C \le T_A \le +125°C$			2			4	nA
Input Voltage Range	V_{CM}		0		1	0		1	V
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, $0.03 \le V_{OUT} \le 1$ V	60			60			V/mV
		$-40°C \le T_A \le +125°C$		70			70		V/mV
Long Term Offset Voltage	V_{OS}	Note 1			150			300	μV
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = +1.7 V to +6 V,	100			97			
		$-40°C \le T_A \le +125°C$	94			90			dB
Supply Current/Amplifier	I_{SY}	V_{CM} = 1.0 V, $R_L = \infty$		13.2	20		13.2	20	μA
		$-40°C \le T_A \le +125°C$			25			25	μA
Supply Voltage Range	V_S		+2		±18	+2		±18	V
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		65			65		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		$pA/\sqrt{Hz}$
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		3			3		μV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		10			10		V/ms
Gain Bandwidth Product	GBP			25			25		kHz

WAFER TEST LIMITS (@ V_S = +5.0 V, V_{CM} = 0.1 V, V_{OUT} = 2 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	V_S = ±15 V, V_{OUT} = 0 V	±75	μV max
		V_S = +2 V, V_{OUT} = 1.0 V	±75	μV max
Input Bias Current	I_B	V_{CM} = 1.0 V	20	nA max
Input Offset Current	I_{OS}	V_{CM} = 1.0 V	4	nA max
Input Voltage Range[1]	V_{CM}		0 to 4	V min
Common-Mode Rejection	CMRR	$0 \le V_{CM} \le 4$ V	96	dB min
Power Supply Rejection Ratio	PSRR	V_S = ±1.5 V to ±18 V	100	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ	100	V/mV min
Output Voltage Swing High	V_{OH}	I_L = 1 mA	4.1	V min
Output Voltage Swing Low	V_{OL}	I_L = –1 mA	400	mV max
Supply Current/Amplifier	I_{SY}	V_O = 0 V, $R_L = \infty$, V_S = ±18 V	25	μA max

NOTES

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

[1] Guaranteed by CMRR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Input Voltage[2] . . . . ±18 V
Differential Input Voltage[2] . . . . ±18 V
Output Short-Circuit Duration to Gnd . . . . Indefinite
Storage Temperature Range
  P, S Package . . . . –65°C to +150°C
Operating Temperature Range
  OP193/OP293/OP493E, F . . . . –40°C to +125°C
Junction Temperature Range
  P, S Package . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES

[1] Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

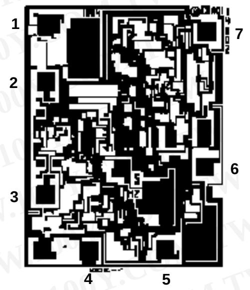
[2] For supply voltages less than ±18 V, the input voltage is limited to the supply voltage.

[3] θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP, and θ_{JA} is specified for device soldered in circuit board for SOIC package.

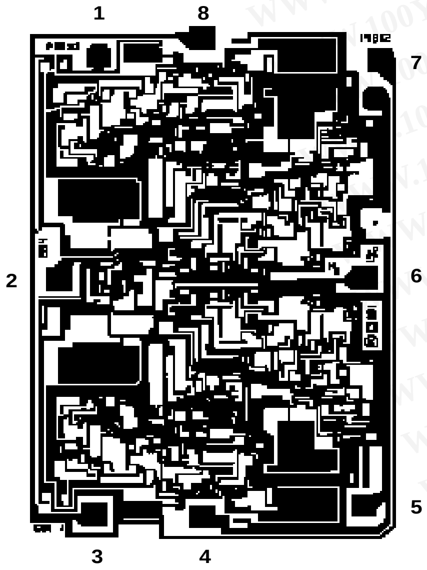
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP193EP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP193ES	–40°C to +125°C	8-Pin SOIC	SO-8
OP193ES-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP193ES-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP193FP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP193FS	–40°C to +125°C	8-Pin SOIC	SO-8
OP193FS-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP193FS-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP193GBC	+25°C	DICE	
OP293EP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP293ES	–40°C to +125°C	8-Pin SOIC	SO-8
OP293ES-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP293ES-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP293FP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP293FS	–40°C to +125°C	8-Pin SOIC	SO-8
OP293FS-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP293FS-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP293GBC	+25°C	DICE	
OP493EP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP493ES	–40°C to +125°C	16-Pin SOL	SOL-16
OP493ES-REEL	–40°C to +125°C	16-Pin SOL	SOL-16
OP493FP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP493FS	–40°C to +125°C	16-Pin SOL	SOL-16
OP493FS-REEL	–40°C to +125°C	16-Pin SOL	SOL-16
OP493GBC	+25°C	DICE	

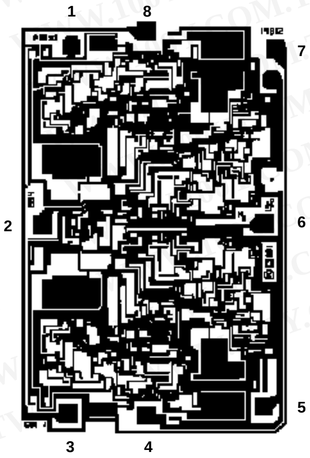
DICE CHARACTERISTICS



OP193 Die Size 0.070 × 0.055 Inch, 3,850 Sq. Mils Substrate (Die Backside) Is Connected to V– Transistor Count, 55



OP493 Die Size 0.106 × 0.143 Inch, 15,158 Sq. Mils Substrate (Die Backside) Is Connected to V– Transistor Count, 215



OP293 Die Size 0.072 × 0.110 Inch, 7,920 Sq. Mils Substrate (Die Backside) Is Connected to V– Transistor Count, 105

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP193/OP293/OP493 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Performance Characteristics–OP193/OP293/OP493

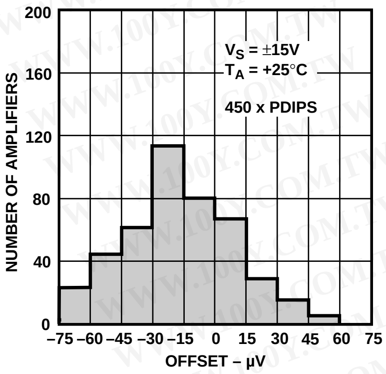


Figure 1. OP193 Offset Distribution, $V_S = \pm15$ V

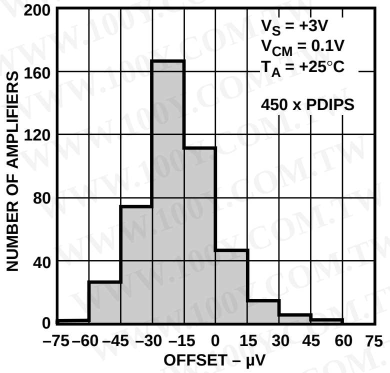


Figure 2. OP193 Offset Distribution, $V_S = +3$ V

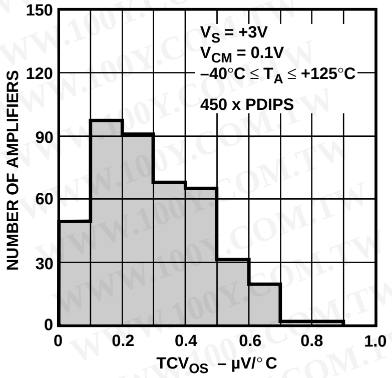


Figure 3. OP193 TCV_{OS} Distribution, $V_S = +3$ V

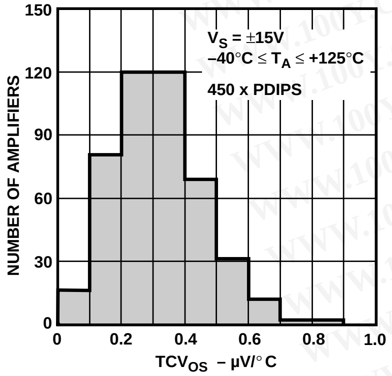


Figure 4. OP193 TCV_{OS} Distribution, $V_S = \pm15$ V

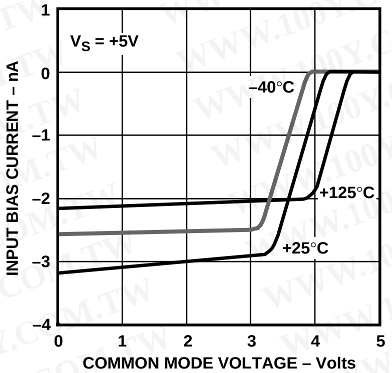


Figure 5. Input Bias Current vs. Common-Mode Voltage

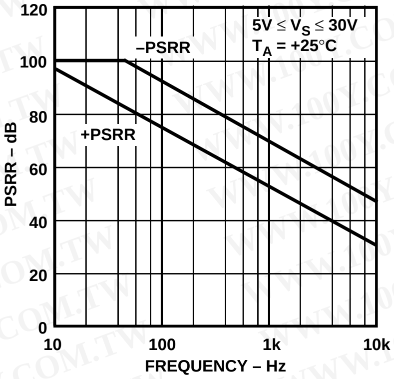


Figure 6. PSRR vs. Frequency

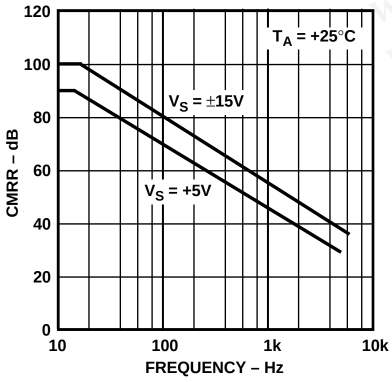


Figure 7. CMRR vs. Frequency

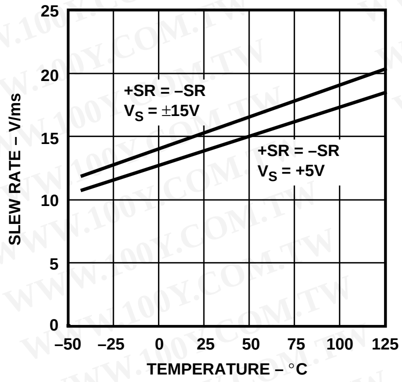


Figure 8. Slew Rate vs. Temperature

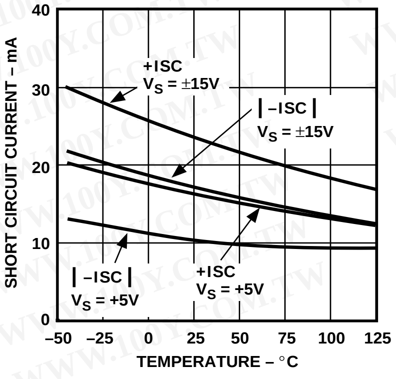


Figure 9. Short Circuit Current vs. Temperature

OP193/OP293/OP493–Typical Performance Characteristics

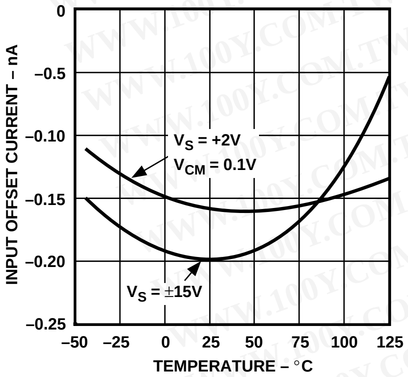


Figure 10. Input Offset Current vs. Temperature

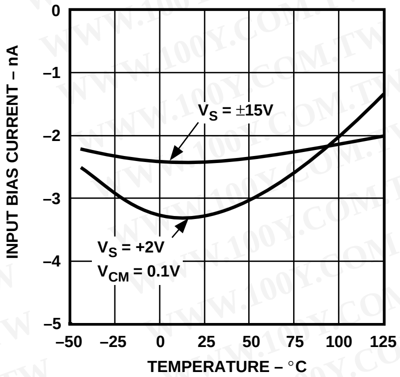


Figure 11. Input Bias Current vs. Temperature

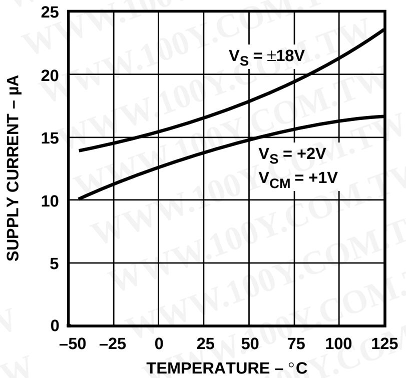


Figure 12. Supply Current vs. Temperature

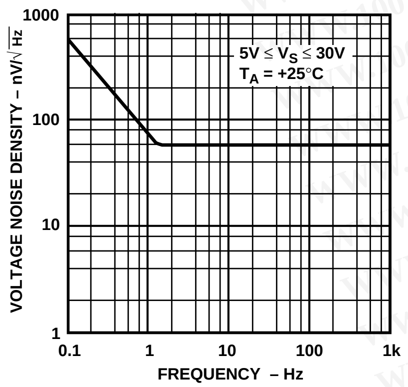


Figure 13. Voltage Noise Density vs. Frequency

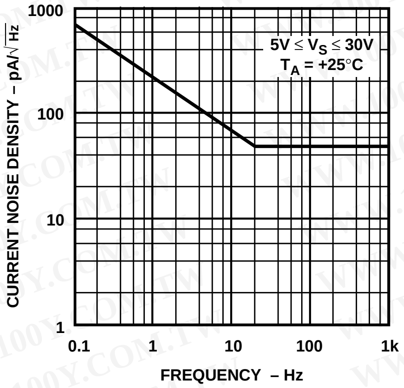


Figure 14. Current Noise Density vs. Frequency

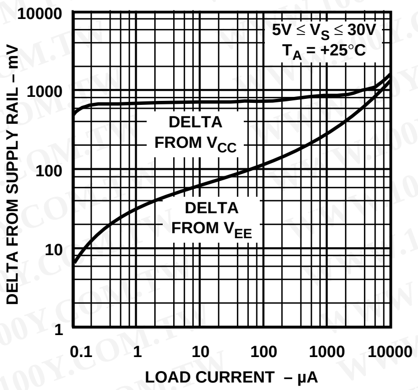


Figure 15. Delta Output Swing from Either Rail vs. Current Load

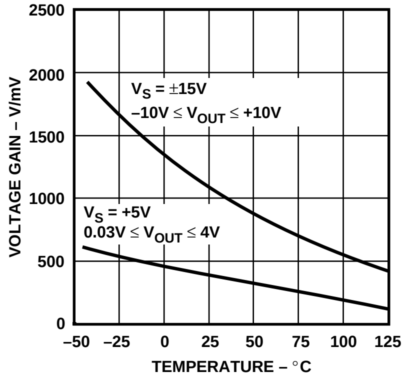


Figure 16. Voltage Gain (R_L = 100 kΩ) vs. Temperature

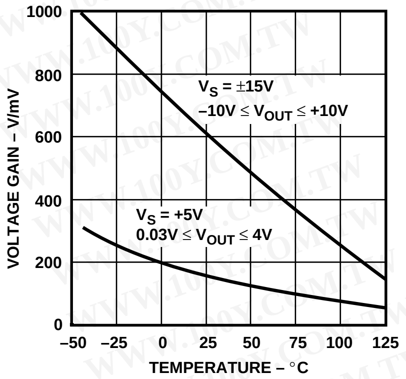


Figure 17. Voltage Gain (R_L = 10 kΩ) vs. Temperature

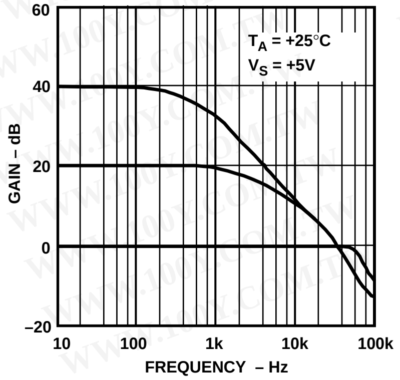


Figure 18. Closed-Loop Gain vs. Frequency, V_S = 5 V

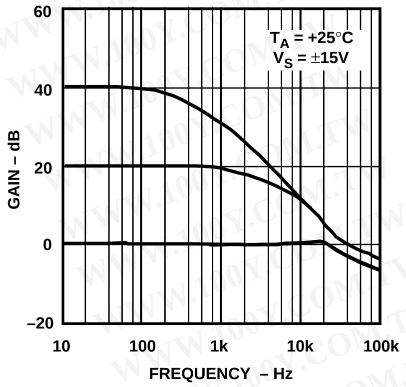


Figure 19. Closed-Loop Gain vs. Frequency, $V_S = \pm 15$ V

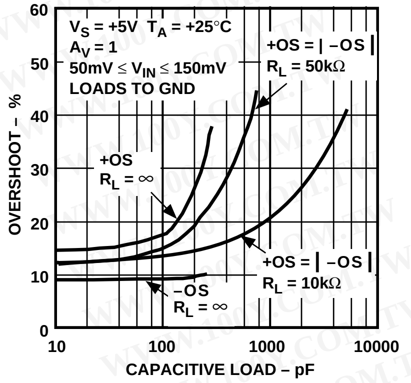


Figure 20. Small Signal Overshoot vs. Capacitive Load

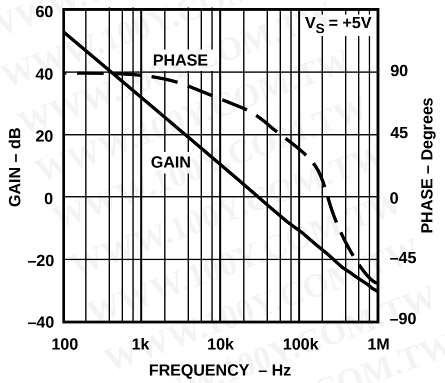


Figure 21. Open Loop, Gain and Phase vs. Frequency

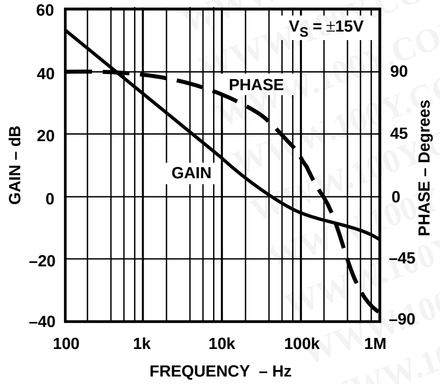


Figure 22. Open Loop, Gain and Phase vs. Frequency

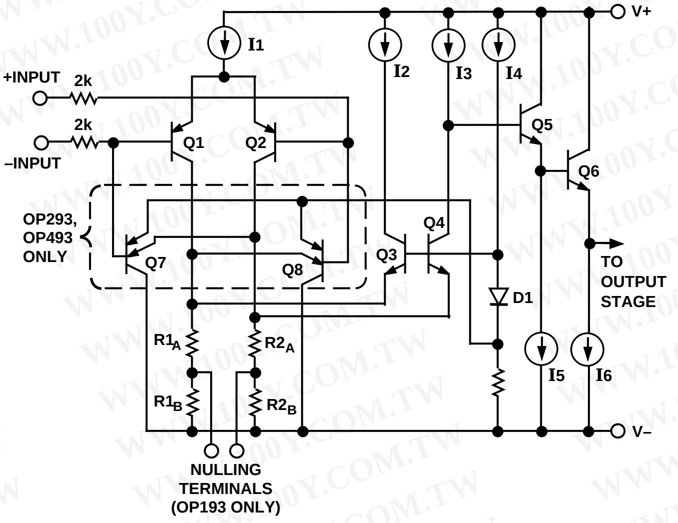


Figure 23. OP193/OP293/OP493 Equivalent Input Circuit

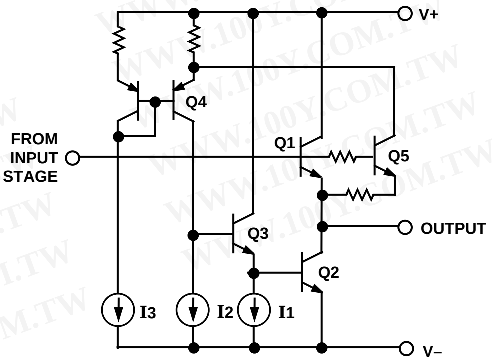


Figure 24. OP193/OP293/OP493 Equivalent Output Circuit

FUNCTIONAL DESCRIPTION

The OP193 family of operational amplifiers are single-supply, micropower, precision amplifiers whose input and output ranges both include ground. Input offset voltage (V_{OS}) is only 75 µV maximum, while the output will deliver ±5 mA to a load. Supply current is only 17 µA.

A simplified schematic of the input stage is shown in Figure 23. Input transistors Q1 and Q2 are PNP devices, which permit the inputs to operate down to ground potential. The input transistors have resistors in series with the base terminals to protect the junctions from over voltage conditions. The second stage is an NPN cascode which is buffered by an emitter follower before driving the final PNP gain stage.

The OP193 includes connections to taps on the input load resistors, which can be used to null the input offset voltage, V_{OS}. The OP293 and OP493 have two additional transistors, Q7 and Q8. The behavior of these transistors is discussed in the Output Phase Reversal section of this data sheet.

The output stage, shown in Figure 24, is a noninverting NPN "totem-pole" configuration. Current is sourced to the load by emitter follower Q1, while Q2 provides current sink capability. When Q2 saturates, the output is pulled to within 5 mV of ground without an external pull-down resistor. The totem-pole output stage will supply a minimum of 5 mA to an external load, even when operating from a single 3.0 V power supply.

By operating as an emitter follower, Q1 offers a high impedance load to the final PNP collector of the input stage. Base drive to Q2 is derived by monitoring Q1's collector current. Transistor Q5 tracks the collector current of Q1. When Q1 is on, Q5 keeps Q4 off, and current source I1 keeps Q2 turned off. When Q1 is driven to cutoff (i.e., the output must move toward V–), Q5 allows Q4 to turn on. Q4's collector current then provides the base drive for Q3 and Q2, and the output low voltage swing is set by Q2's $V_{CE,SAT}$ which is about 5 mV.

Driving Capacitive Loads

OP193 family amplifiers are unconditionally stable with capacitive loads less than 200 pF. However, the small signal, unity-gain overshoot will improve if a resistive load is added. For example, transient overshoot is 20% when driving a 1000 pF/ 10 kΩ load. When driving large capacitive loads in unity-gain configurations, an in-the-loop compensation technique is recommended as illustrated in Figure 28.

Input Overvoltage Protection

As previously mentioned, the OP193 family of op amps use a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors, coupled with the protection resistors, provides a large amount of input protection from over voltage conditions. The inputs can therefore be taken 20 V beyond either supply without damaging the amplifier.

Output Phase Reversal—OP193

The OP193's input PNP collector-base junction can be forward-biased if the inputs are brought more than one diode drop (0.7 V) below ground. When this happens to the noninverting input, Q4 of the cascode stage turns on and the output goes high. If the positive input signal can go below ground, phase reversal can be prevented by clamping the input to the negative supply (i.e., GND) with a diode. The reverse leakage of the diode will, of course, add to the input bias current of the amplifier. If input bias current is not critical, a 1N914 will add less than 10 nA of leakage. However, its leakage current will double for every 10°C increase in ambient temperature. For critical applications, the collector-base junction of a 2N3906 transistor will only add about 10 pA of additional bias current. To limit the current through the diode under fault conditions, a 1 kΩ resistor is recommended in series with the input. (The OP193's internal current limiting resistors will not protect the external diode).

Output Phase Reversal—OP293 and OP493

The OP293 and OP493 include lateral PNP transistors Q7 and Q8 to protect against phase reversal. If an input is brought more than one diode drop (≈0.7 V) below ground, Q7 and Q8 combine to level shift the entire cascode stage, including the bias to Q3 and Q4, simultaneously. In this case Q4 will not saturate and the output remains low.

The OP293 and OP493 do not exhibit output phase reversal for inputs up to –5 V below V– at +25°C. The phase reversal limit at +125°C is about –3 V. If the inputs can be driven below these levels, an external clamp diode, as discussed in the previous section, should be added.

Battery Powered Applications

OP193 series op amps can be operated on a minimum supply voltage of +1.7 V, and draw only 13 µA of supply current per amplifier from a 2.0 V supply. In many battery-powered circuits, OP193 devices can be continuously operated for thousands of hours before requiring battery replacement, thus reducing equipment downtime and operating cost.

High performance portable equipment and instruments frequently use lithium cells because of their long shelf life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3 V and are noted for a flat discharge characteristic. The low supply voltage requirement of the OP193, combined with the flat discharge characteristic of the lithium cell, indicates that the OP193 can be operated over the entire useful life of the cell. Figure 25 shows the typical discharge characteristic of a 1 AH lithium cell powering the OP193, OP293, and OP493, with each amplifier, in turn, driving 2.1 Volts into a 100 kΩ load.

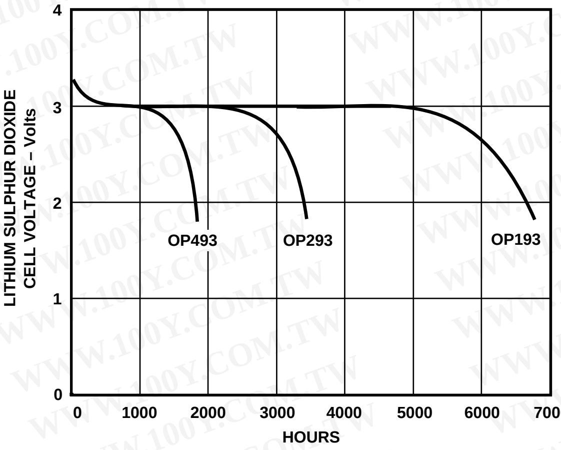


Figure 25. Lithium Sulfur Dioxide Cell Discharge Characteristic with OP193 Family and 100 kΩ Loads

Input Offset Voltage Nulling

The OP193 provides two offset nulling terminals that can be used to adjust the OP193's internal V_{OS}. In general, operational amplifier terminals should never be used to adjust system offset voltages. The offset null circuit of Figure 26 provides about ±7 mV of offset adjustment range. A 100 kΩ resistor placed in series with the wiper arm of the offset null potentiometer, as shown in Figure 27, reduces the offset adjustment range to 400 µV and is recommended for applications requiring high null resolution. Offset nulling does not adversely affect TCV_{OS} performance, providing that the trimming potentiometer temperature coefficient does not exceed ±100 ppm/°C.

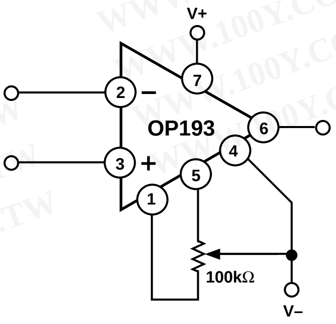


Figure 26. Offset Nulling Circuit

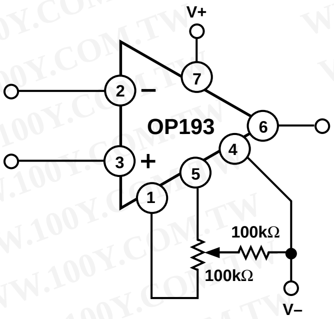


Figure 27. High Resolution Offset Nulling Circuit

A Micropower False-Ground Generator

Some single supply circuits work best when inputs are biased above ground, typically at 1/2 of the supply voltage. In these cases a false ground can be created by using a voltage divider buffered by an amplifier. One such circuit is shown in Figure 28.

This circuit will generate a false-ground reference at 1/2 of the supply voltage, while drawing only about 27 µA from a 5 V supply. The circuit includes compensation to allow for a 1 µF bypass capacitor at the false-ground output. The benefit of a large capacitor is that not only does the false ground present a very low dc resistance to the load, but its ac impedance is low as well. The OP193 can both sink and source more than 5 mA, which improves recovery time from transients in the load current.

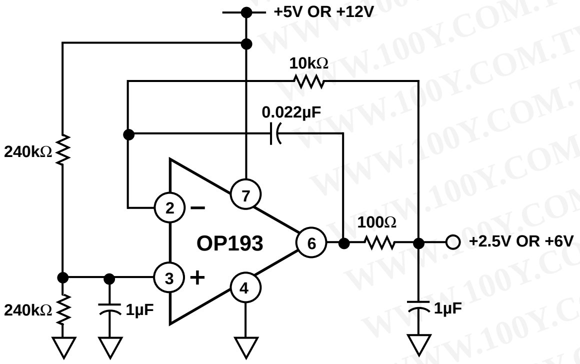


Figure 28. A Micropower False-Ground Generator

A Battery Powered Voltage Reference

The circuit of Figure 29 is a battery-powered voltage reference that draws only 17 µA of supply current. At this level, two AA alkaline cells can power this reference for more than 18 months. At an output voltage of 1.23 V @ 25°C, drift of the reference is only 5.5 µV/°C over the industrial temperature range. Load regulation is 85 µV/mA with line regulation at 120 µV/V.

Design of the reference is based on the Brokaw bandgap core technique. Scaling of resistors R1 and R2 produces unequal currents in Q1 and Q2. The resulting ΔV_{BE} across R3 creates a temperature-proportional voltage (PTAT) which, in turn, produces a larger temperature-proportional voltage across R4 and R5, V1. The temperature coefficient of V1 cancels (first order) the complementary to absolute temperature (CTAT) coefficient of V_{BE1}. When adjusted to 1.23 V @ +25°C, output voltage tempco is at a minimum. Bandgap references can have start-up problems. With no current in R1 and R2, the OP193 is beyond its positive input range limit and has an undefined output state. Shorting Pin 5 (an offset adjust pin) to ground forces the output high under these circumstances and insures reliable startup without significantly degrading the OP193's offset drift.

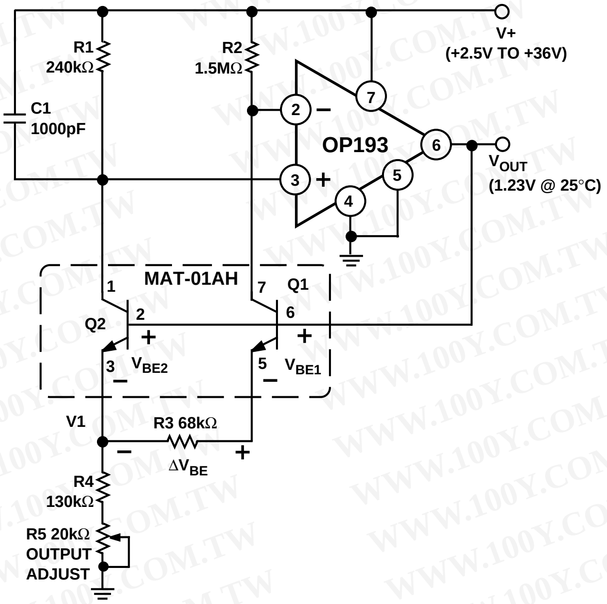


Figure 29. A Battery Powered Voltage Reference

A Single-Supply Current Monitor

Current monitoring essentially consists of amplifying the voltage drop across a resistor placed in series with the current to be measured. The difficulty is that only small voltage drops can be tolerated, and with low precision op amps this greatly limits the overall resolution. The single-supply current monitor of Figure 30 has a resolution of 10 µA and is capable of monitoring 30 mA of current. This range can be adjusted by changing the current sense resistor R1. When measuring total system current, it may be necessary to include the supply current of the current monitor, which bypasses the current sense resistor, in the final result. This current can be measured and calibrated (together with the residual offset) by adjustment of the offset trim potentiometer, R2. This produces a deliberate temperature dependent offset. However, the supply current of the OP193 is also proportional to temperature, and the two effects tend to track. Current in R4 and R5, which also bypasses R1, can be adjusted via a gain trim.

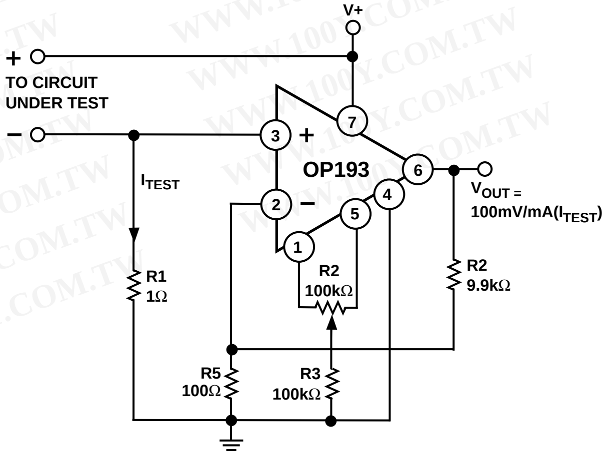


Figure 30. Single-Supply Current Monitor

A Single-Supply Instrumentation Amplifier

Designing a true single-supply instrumentation amplifier with zero-input and zero-output operation requires special care. The traditional configuration, shown in Figure 31, depends upon amplifier A1's output being at 0 V when the applied common-mode input voltage is at 0 V. Any error at the output is multiplied by the gain of A2. In addition, current flows through resistor R3 as A2's output voltage increases. A1's output must remain at 0 V while sinking the current through R3, or a gain error will result. With a maximum output voltage of 4 V, the current through R3 is only 2 µA, but this will still produce an appreciable error.

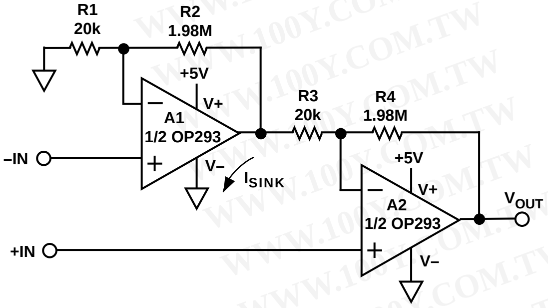


Figure 31. A Conventional Instrumentation Amplifier

One solution to this problem is to use a pull-down resistor. For example, if R3 = 20 kΩ, then the pull-down resistor must be less than 400 Ω. However, the pull-down resistor appears as a fixed load when a common-mode voltage is applied. With a 4 V common-mode voltage, the additional load current will be 10 mA, which is unacceptable in a low power application.

Figure 32 shows a better solution. A1's sink current is provided by a pair of N-channel FET transistors, configured as a current mirror. With the values shown, sink current of Q2 is about 340 µA. Thus, with a common-mode voltage of 4 V, the additional load current is limited to 340 µA versus 10 mA with a 400 Ω resistor.

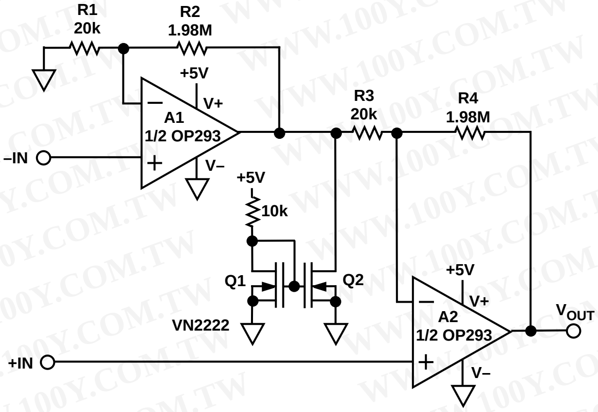


Figure 32. An Improved Single-Supply, 0 V_{IN}, 0 V_{OUT} Instrumentation Amplifier

A Low-Power, Temperature to 4–20 mA Transmitter

A simple temperature to 4–20 mA transmitter is shown in Figure 33. After calibration, this transmitter is accurate to ±0.5°C over the –50°C to +150°C temperature range. The transmitter operates from +8 V to +40 V with supply rejection better than 3 ppm/V. One half of the OP293 is used to buffer the V_{TEMP} pin, while the other half regulates the output current to satisfy the current summation at its noninverting input:

$$I_{OUT} + \frac{V_{TEMP} \times (R6 + R7)}{R2 \times R10} - V_{SET}\left(\frac{R2 + R6 + R7}{R2 \times R10}\right)$$

The change in output current with temperature is the derivative of the transfer function:

$$\frac{\Delta I_{OUT}}{\Delta T} = \frac{\frac{\Delta V_{TEMP}}{\Delta T}(R6 + R7)}{R2 \times R10}$$

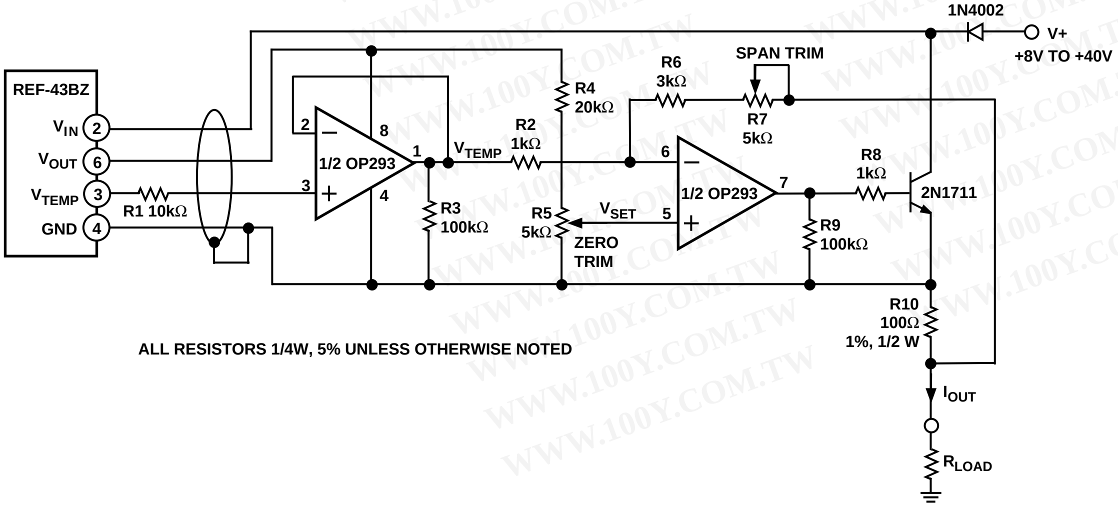


Figure 33. Temperature to 4–20 mA Transmitter

From the formulas, it can be seen that if the span trim is adjusted before the zero trim, the two trims are not interactive, which greatly simplifies the calibration procedure.

Calibration of the transmitter is simple. First, the slope of the output current versus temperature is calibrated by adjusting the span trim, R7. A couple of iterations may be required to be sure the slope is correct.

Once the span trim has been completed, the zero trim can be made. Remember that adjusting the zero trim will not affect the gain.

The zero trim can be set at any known temperature by adjusting R5 until the output current equals:

$$I_{OUT} = \left(\frac{\Delta I_{FS}}{\Delta T_{OPERATING}}\right)(T_{AMBIENT} - T_{MIN}) + 4\ mA$$

Table I shows the values of R6 required for various temperature ranges.

Table I. R6 Values vs. Temperature

Temp Range	R6
0°C to +70°C	10 kΩ
–40°C to +85°C	6.2 kΩ
–55°C to +150°C	3 kΩ

A Micropower Voltage Controlled Oscillator

An OP293 in combination with an inexpensive quad CMOS analog switch forms the precision VCO of Figure 34. This circuit provides triangle and square wave outputs and draws only 50 µA from a single 5 V supply. A1 acts as an integrator; S1 switches the charging current symmetrically to yield positive and negative ramps. The integrator is bounded by A2 which acts as a Schmitt trigger with a precise hysteresis of 1.67 volts, set by resistors R5, R6, and R7, and associated CMOS switches. The resulting output of A1 is a triangle wave with upper and lower levels of 3.33 and 1.67 volts. The output of A2 is a square wave with almost rail-to-rail swing. With the components shown, frequency of operation is given by the equation:

$$f_{OUT} = V_{CONTROL}\,(Volts) \times 10\ Hz/V$$

but this can easily be changed by varying C1. The circuit operates well up to 500 Hz.

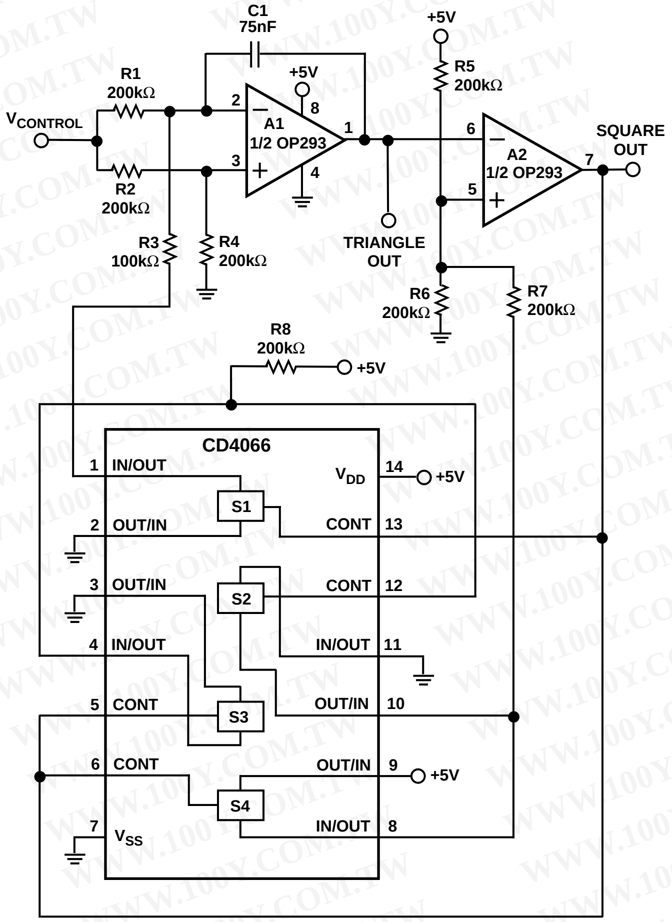


Figure 34. Micropower Voltage Controlled Oscillator

A Micropower, Single-Supply Quad Voltage Output 8-Bit DAC

The circuit of Figure 35 uses the DAC8408 CMOS quad 8-bit DAC and the OP493 to form a single-supply quad voltage output DAC with a supply drain of only 140 µA. The DAC8408 is used in the voltage switching mode and each DAC has an output resistance (≈10 kΩ) independent of the digital input code. The output amplifiers act as buffers to avoid loading the DACs. The 100 kΩ resistors ensure that the OP493 outputs will swing to within 1/2 LSB of ground, i.e.:

$$\frac{1}{2} \times \frac{1.23\ V}{256} = 3\ mV$$

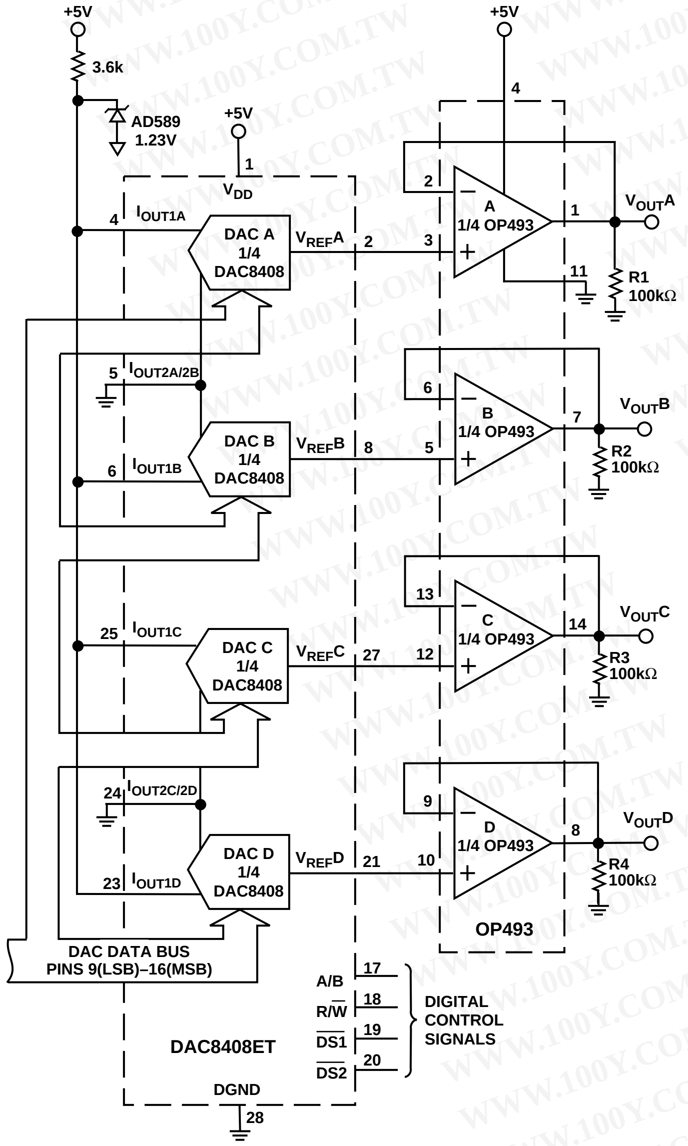


Figure 35. Micropower Single-Supply Quad Voltage-Output 8-Bit DAC

A Single-Supply Micropower Quad Programmable-Gain Amplifier

The combination of the quad OP493 and the DAC8408 quad 8-bit CMOS DAC creates a quad programmable gain amplifier with a quiescent supply drain of only 140 µA (Figure 36). The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the fixed DAC feedback resistor and the resistance that the DAC feedback ladder presents to the op amp feedback loop. The gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{256}{n}$$

where *n* equals the decimal equivalent of the 8-bit digital code present at the DAC.

If the digital code present at the DAC consists of all zeros, the feedback loop will be open causing the op amp to saturate. The 10 MΩ resistors placed in parallel with the DAC feedback loop eliminates this problem with a very small reduction in gain accuracy. The 2.5 V reference biases the amplifiers to the center of the linear region providing maximum output swing.

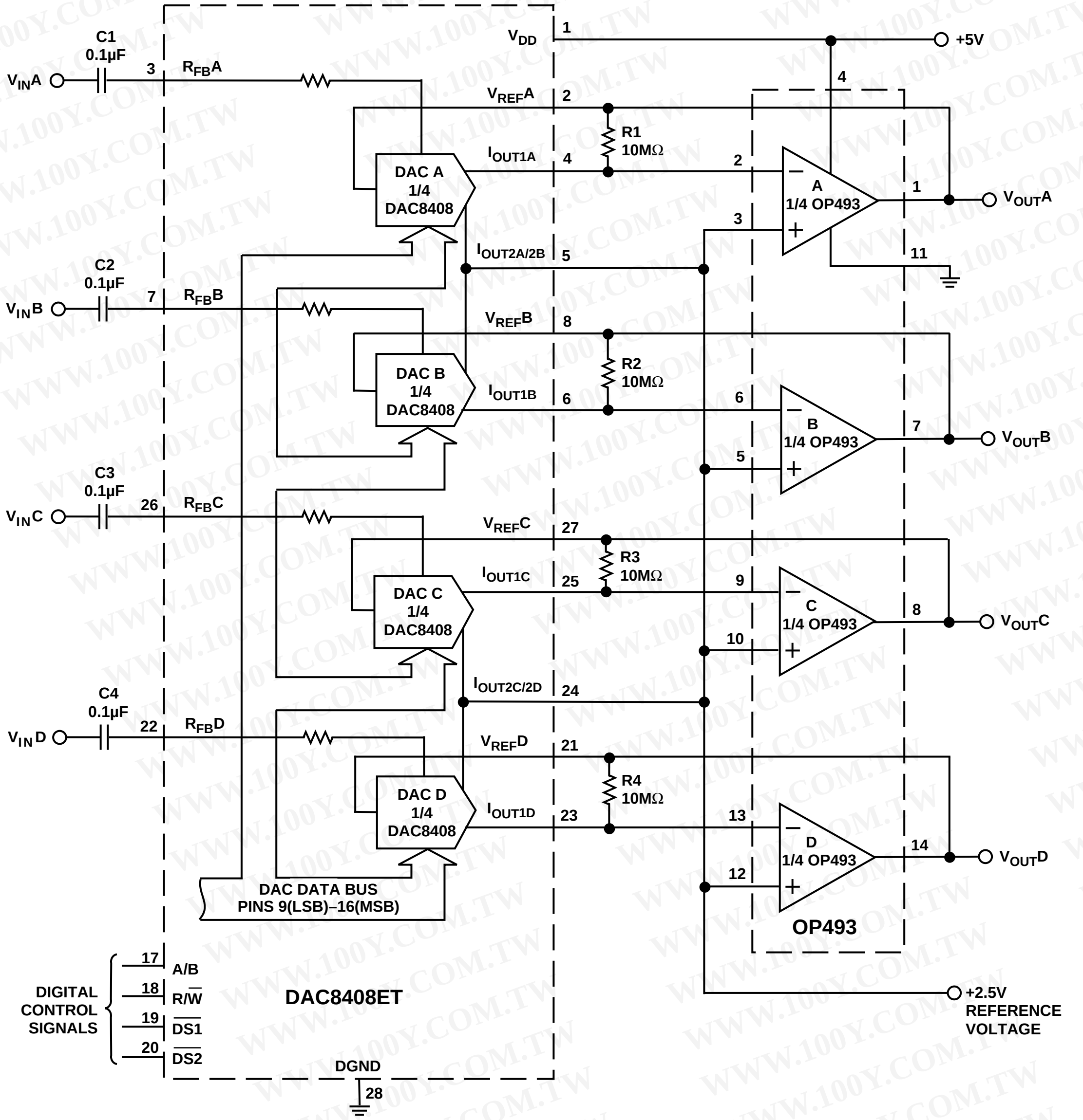
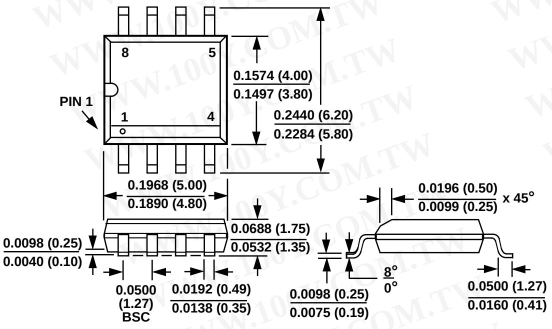


Figure 36. Single-Supply Micropower Quad Programmable-Gain Amplifier

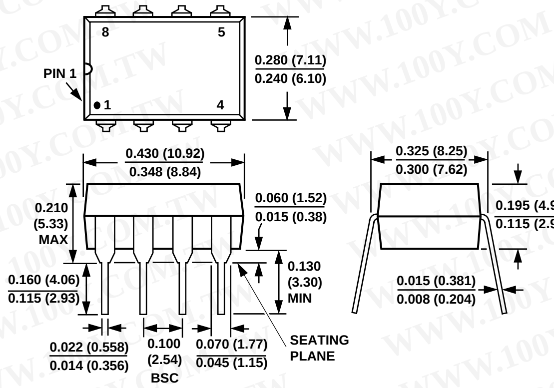
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

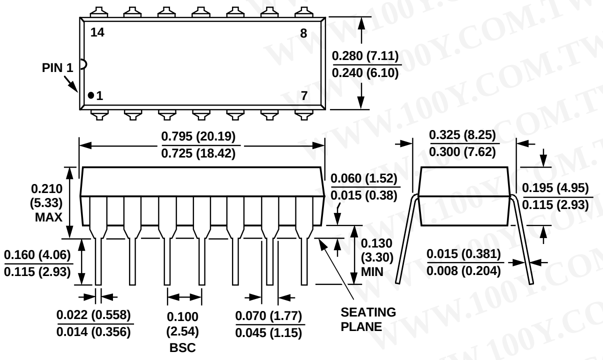
8-Lead SO (S Suffix)



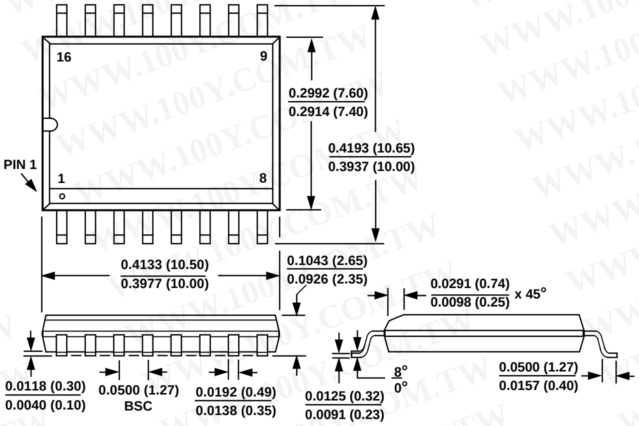
8-Lead Epoxy DIP (P Suffix)



14-Lead Epoxy DIP (P Suffix)



16-Lead Wide Body SOL (S Suffix)



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