National Semiconductor

December 1993

NM27C256
262,144-Bit (32K x 8) High Performance CMOS EPROM

General Description

The NM27C256 is a 256K Electrically Programmable Read Only Memory. It is manufactured in National's latest CMOS split gate EPROM technology which enables it to operate at speeds as fast as 120 ns access time over the full operating range.

The NM27C256 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 120 ns access time provides high speed operation with high-performance CPUs. The NM27C256 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

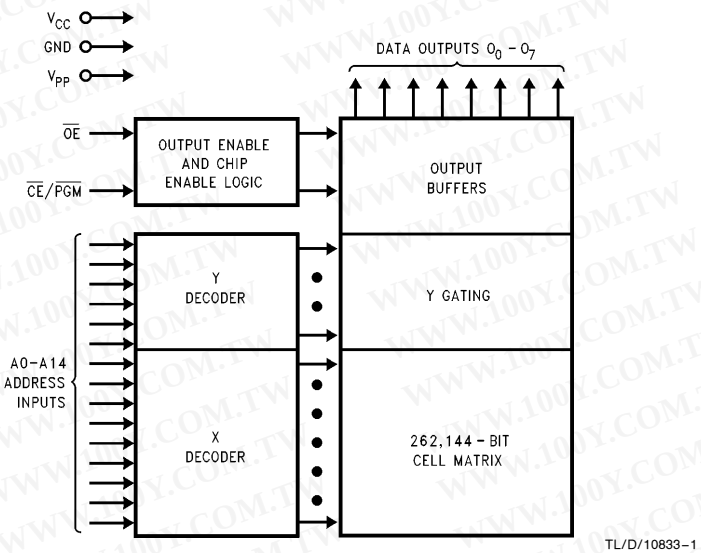
The NM27C256, is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C256 is one member of a high density EPROM Family which range in densities up to 4 Mb.

Features

- High performance CMOS
  - — 120 ns access time
- JEDEC standard pin configuration
  - — 28-pin DIP package
  - — 32-pin chip carrier
- Drop-in replacement for 27C256 or 27256
- Manufacturer's identification code

Block Diagram



TL/D/10833–1

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
HPC™ is a trademark of National Semiconductor Corporation.

 TL/D/10833

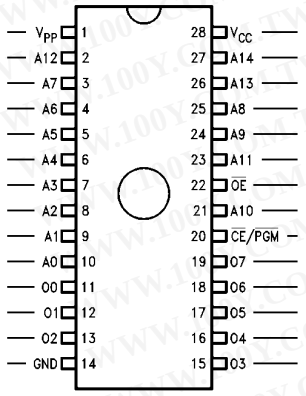
RRD-B30M65/Printed in U. S. A.

NM27C256 262,144-Bit (32K x 8) High Performance CMOS EPROM

Connection Diagrams

27C080	27C040	27C020	27C010	27C512
A19	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A16	A16	A16	A16	
A15	A15	A15	A15	A15
A12	A12	A12	A12	A12
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O0	O0	O0	O0	O0
O1	O1	O1	O1	O1
O2	O2	O2	O2	O2
GND	GND	GND	GND	GND

DIP
NM27C256



TL/D/10833–2

27C512	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/$\overline{PGM}$	XX/$\overline{PGM}$	A18	A18
V_{CC}	XX	A17	A17	A17
A14	A14	A14	A14	A14
A13	A13	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
A11	A11	A11	A11	A11
$\overline{OE}$/V_{PP}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/V_{PP}
A10	A10	A10	A10	A10
$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$/$\overline{PGM}$
O7	O7	O7	O7	O7
O6	O6	O6	O6	O6
O5	O5	O5	O5	O5
O4	O4	O4	O4	O4
O3	O3	O3	O3	O3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C256 pins.

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 Q, N, V 120	120
NM27C256 Q, N, V 150	150
NM27C256 Q, N, V 200	200

Military Temp. Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 QM 150	150
NM27C256 QM 250	250

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 QE, NE, VE 120	120
NM27C256 QE, NE, VE 150	150
NM27C256 QE, NE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

Package Types: NM27C256 Q, N, V XXX

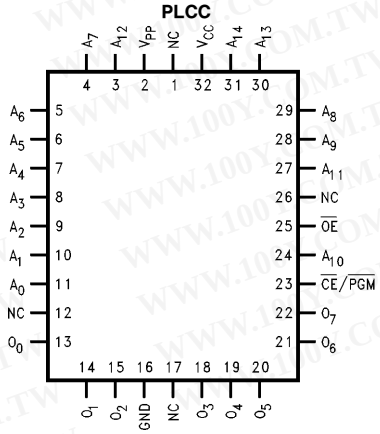
Q = Quartz-Windowed Ceramic DIP
N = Plastic OTP DIP
V = Surface-Mount PLCC

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Pin Names

Symbol	Description
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (during Read)

PLCC



Top

TL/D/10833–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	− 0.6V to +7V
ESD Protection	> 2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}
Comm'l	0°C to +70°C	+5V ±10%
Industrial	−40°C to +85°C	+5V ±10%
Military	−55°C to +125°C	+5V ±10%

Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA	3.5		V
I_{SB1} (Note 11)	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$		100	μA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$		1	mA
I_{CC1}	V_{CC} Active Current TTL Inputs	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	μA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	μA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	100		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		30		35		45		55	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

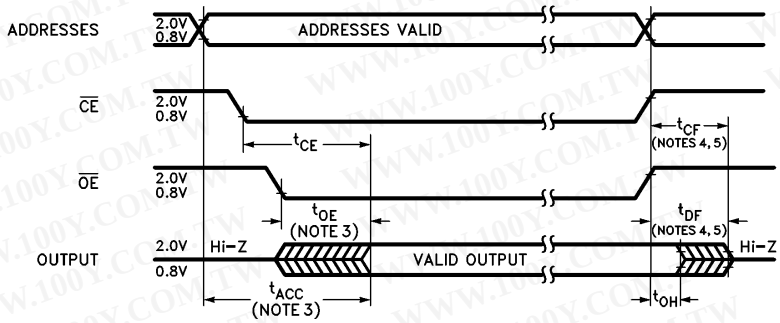
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45 to 2.4V
Timing Measurement Reference Level	(Note 10)
Inputs	0.8V and 2.0V
Outputs	0.8V and 2.0V

AC Waveforms (Notes 6, 7 and 9)



TL/D/10833–4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
C_L = 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

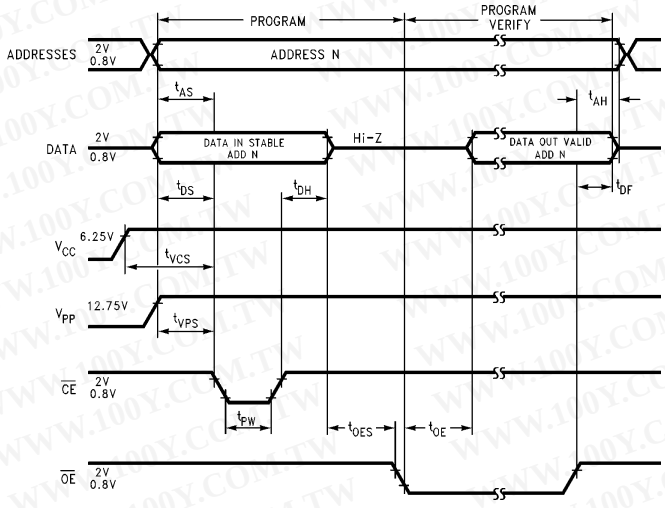
Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: CMOS inputs: V_{IL} = GND ±0.3V, V_{IH} = V_{CC} ±0.3V.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



TL/D/10833–5

Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

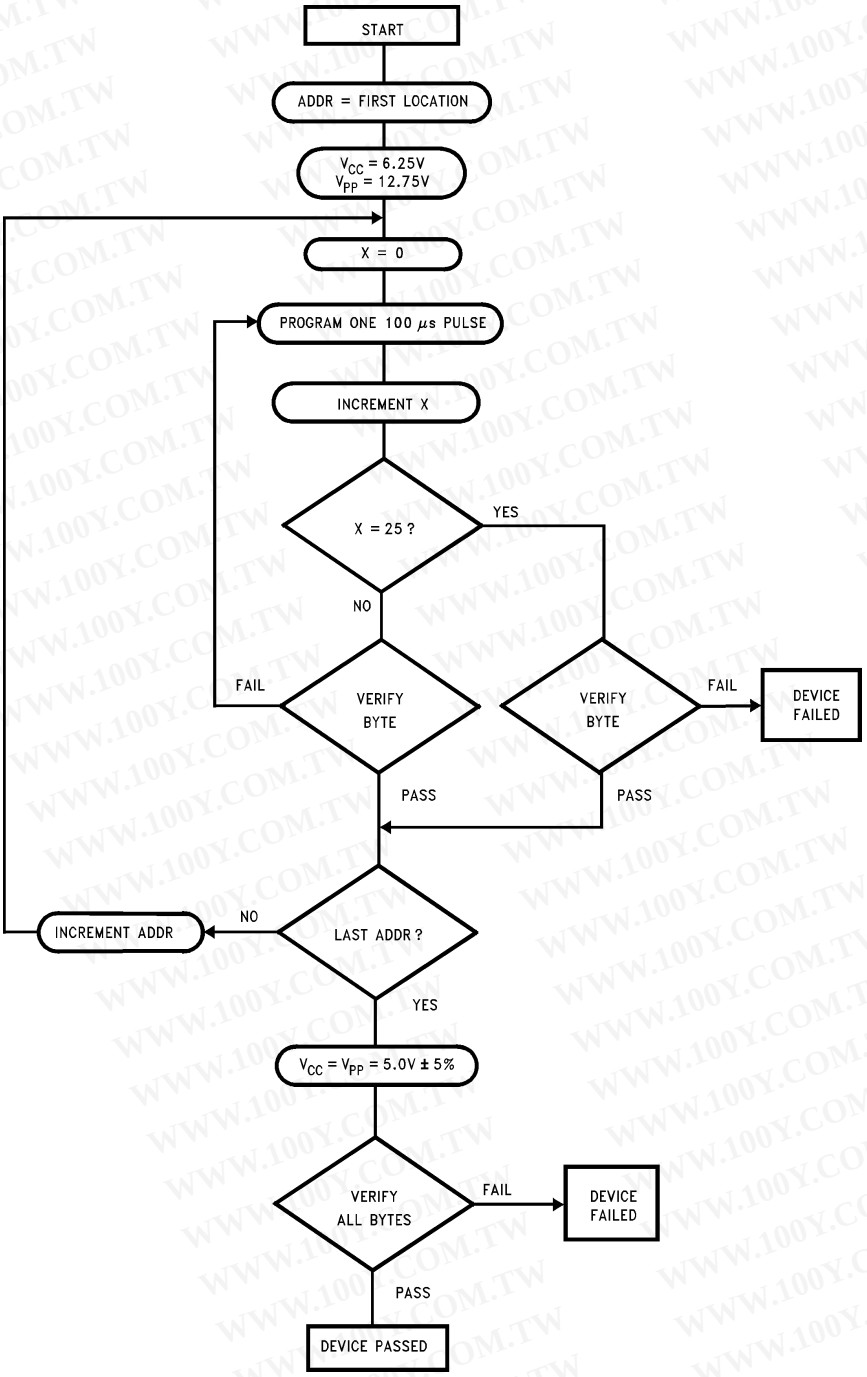
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/10833–6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE/PGM has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the ''1's'' state. Data is introduced by selectively programming ''0's'' into the desired bit locations. Although only ''0's'' will be programmed, both ''1's'' and ''0's'' can be presented in the data word. The only way to change a ''0'' to a ''1'' is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and OE is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirments. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM, all like inputs (including OE) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27C256 is ''8F04'', where ''8F'' designates that it is made by National Semiconductor, and ''04'' designates a 256K part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C to $\pm$5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of NM27C256 listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

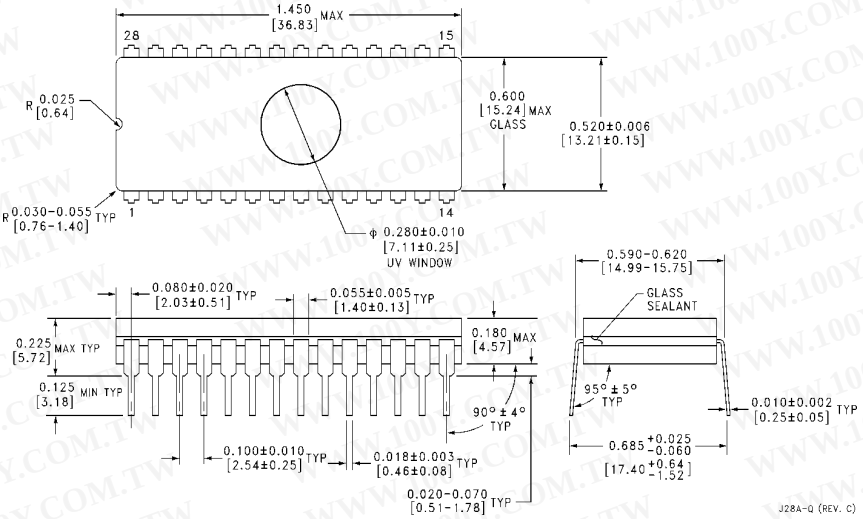
Mode \ Pins	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	V_{CC}	5.0V	High-Z
Standby	V_{IH}	X	V_{CC}	5.0V	High-Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High-Z

Note 1: X can be V_{IL} or V_{IH}.

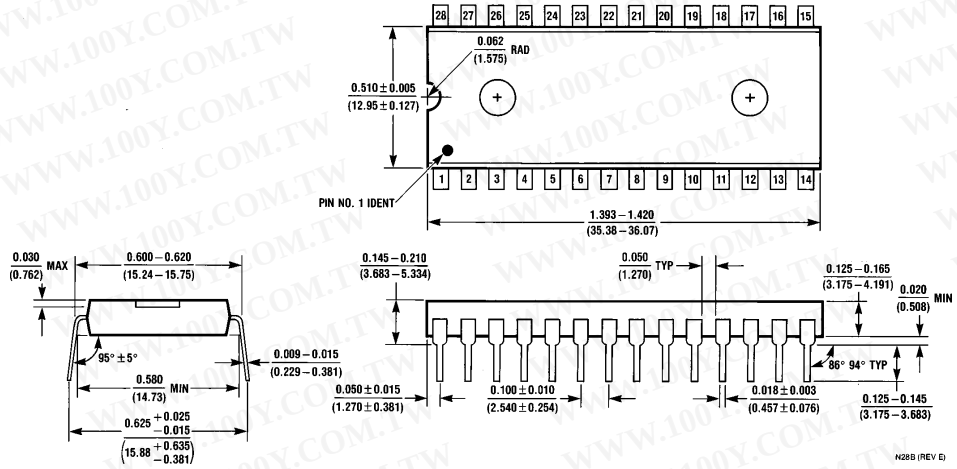
TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	0	1	0	0	04

Physical Dimensions inches (millimeters)

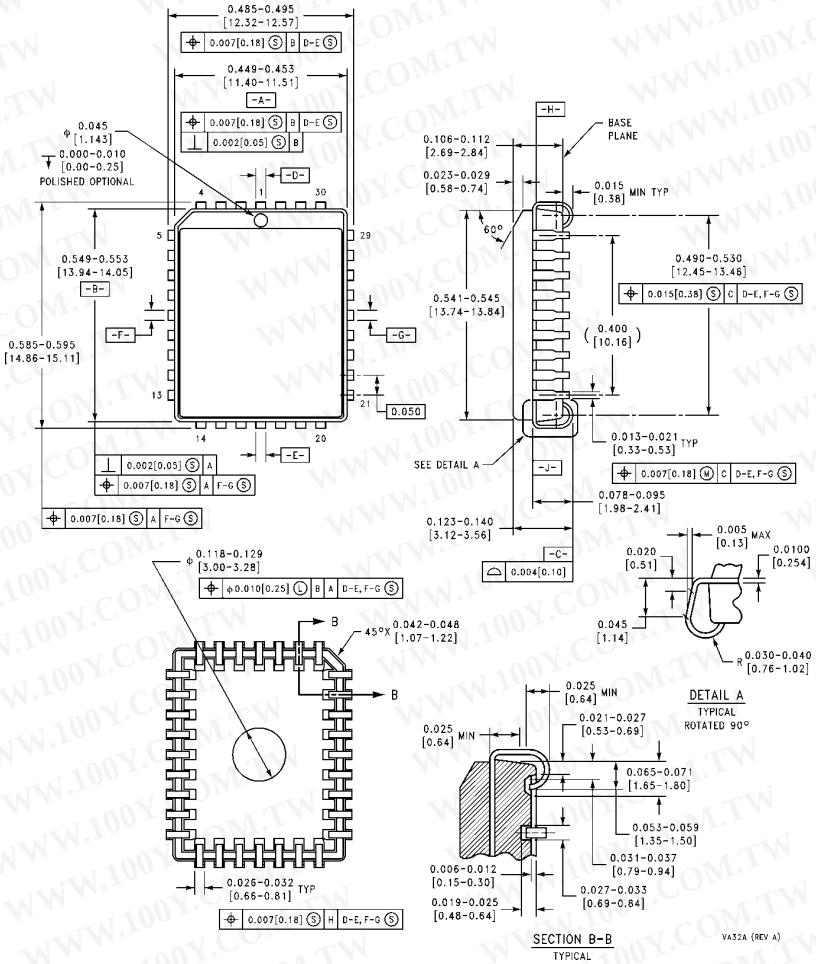


UV Window Cavity Dual-In-Line CerDIP Package (Q)
Order Number NM27C256QXXX
NS Package Number J28AQ



28-Lead Plastic One-Time-Programmable Dual-In-Line Package
OrderNumber NM27C256NXXX
NS Package Number N28B

Physical Dimensions inches (millimeters) (Continued)



32-Lead Plastic Leaded Chip Carrier (PLCC)
Order Number NM27C256VXXX
NS Package Number VA32A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.