MX29F040

4M-BIT [512KX8] CMOS EQUAL SECTOR FLASH MEMORY

FEATURES

- 524,288 x 8 only
- Single power supply operation
  - 5.0V only operation for read, erase and program operation
- Fast access time: 55/70/90/120ns
- Low power consumption
  - 30mA maximum active current(5MHz)
  - 1uA typical standby current
- Command register architecture
  - Byte Programming (7us typical)
  - Sector Erase
  8 equal sectors of 64K-Byte each
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Erase suspend/Erase Resume
  - Suspends an erase operation to read data from, or program data to, another sector that is not being erased, then resumes the erase.
- Status Reply
  - Data polling & Toggle bit for detection of program and erase cycle completion.
- Sector protect/unprotect for 5V only system or 5V/12V system.
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 32-pin PLCC, TSOP or PDIP
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash
- 20 years data retention

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

GENERAL DESCRIPTION

The MX29F040 is a 4-mega bit Flash memory organized as 512K bytes of 8 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F040 is packaged in 32-pin PLCC, TSOP, PDIP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29F040 offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F040 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

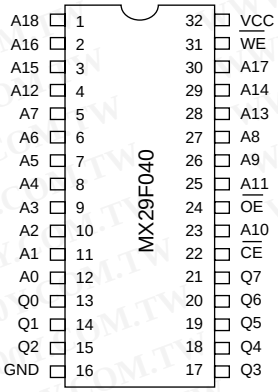
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F040 uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F040 uses a 5.0V±10% VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

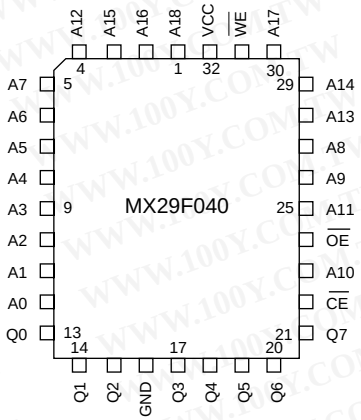
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

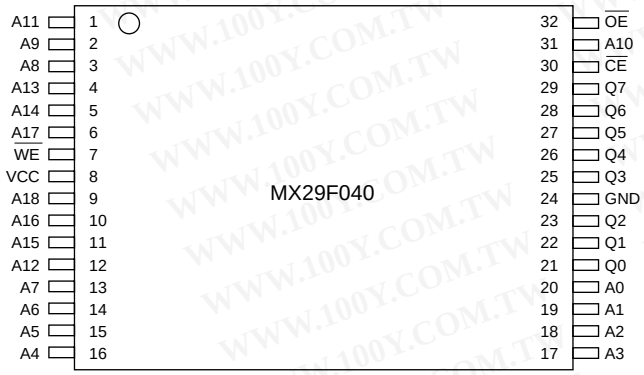
32 PDIP



32 PLCC



32 TSOP (Standard Type) (8mm x 20mm)



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
GND	Ground Pin
VCC	+5.0V single power supply

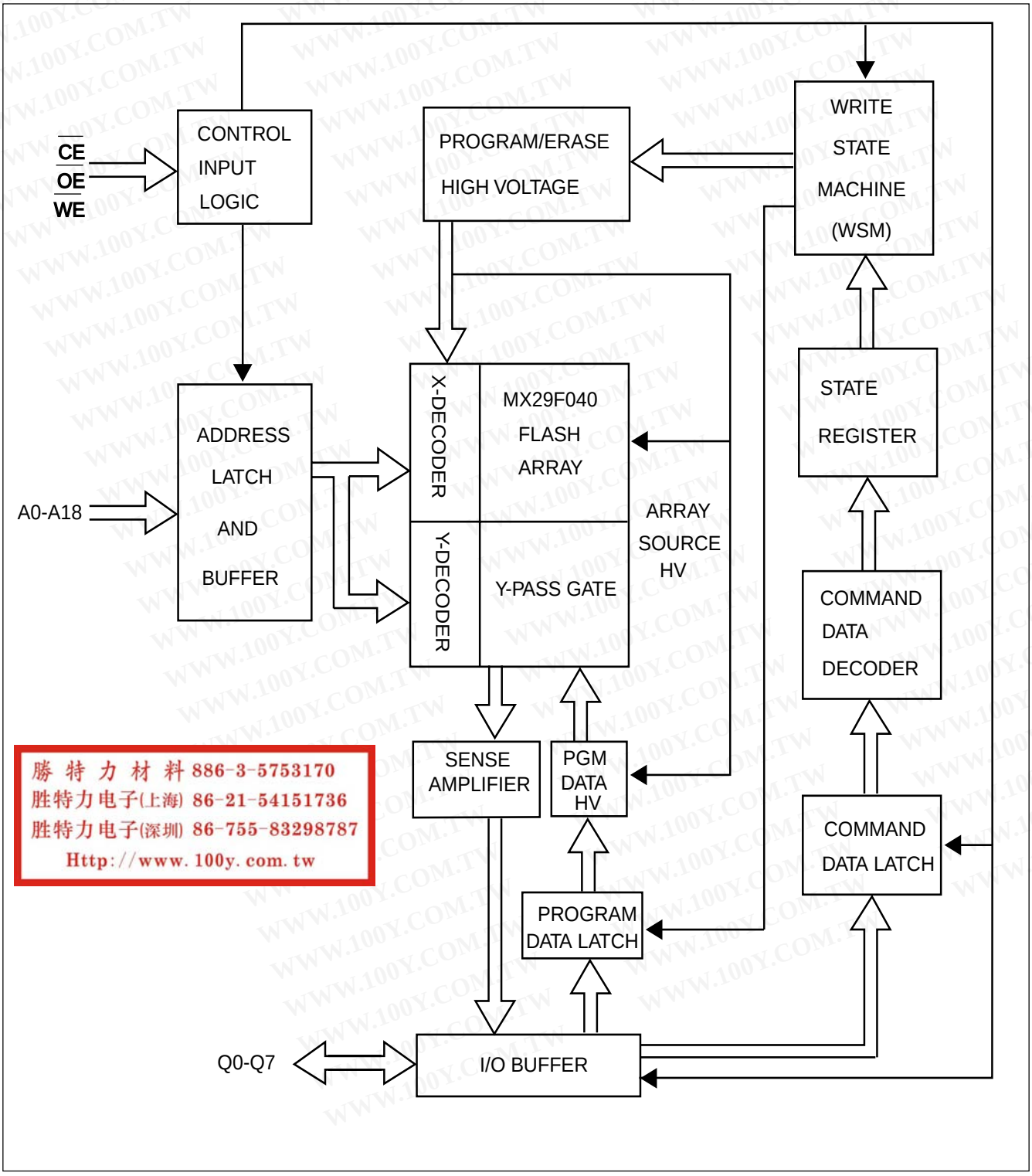
SECTOR STRUCTURE

MX29F040 SECTOR ADDRESS TABLE

Sector	A18	A17	A16	Address Range
SA0	0	0	0	00000h-0FFFFh
SA1	0	0	1	10000h-1FFFFh
SA2	0	1	0	20000h-2FFFFh
SA3	0	1	1	30000h-3FFFFh
SA4	1	0	0	40000h-4FFFFh
SA5	1	0	1	50000h-5FFFFh
SA6	1	1	0	60000h-6FFFFh
SA7	1	1	1	70000h-7FFFFh

Note:All sectors are 64 Kbytes in size.

BLOCK DIAGRAM



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

AUTOMATIC PROGRAMMING

The MX29F040 is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29F040 is less than 4 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 4 second. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29F040 is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm require the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to $\overline{\text{DATA}}$ polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever happeds later, and data are latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever happeds first.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F040 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

TABLE1. SOFTWARE COMMAND DEFINITIONS

Command	Bus Cycle	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXXH	F0H										
Read	1	RA	RD										
Read Silicon ID	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
Sector Protect Verify	4	555H	AAH	2AAH	55H	555H	90H	(SA)X 02	00H 01H				
Porgram	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend	1	XXXH	B0H										
Sector Erase Resume	1	XXXH	30H										
Unlock for sector protect/unprotect	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	20H

Note:
1. ADI = Address of Device identifier; A1=0, A0 = 0 for manufacture code,A1=0, A0 = 1 for device code A2-A18=Do not care.
(Refer to table 3)
DDI = Data of Device identifier : C2H for manufacture code, A4H for device code.
X = X can be VIL or VIH
RA=Address of memory location to be read.
RD=Data to be read at location RA.
2.PA = Address of memory location to be programmed.
PD = Data to be programmed at location PA.
SA = Address to the sector to be erased.
3.The system should generate the following address patterns: 555H or 2AAH to Address A10~A0 .
Address bit A11~A18=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequence may be initiated with A11~A18 in either state.
4.For Sector Protect Verify Operation : If read out data is 01H, it means the sector has been protected.If read out data is 00H,it means the sector is still not being protected.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 1 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device(when applicable).

TABLE 2. MX29F040 BUS OPERATION

Mode	Pins							
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	Q0 ~ Q7
Read Silicon ID Manfacturer Code(1)	L	L	H	L	L	X	V_{ID}(2)	C2H
Read Silicon ID Device Code(1)	L	L	H	H	L	X	V_{ID}(2)	A4H
Read	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D_{IN}(3)
Sector Protect with 12V system(6)	L	V_{ID}(2)	L	X	X	L	V_{ID}(2)	X
Chip Unprotect with 12V system(6)	L	V_{ID}(2)	L	X	X	H	V_{ID}(2)	X
Verify Sector Protect with 12V system	L	L	H	X	H	X	V_{ID}(2)	Code(5)
Sector Protect without 12V system (6)	L	H	L	X	X	L	H	X
Chip Unprotect without 12V system (6)	L	H	L	X	X	H	H	X
Verify Sector Protect/Unprotect without 12V system (7)	L	L	H	X	H	X	H	Code(5)
Reset	X	X	X	X	X	X	X	HIGH Z

NOTES:

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H means unprotected.
   Code=01H means protected.
   A18~A16=Sector address for sector protect.
6. Refer to sector protect/unprotect algorithm and waveform.
   Must issue "unlock for sector protect/unprotect" command before "sector protect/unprotect without 12V system" command.
7. The "verify sector protect/unprotect without 12V sysytem" is only following "Sector protect/unprotect without 12V system" command.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F040 contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL,A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of A4H for MX29F040.

SET-UP AUTOMATIC CHIP/SECTOR ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verification command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$, whichever happeds first pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

TABLE 3. EXPANDED SILICON ID CODE

Pins	A0	A1	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	VIL	VIL	1	1	0	0	0	0	1	0	C2H
Device code for MX29F040	VIH	VIL	1	0	1	0	0	1	0	0	A4H
Sector Protection Verification	X	VIH	0	0	0	0	0	0	0	1	01H(Protected)
	X	VIH	0	0	0	0	0	0	0	0	00H(Unprotected)

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happeds later, while the command(data) is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happeds first. Sector addresses selected are loaded into internal register on the sixth falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happeds later. Each successive sector load cycle started by the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happeds later must begin within 30us from the rising edge of the preceding $\overline{WE}$ or $\overline{CE}$, whichever happeds first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Table 4. Write Operation Status

	Status		Q7 Note1	Q6	Q5 Note2	Q3	Q2
In Progress	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	N/A	No Toggle
	Auto Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program	$\overline{Q7}$	Toggle	0	N/A	N/A
Exceeded Time Limits	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	N/A	No Toggle
	Auto Erase Algorithm		0	Toggle	1	1	Toggle
	Erase Suspend Program		$\overline{Q7}$	Toggle	1	N/A	N/A

Note:
1. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. Q5 switches to '1' when an Auto Program or Auto Erase operation has exceeded the maximum timing limits. See "Q5:Exceeded Timing Limits " for more information.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 100us to suspend the erase operations. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and program commands.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended sectors.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions.Another Erase Suspend command can be written after the chip has resumed erasing.

SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next $\overline{WE}$ or $\overline{CE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the $\overline{WE}$ or $\overline{CE}$, whichever happeds first pulse. The rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happeds first also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program opetation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode(no program verify command is required).

$\overline{DATA}$ POLLING-Q7

The MX29F040 also features $\overline{Data}$ Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The $\overline{Data}$ Polling feature is valid after the rising edge of the fourth $\overline{WE}$ or $\overline{CE}$, whichever happeds first pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1". The $\overline{Data}$ Polling feature is valid after the rising edge of the sixth $\overline{WE}$ or $\overline{CE}$, whichever happeds first pulse of six write pulse sequences for automatic chip/ sector erase.

The $\overline{Data}$ Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out.(see section Q3 Sector Erase Timer)

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE or CE, whichever happeds first pulse in the command sequence(prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE or CE to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 4 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively eraseing (that is, the Automatic Erase alorithm is in process), or whether that sector is erase-suspended. Toggle Bit I is valid after the rising edge of the final WE or CE, whichever happeds first pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE or CE to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 4 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfuly completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits(internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector maynot be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

DATA PROTECTION

The MX29F040 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

Q3
Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

SECTOR PROTECTION WITH 12V SYSTEM

The MX29F040 features sector protection. This feature will disable both program and erase operations for these sectors protected. To activate this mode, the programming equipment must force VID on address pin A9 and control pin $\overline{OE}$, (suggest VID = 12V) A6 = VIL and $\overline{CE}$ = VIL.(see Table 2) Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ or $\overline{CE}$, whichever happeds later pulse and is terminated on the rising edge. Please refer to sector protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with $\overline{CE}$ and $\overline{OE}$ at VIL and $\overline{WE}$ at VIH). When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses, except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes.(Read Silicon ID)

It is also possible to determine if the sector is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT WITH 12V SYSTEM

The MX29F040 also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin OE and address pin A9. The CE pins must be set at VIL. Pins A6 must be set to VIH.(see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ or $\overline{CE}$, whichever happeds later, pulse and is terminated on the rising edge.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs(Q0-Q7) for an unprotected sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

POWER-UP SEQUENCE

The MX29F040 powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

SECTOR PROTECTION WITHOUT 12V SYSTEM

The MX29F040 also feature a sector protection method in a system without 12V power suppply. The programming equipment do not need to supply 12 volts to protect sectors. The details are shown in sector protect algorithm and waveform.

CHIP UNPROTECT WITHOUT 12V SYSTEM

The MX29F040 also feature a chip unprotection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to unprotect all sectors. The details are shown in chip unprotect algorithm and waveform.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

CAPACITANCE (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			8	pF	VIN = 0V
CIN2	Control Pin Capacitance			12	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

READ OPERATION

DC CHARACTERISTICS (TA = 0°C TO 70°C, VCC = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN = GND to VCC
ILO	Output Leakage Current			10	uA	VOUT = GND to VCC
ISB1	Standby VCC current			1	mA	$\overline{CE}$ = VIH
ISB2			1	5	uA	$\overline{CE}$ = VCC + 0.3V
ICC1	Operating VCC current			30	mA	IOUT = 0mA, f=5MHz
ICC2				50	mA	IOUT = 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(NOTE 1)		0.8	V	
VIH	Input High Voltage	2.0		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH1	Output High Voltage(TTL)	2.4			V	IOH = -2mA
VOH2	Output High Voltage(CMOS)	VCC-0.4			V	IOH = -100uA,VCC=VCC MIN

NOTES:

1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns.
   If VIH is over the specified maximum value, read operation cannot be guaranteed.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

AC CHARACTERISTICS (TA = 0°C to 70°C, VCC = 5V±10%)

		29F040-55(note2)		29F040-70		29F040-90		29F040-12			
Symbol	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit	Conditions
tACC	Address to Output Delay		55		70		90		120	ns	CE=OE=VIL
tCE	CE to Output Delay		55		70		90		120	ns	$\overline{OE}$=VIL
tOE	OE to Output Delay		30		40		40		50	ns	$\overline{CE}$=VIL
tDF	OE High to Output Float (Note1)	0	30	0	30	0	40	0	40	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times is equal to or less than 0ns
- Output load: 1 TTL gate + 100pF (Including scope and jig)
- Reference levels for measuring timing: 0.8V, 2.0V

NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Under condition of VCC=5V±10%,CL=50pF,VIH/VIL=3.0/0V,VOH/VOL=1.5/1.5V,IOL=2mA,IOH=-2mA.

ABSOLUTE MAXIMUM RATINGS

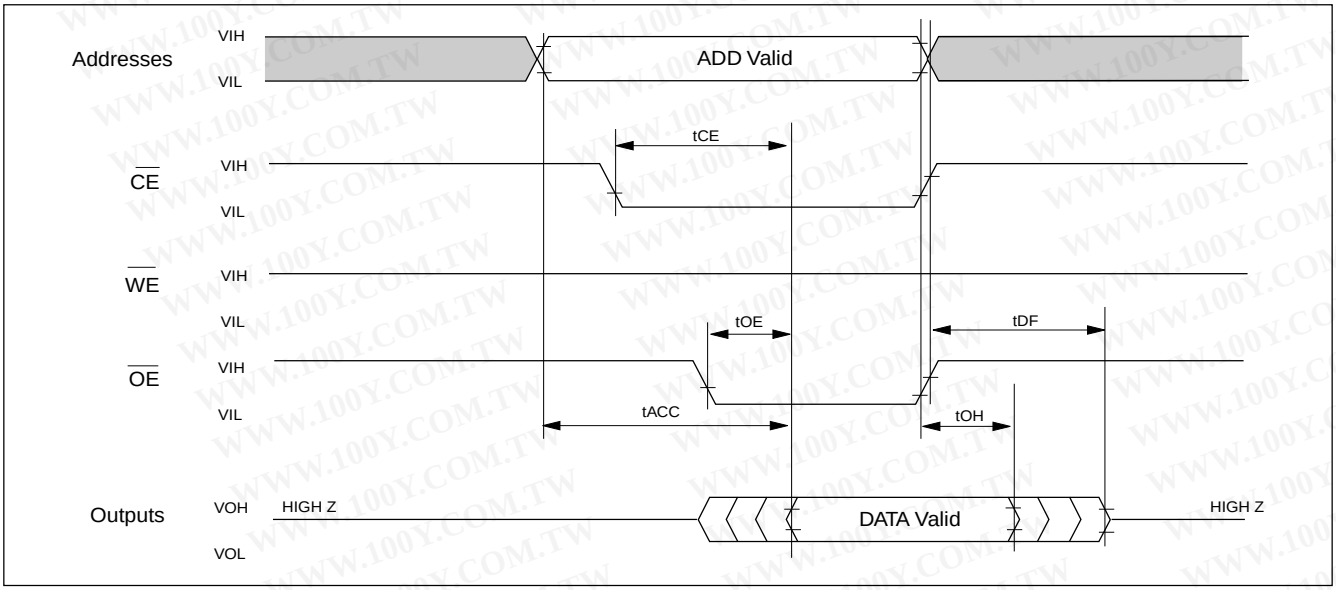
RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Ambient Temperature with Power Applied	-55°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9 & $\overline{OE}$	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

READ TIMING WAVEFORMS



COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

DC CHARACTERISTICS (TA = 0°C to 70°C, VCC = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ICC1 (Read)	Operating VCC Current			30	mA	IOUT=0mA, f=5MHz
ICC2				50	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	$\overline{CE}$=VIH, Erase Suspended

NOTES:

1. VIL min. = -0.6V for pulse width is equal to or less than 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.

AC CHARACTERISTICS TA = 0ºC to 70ºC, VCC = 5V ± 10%

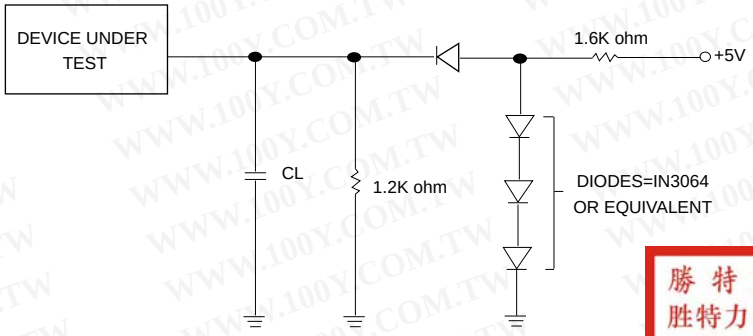
		29F040-55(Note2)		29F040-70		29F040-90		29F040-12		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit
tOES	$\overline{OE}$ setup time	50		50		50		50		ns
tCWC	Command programming cycle	70		70		90		120		ns
tCEP	$\overline{WE}$ programming pulse width	45		45		45		50		ns
tCEPH1	$\overline{WE}$ programming pluse width High	20		20		20		20		ns
tCEPH2	$\overline{WE}$ programming pluse width High	20		20		20		20		ns
tAS	Address setup time	0		0		0		0		ns
tAH	Address hold time	45		45		45		50		ns
tDS	Data setup time	30		30		45		50		ns
tDH	Data hold time	0		0		0		0		ns
tCESC	$\overline{CE}$ setup time before command write	0		0		0		0		ns
tDF	Output disable time (Note 1)		30		30		40		40	ns
tAETC	Total erase time in auto chip erase	4(TYP.)	32	4(TYP.)	32	4(TYP.)	32	4(TYP.)	32	s
tAETB	Total erase time in auto sector erase	1.3(TYP.)	10.4	1.3(TYP.)	10.4	1.3(TYP.)	10.4	1.3(TYP.)	10.4	s
tAVT	Total programming time in auto verify	7	210	7	210	7	210	7	210	us
tBAL	Sector address load time	100		100		100		100		us
tCH	$\overline{CE}$ Hold Time	0		0		0		0		ns
tCS	$\overline{CE}$ setup to WE going low	0		0		0		0		ns
tVLHT	Voltge Transition Time	4		4		4		4		us
tOESP	$\overline{OE}$ Setup Time to $\overline{WE}$ Active	4		4		4		4		us
tWPP1	Write pulse width for sector protect	10		10		10		10		us
tWPP2	Write pulse width for sector unprotect	12		12		12		12		ms

NOTES:

1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Under conditions of VCC=5V±10%,CL=50pF,VIH/VIL=3.0/0V,VOL/VOH=1.5/1.5, IOL=2mA,IOH=-2mA.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

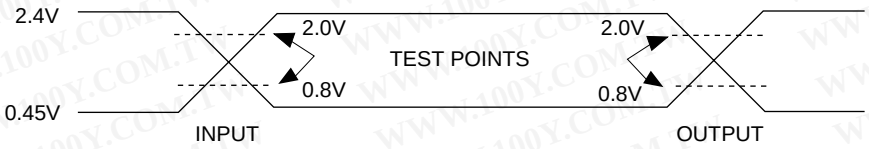
SWITCHING TEST CIRCUITS



CL=100pF Including jig capacitance
CL= 50pF for 29F040-55

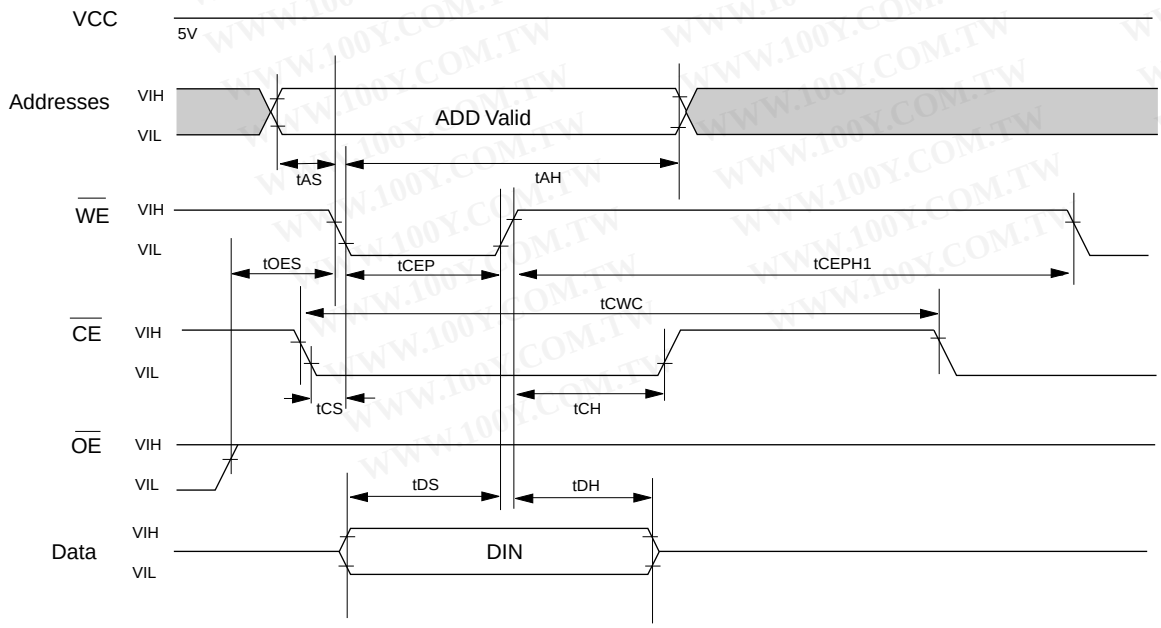
勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are < 20ns.(5ns for 29F040-55)
Note:VIH/VIL=3.0/0V,VOH/VOL=1.5/1.5V for 29F040-55

COMMAND WRITE TIMING WAVEFORM

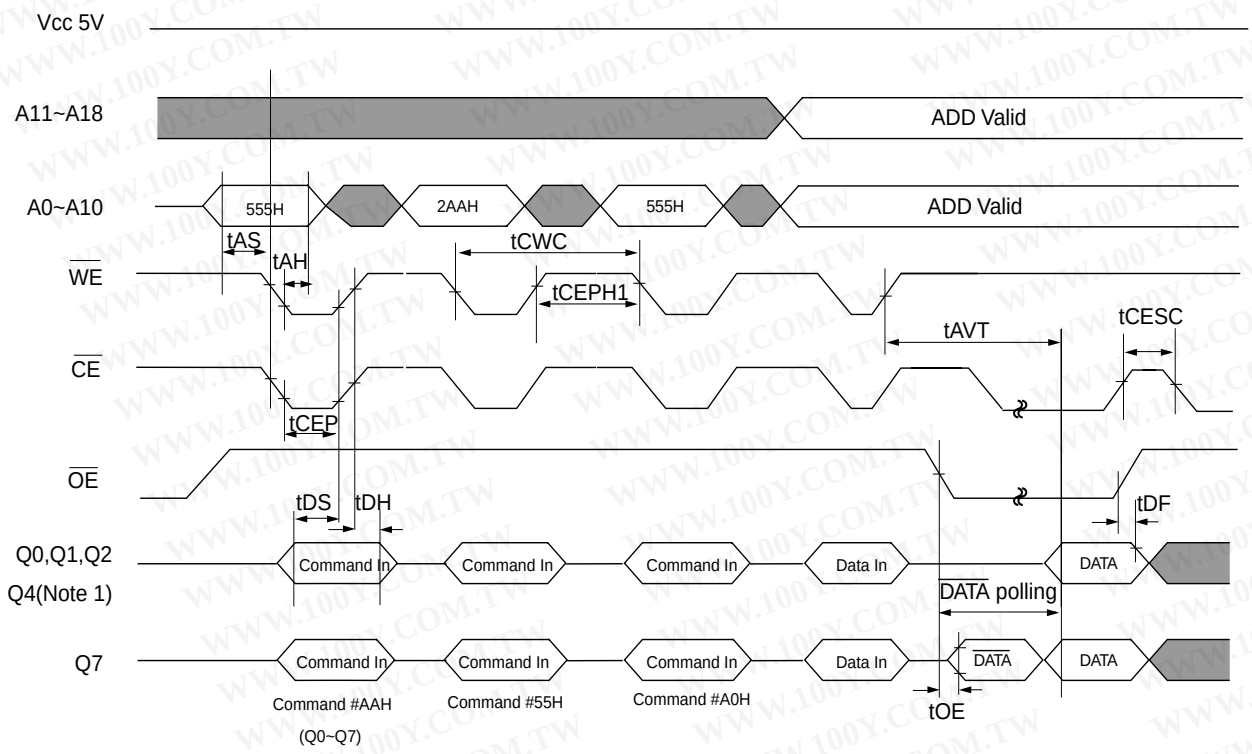


AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic verification starts. Device outputs $\overline{DATA}$ during programming and $\overline{DATA}$ after programming on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

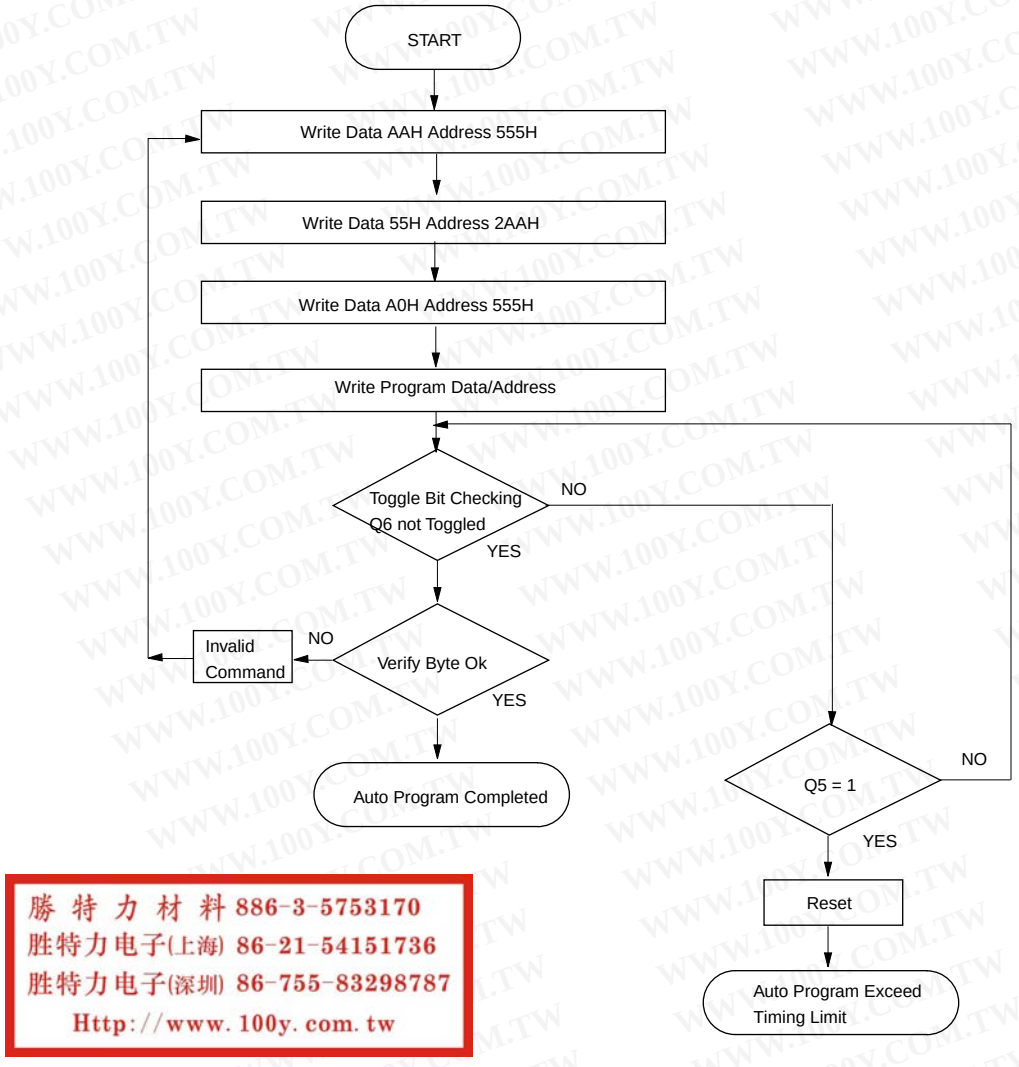
AUTOMATIC PROGRAMMING TIMING WAVEFORM



Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit

AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

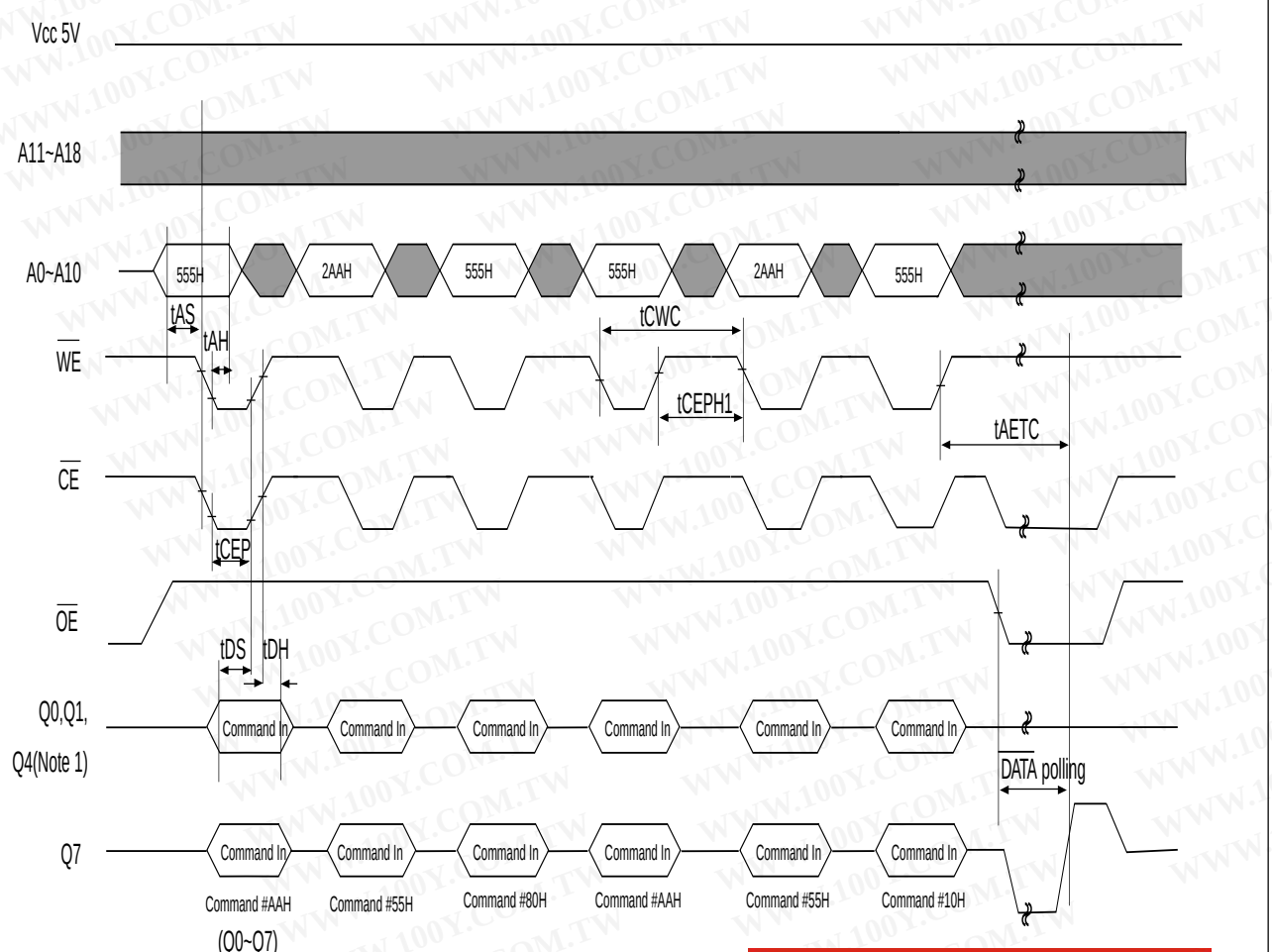


勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verification is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

AUTOMATIC CHIP ERASE TIMING WAVEFORM

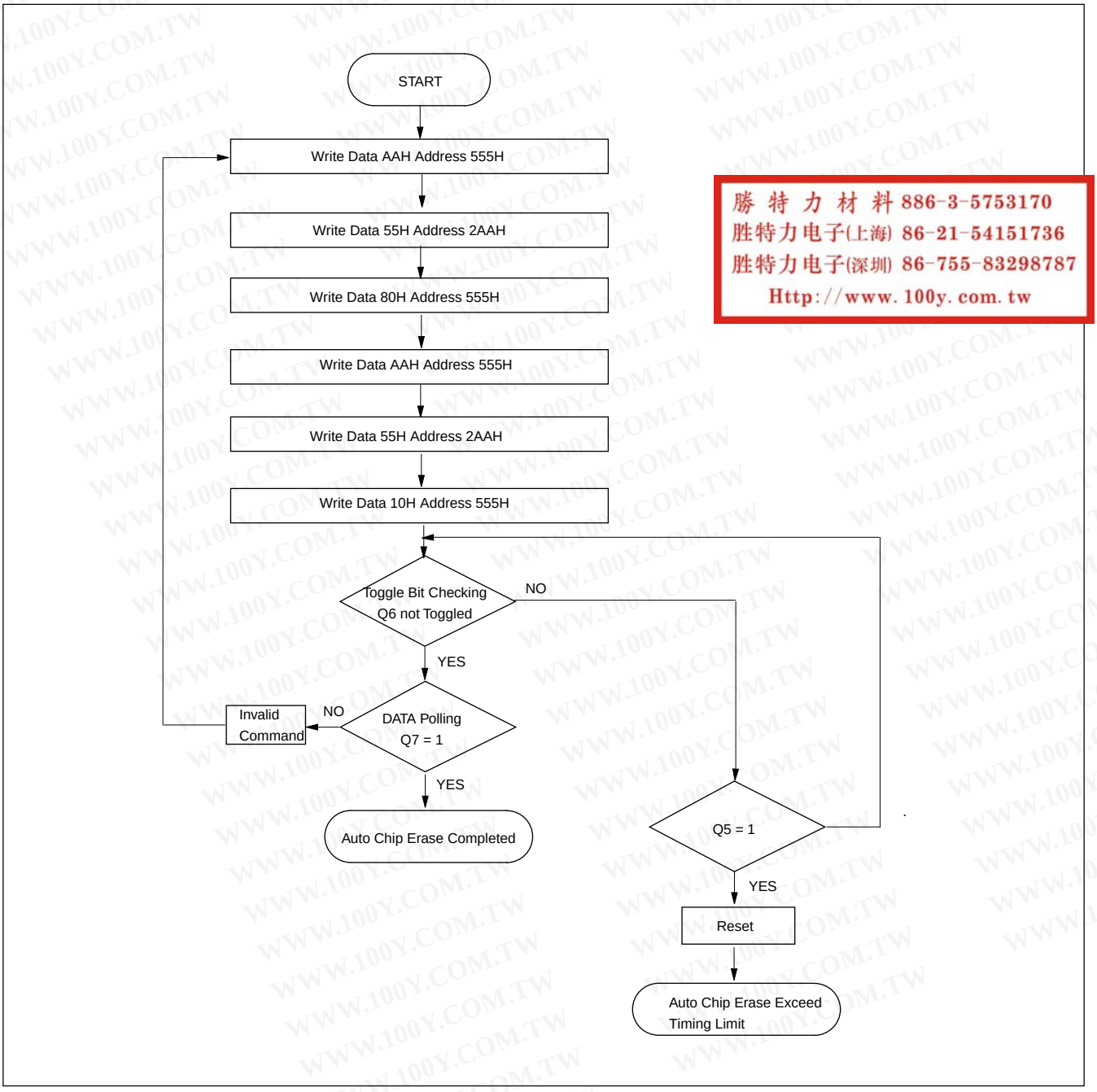


Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

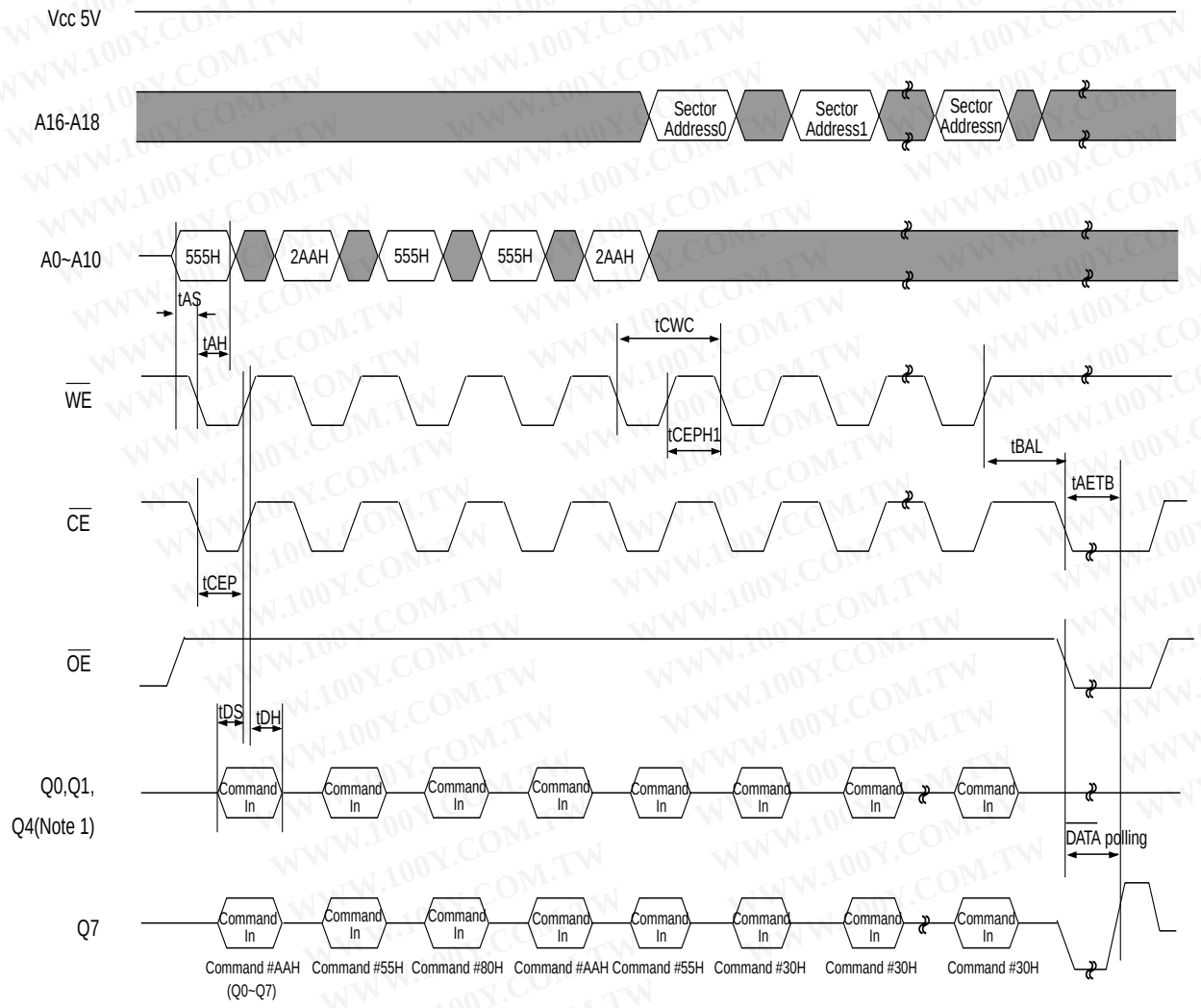


勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Sector data indicated by A16 to A18 are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by $\overline{\text{DATA}}$ polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{\text{DATA}}$ polling, timing waveform)

AUTOMATIC SECTOR ERASE TIMING WAVEFORM

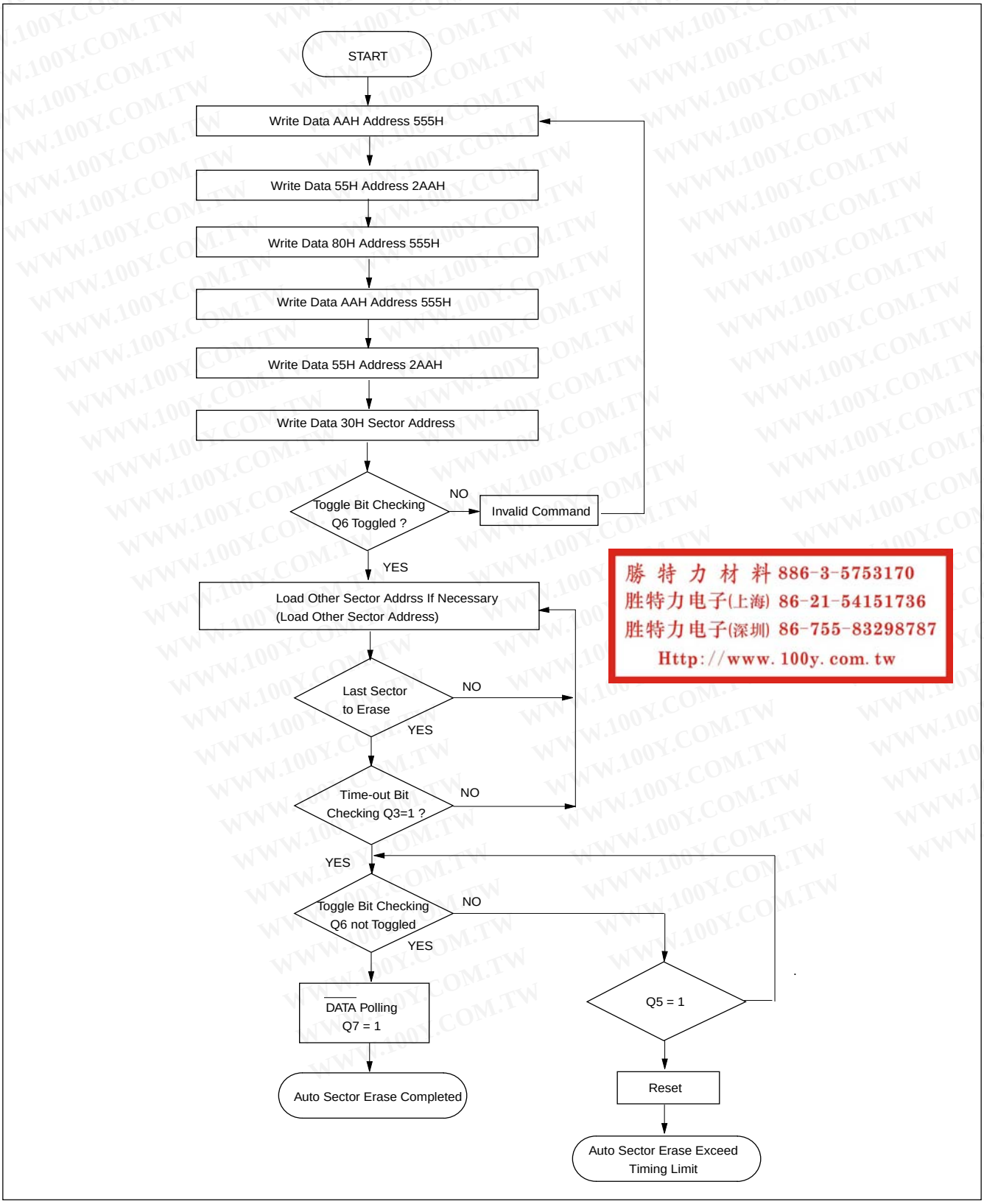


Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

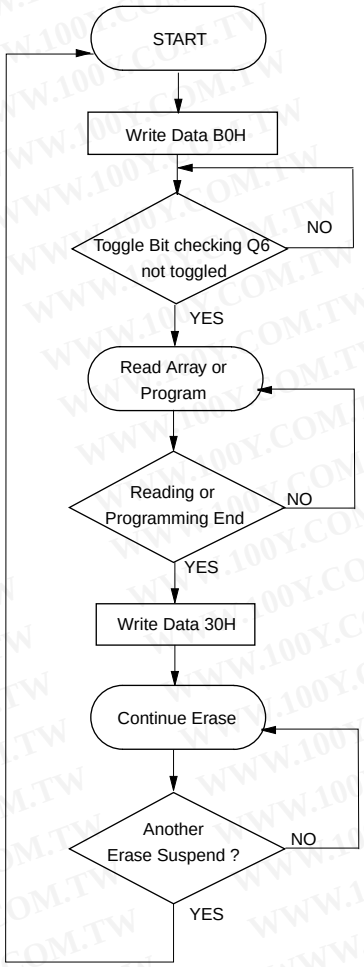
勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART



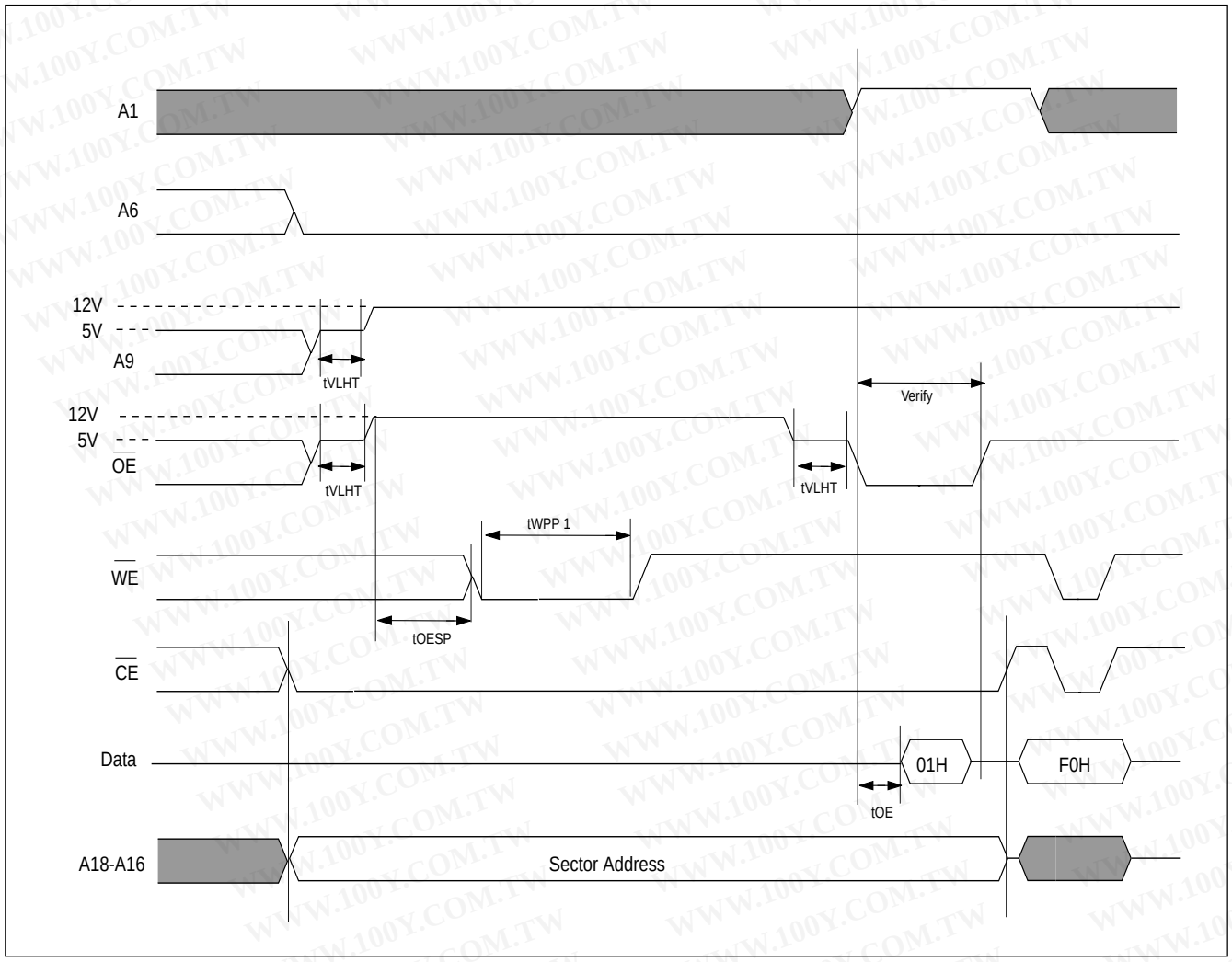
勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

ERASE SUSPEND/ERASE RESUME FLOWCHART



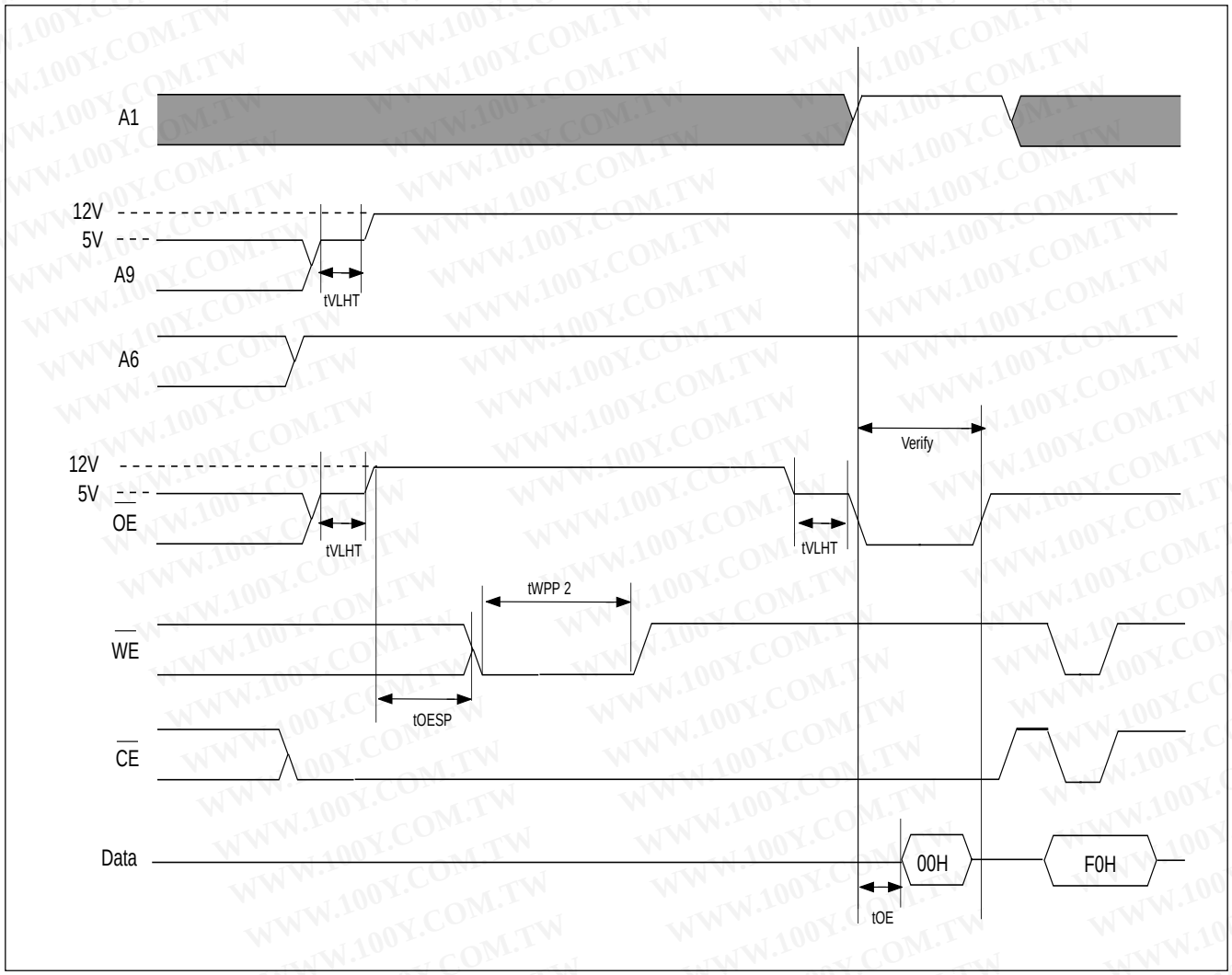
勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

TIMING WAVEFORM FOR SECTOR PROTECTION FOR SYSTEM WITH 12V



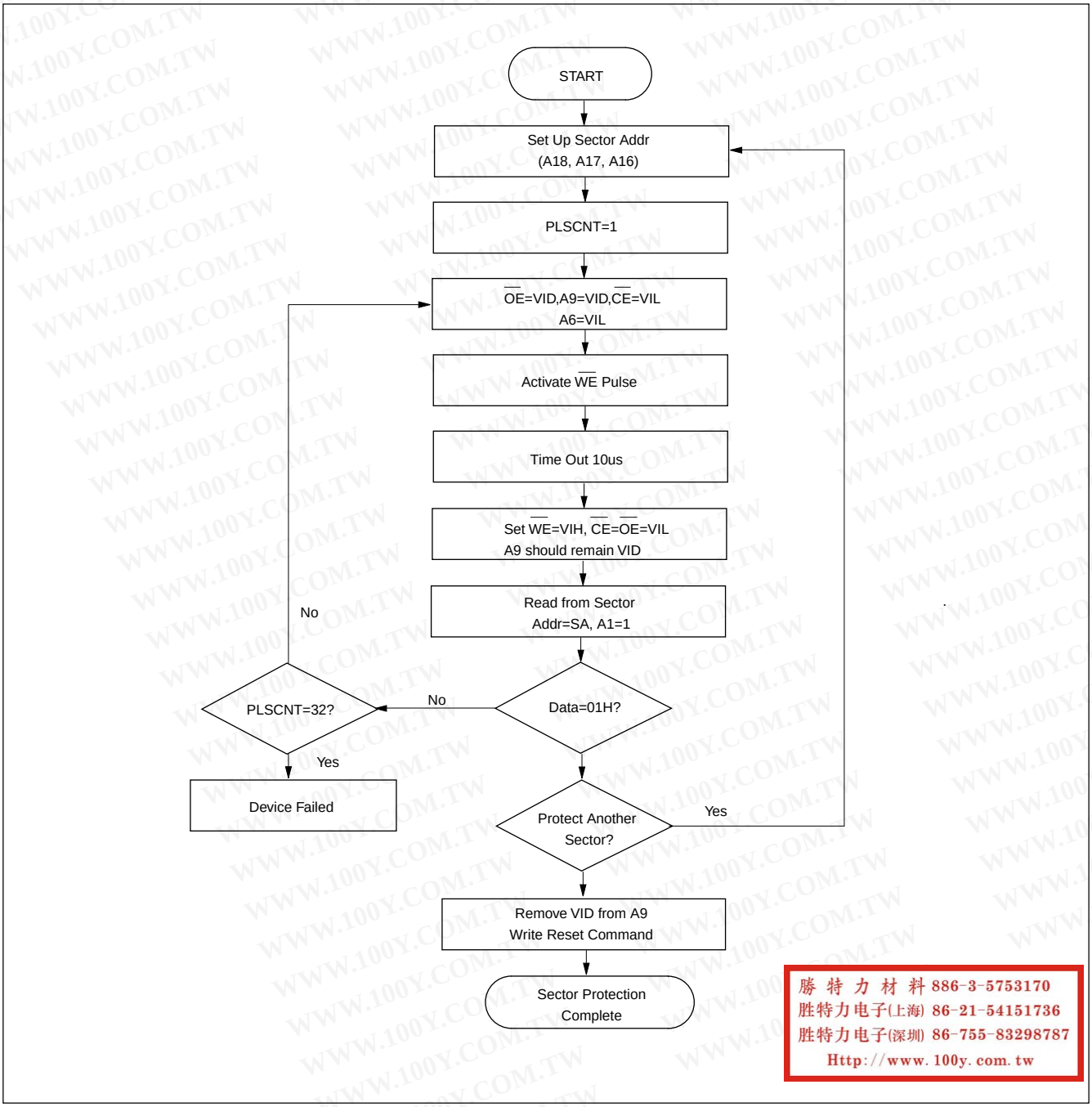
勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITH 12V



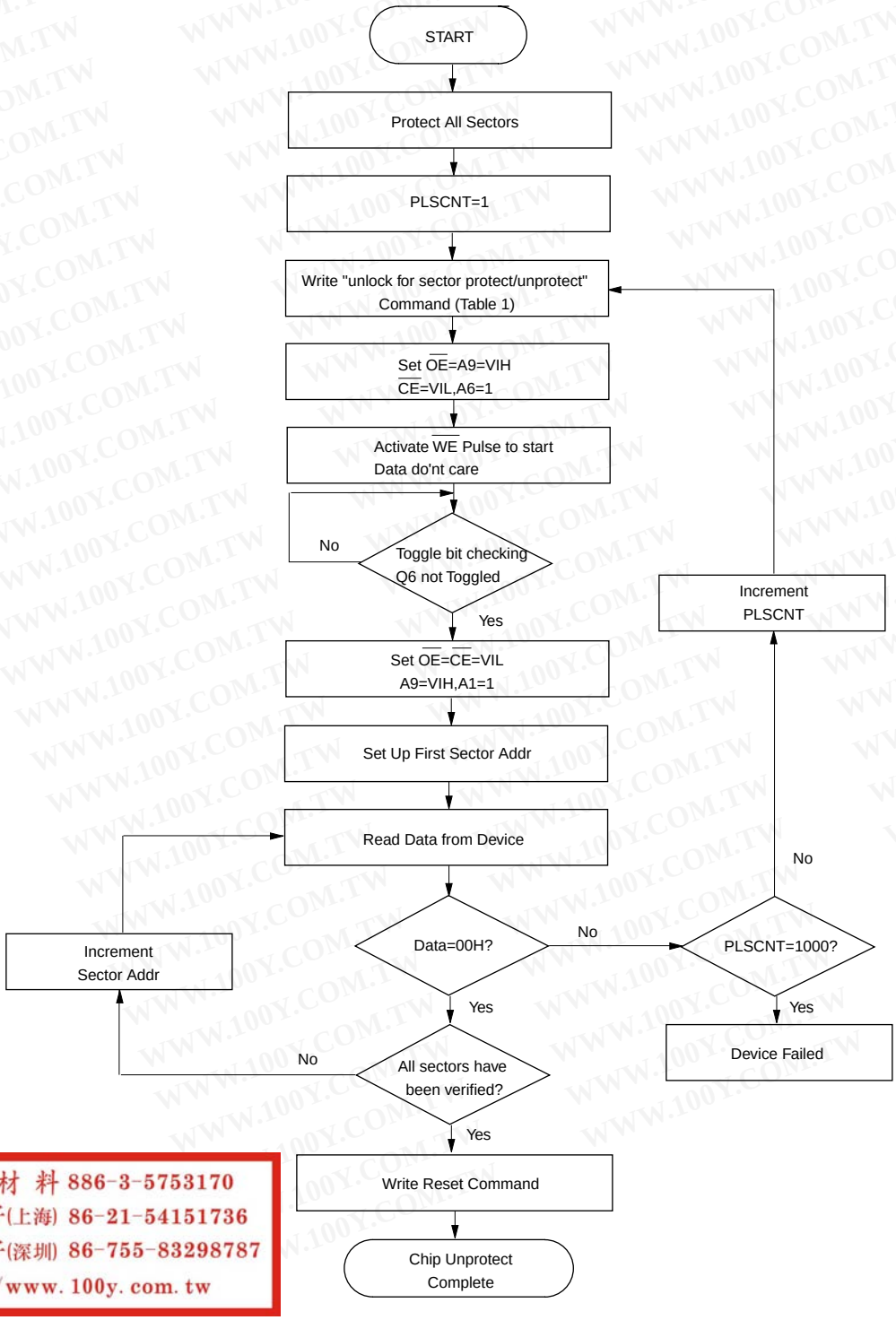
勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

SECTOR PROTECTION ALGORITHM FOR SYSTEM WITH 12V



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

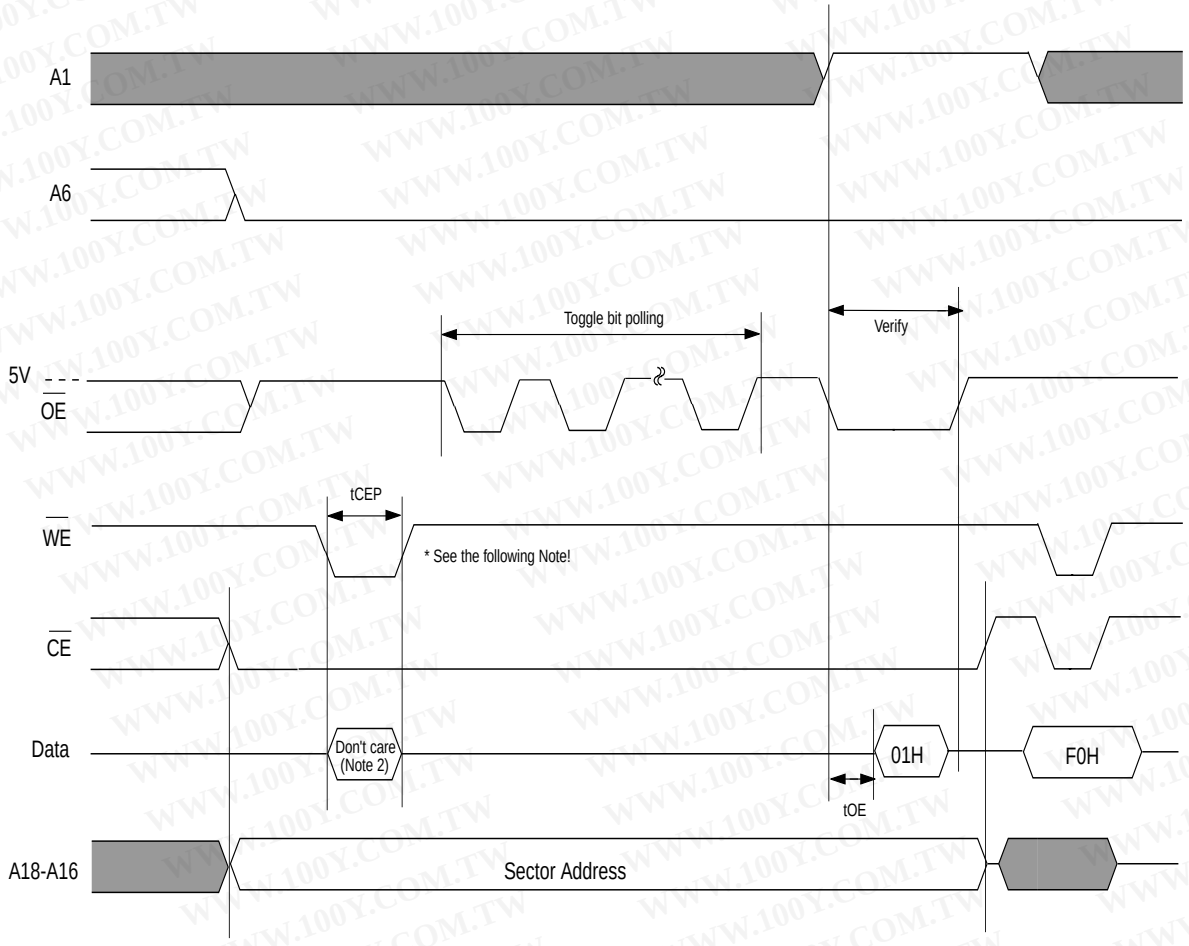
CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITH 12V



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

* It is recommended before unprotect whole chip, all sectors should be protected in advance.

TIMING WAVEFORM FOR SECTOR PROTECTION FOR SYSTEM WITHOUT 12V

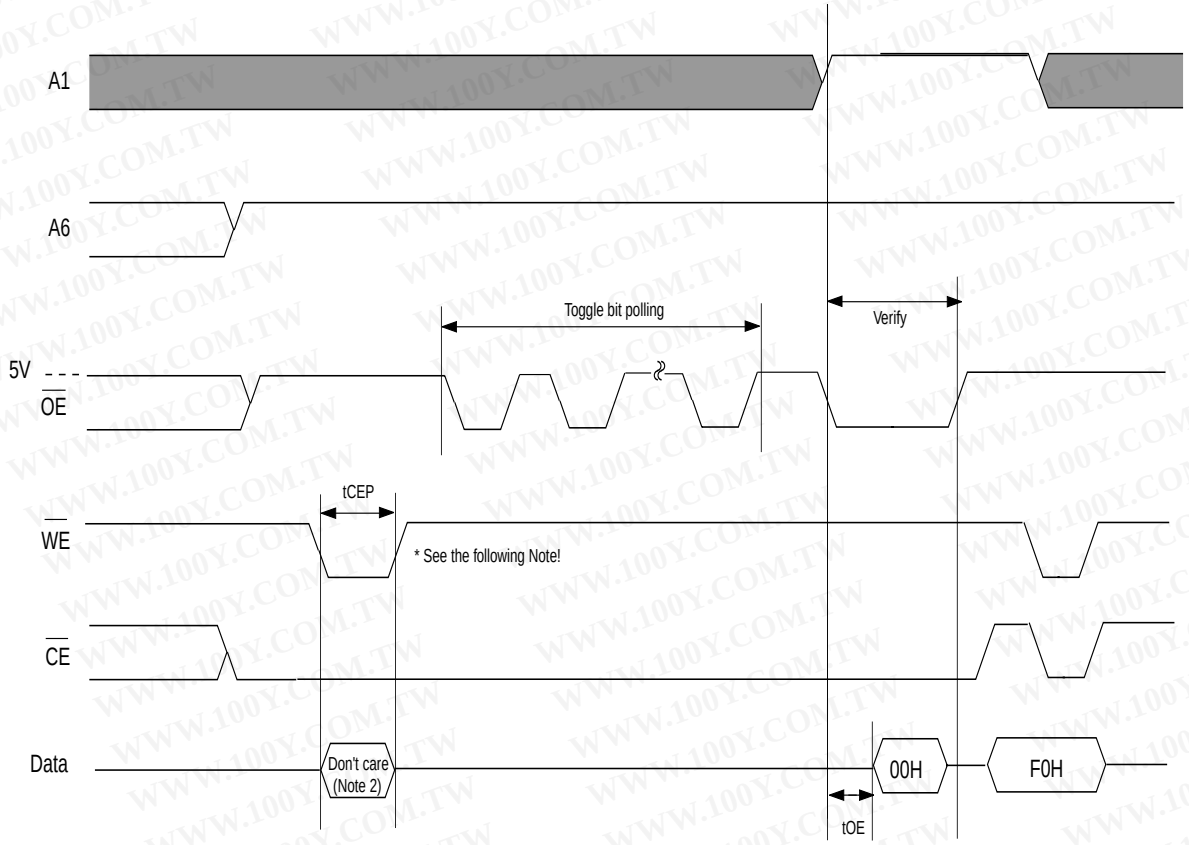


Note1: Must issue "unlock for sector protect/unprotect" command before sector protection for a system without 12V provided.

Note2: Except F0H

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITHOUT 12V

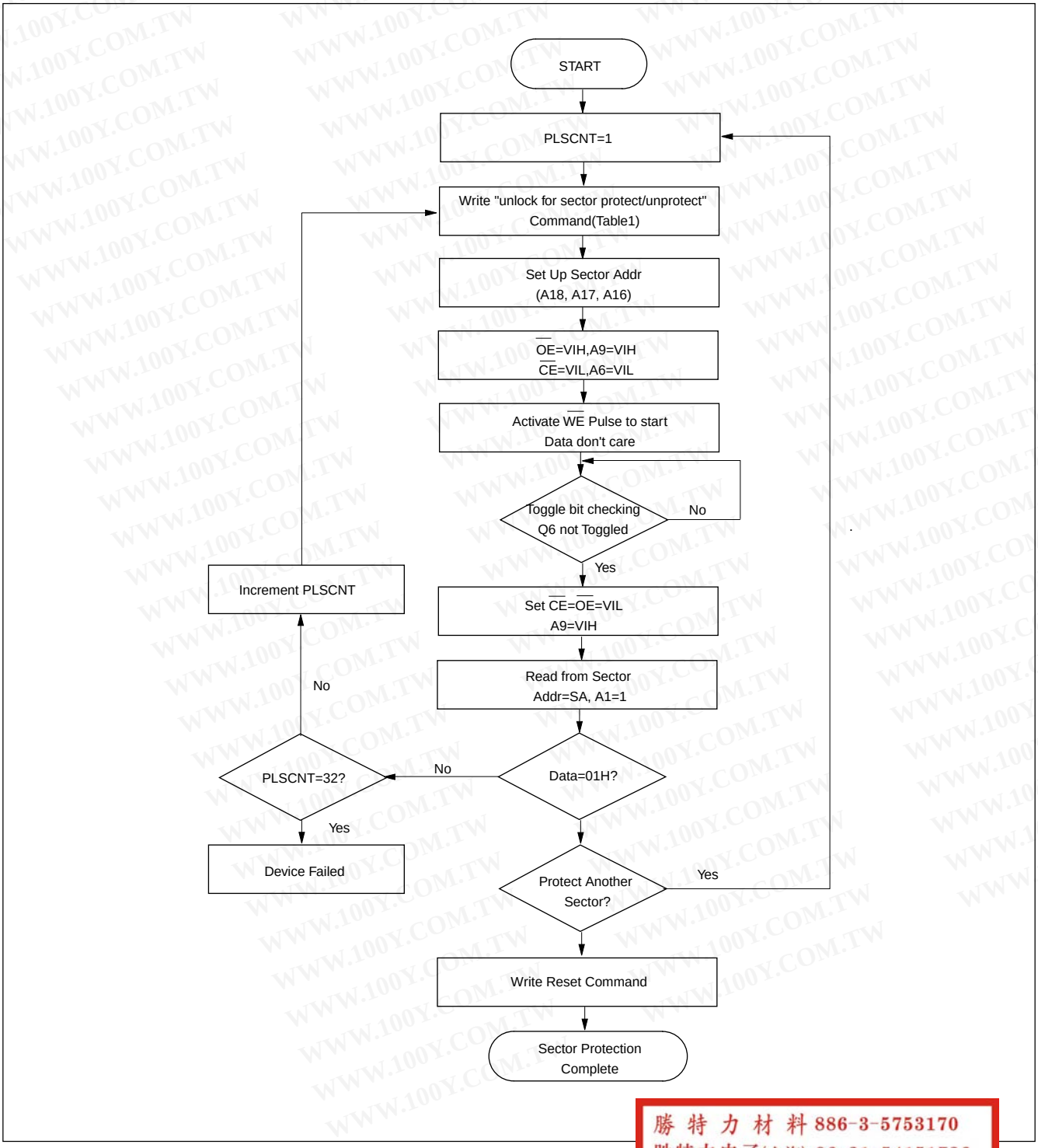


Note1: Must issue "unlock for sector protect/unprotect" command before sector unprotection for a system without 12V provided.

Note2: Except F0H

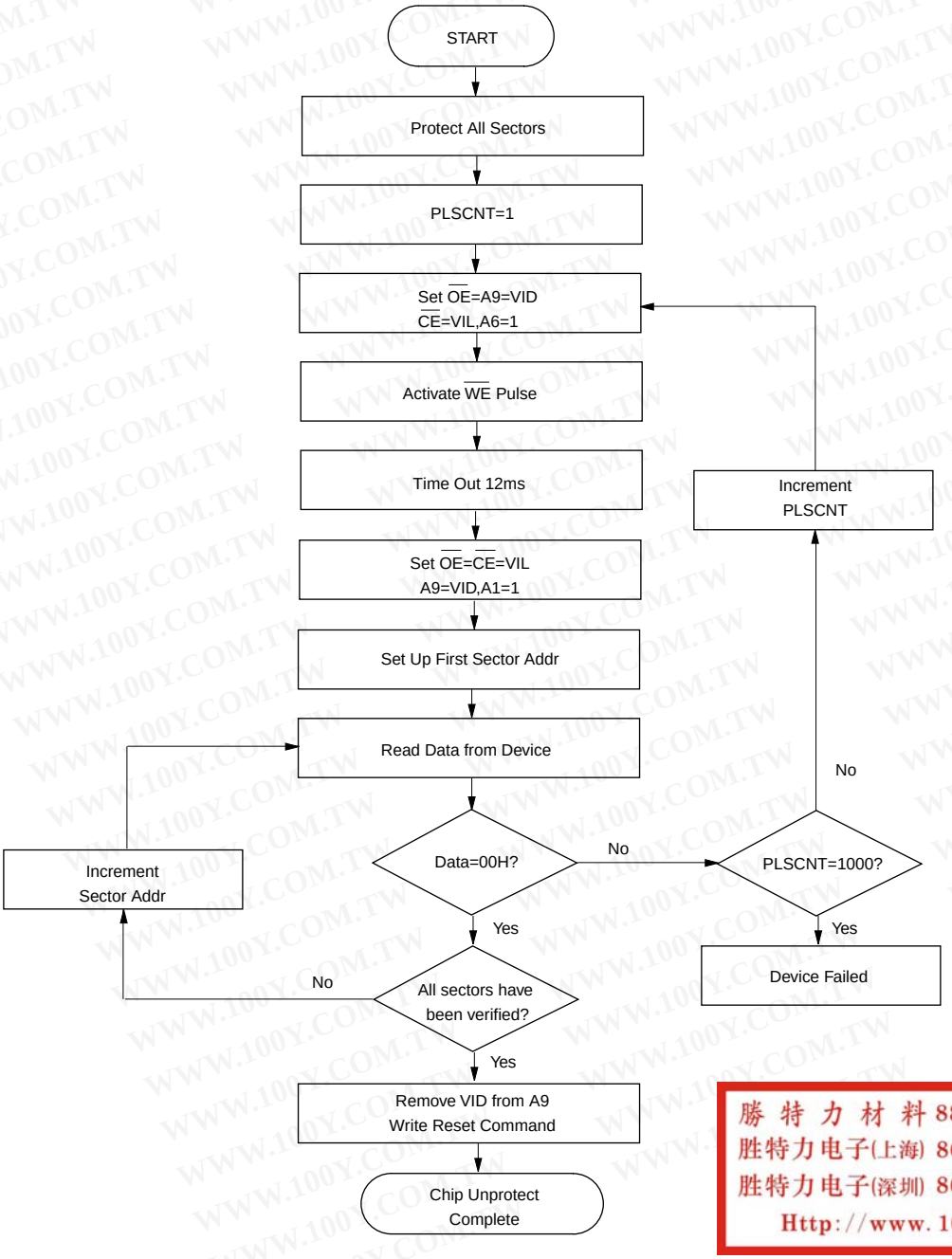
勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

SECTOR PROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

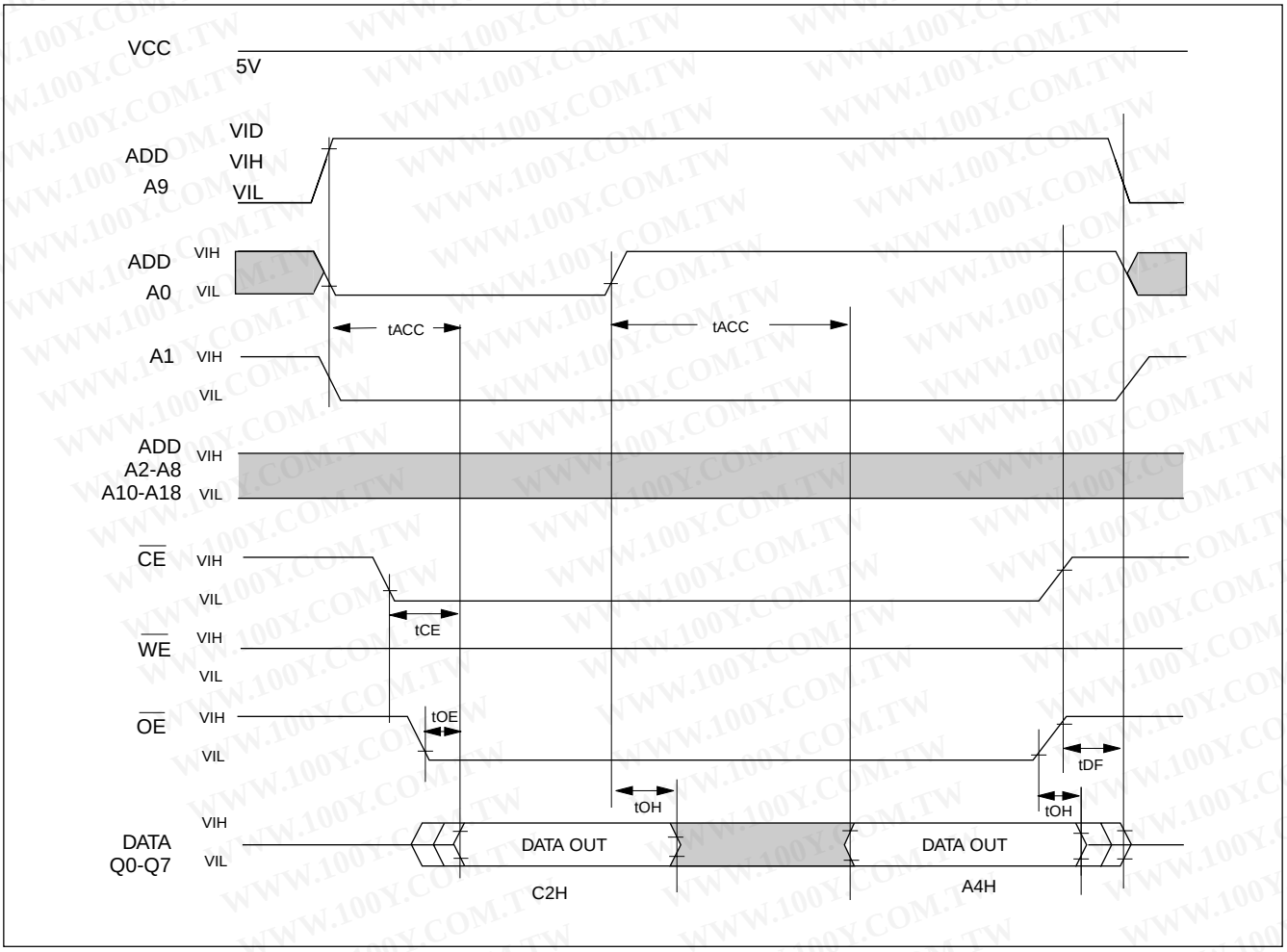
CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

* It is recommended before unprotect whole chip, all sectors should be protected in advance.

ID CODE READ TIMING WAVEFORM



勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

ORDERING INFORMATION

PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX29F040QC-55	55	30	5	32 Pin PLCC
MX29F040QC-70	70	30	5	32 Pin PLCC
MX29F040QC-90	90	30	5	32 Pin PLCC
MX29F040QC-12	120	30	5	32 Pin PLCC
MX29F040TC-55	55	30	5	32 Pin TSOP (Normal Type)
MX29F040TC-70	70	30	5	32 Pin TSOP (Normal Type)
MX29F040TC-90	90	30	5	32 Pin TSOP (Normal Type)
MX29F040TC-12	120	30	5	32 Pin TSOP (Normal Type)
MX29F040PC-55	55	30	5	32 Pin PDIP
MX29F040PC-70	70	30	5	32 Pin PDIP
MX29F040PC-90	90	30	5	32 Pin PDIP
MX29F040PC-12	120	30	5	32 Pin PDIP

ERASE AND PROGRAMMING PERFORMANCE(1)

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.(3)	
Sector Erase Time		1.3	10.4	sec
Chip Erase Time		4	32	sec
Byte Programming Time		7	210	us
Chip Programming Time		4	12	sec
Erase/Program Cycles	100,000			Cycles

Note: 1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25℃,5V.
3.Maximunm values measured at 25℃,4.5V.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

LATCHUP CHARACTERISTICS

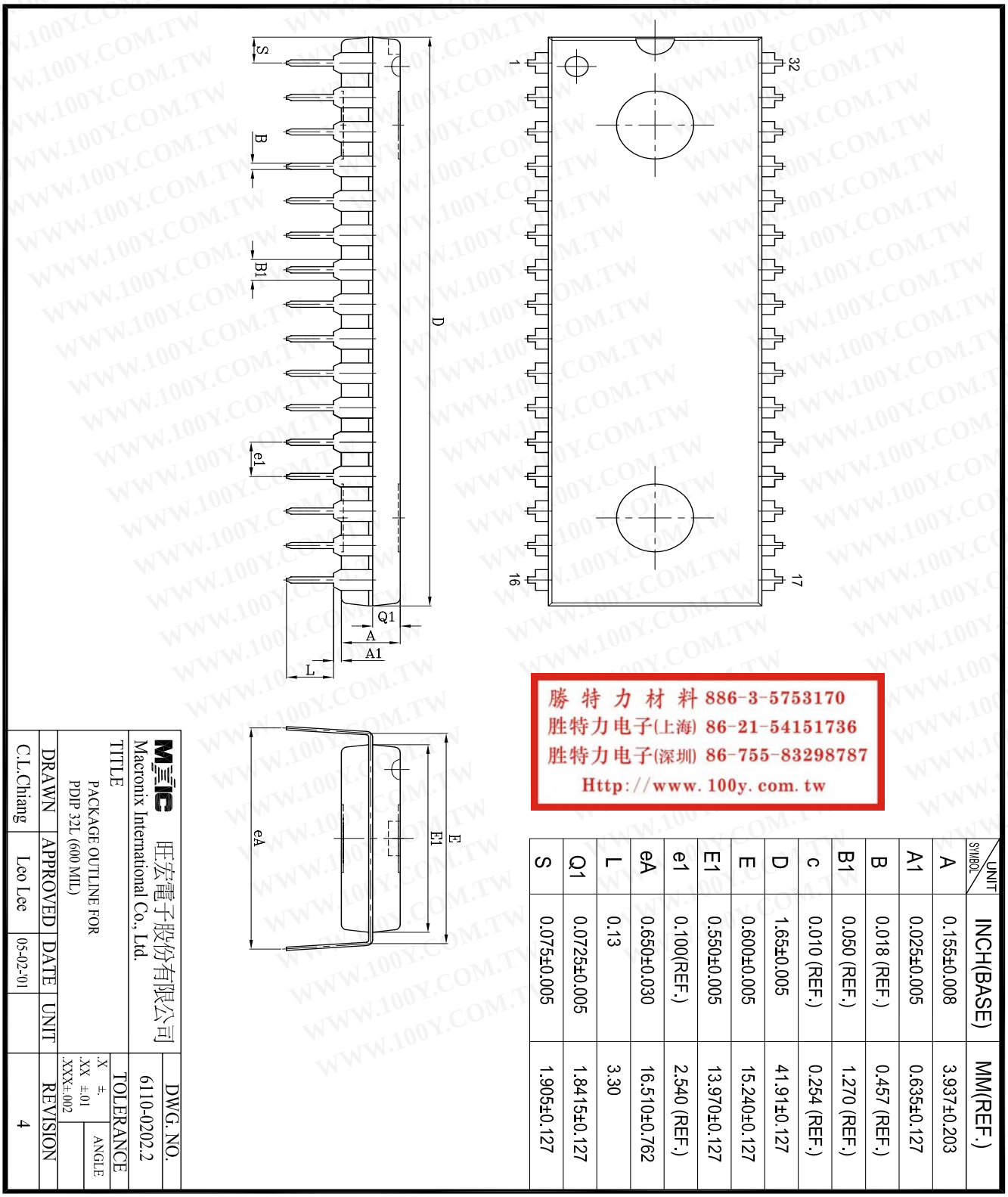
	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

DATA RETENTION

PARAMETER	MIN.	UNIT
Data Retention Time	20	Years

PACKAGE INFORMATION

32-PIN PLASTIC DIP

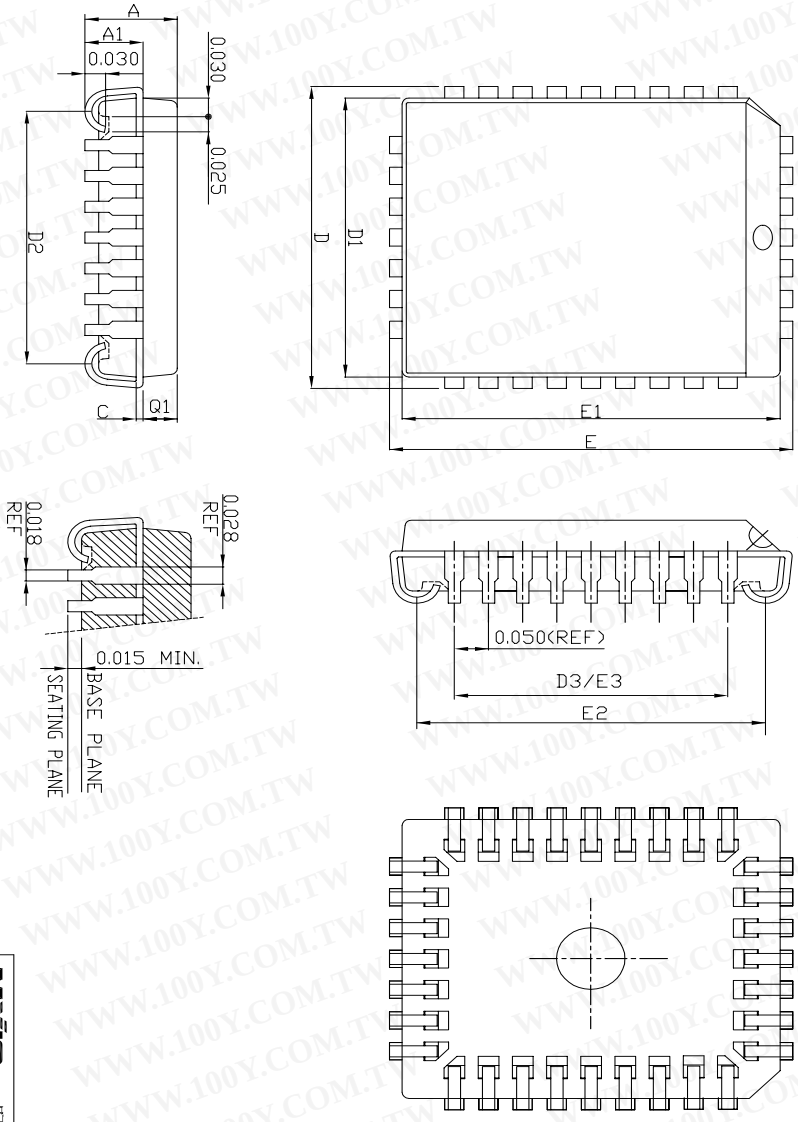


SYMBOL / UNIT	INCH(BASE)	MM(REF.)
A	0.155±0.008	3.937±0.203
A1	0.025±0.005	0.635±0.127
B	0.018 (REF.)	0.457 (REF.)
B1	0.050 (REF.)	1.270 (REF.)
c	0.010 (REF.)	0.254 (REF.)
D	1.65±0.005	41.91±0.127
E	0.600±0.005	15.240±0.127
E1	0.550±0.005	13.970±0.127
e1	0.100(REF.)	2.540 (REF.)
eA	0.650±0.030	16.510±0.762
L	0.13	3.30
Q1	0.0725±0.005	1.8415±0.127
S	0.075±0.005	1.905±0.127

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd.			DWG. NO. 6110-0202.2
TITLE PACKAGE OUTLINE FOR PDIP 32L (600 MIL)		UNIT	TOLERANCE .X ±.1 .XX ±.01 .XXX±.002 ANGLE
DRAWN C.L.Chiang	APPROVED Leo Lee	DATE 05-02-'01	REVISION 4

32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



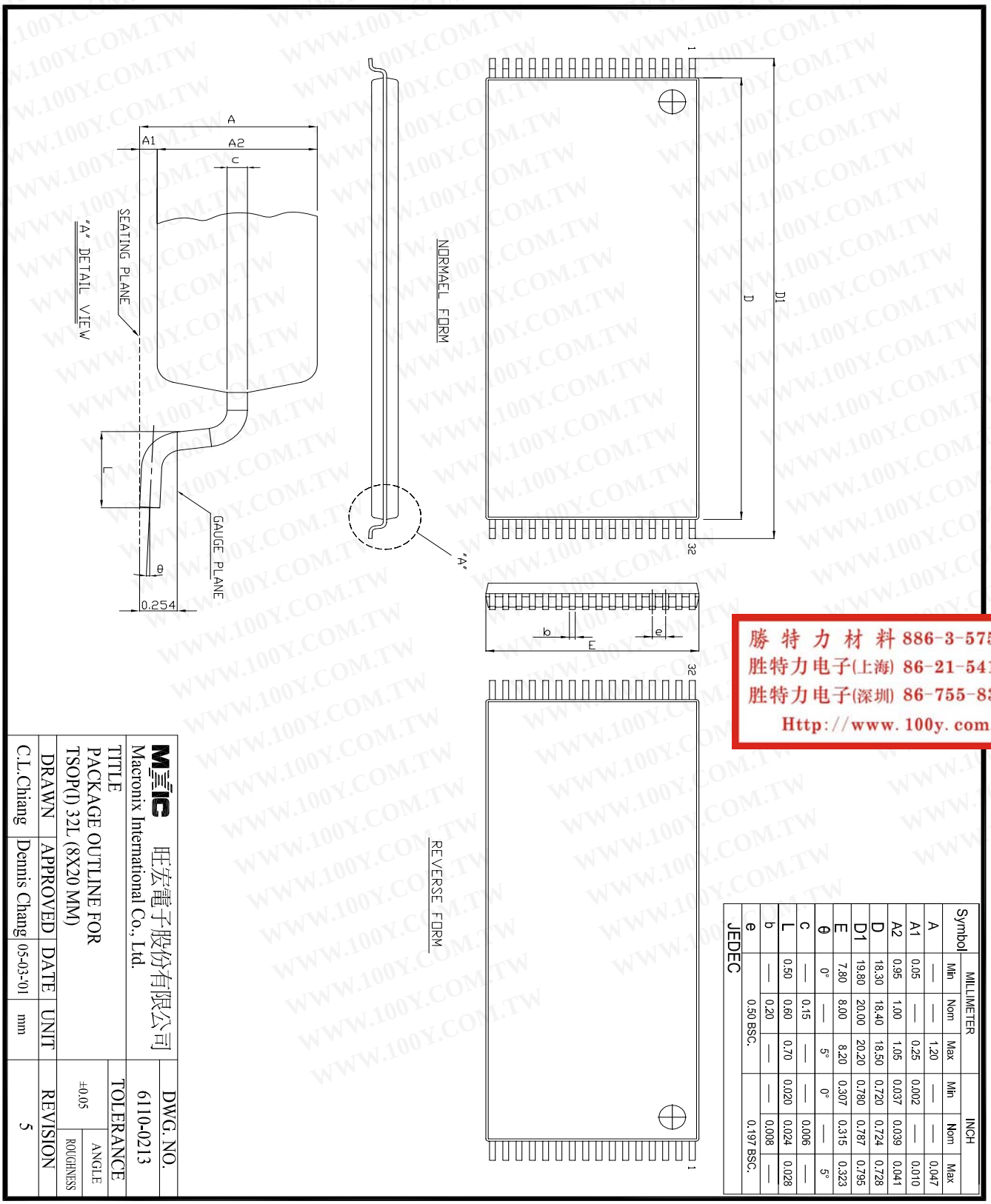
Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A			0.140			3.56
A1	0.080	0.085	0.090	2.03	2.16	2.29
Q1	0.048	0.050	0.052	1.22	1.27	1.32
c		0.010(REF)			0.25(REF)	
D	0.485	0.490	0.495	12.32	12.45	12.57
D1	0.450	0.453	0.456	11.43	11.51	11.58
D2	0.400	0.410	0.420	10.16	10.41	10.67
D3		0.300(REF)			7.62(REF)	
E	0.585	0.590	0.595	14.86	14.99	15.11
E1	0.550	0.553	0.556	13.97	14.05	14.12
E2	0.500	0.510	0.520	12.70	12.95	13.21
E3		0.400(REF)			10.16(REF)	

REFERENCE DOCUMENT : JEDEC SPEC - MS-016a

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

MIC 旺宏電子股份有限公司 Macronix International Co., Ltd.			DWG. NO. 6110-0209.1
TITLE PACKAGE OUTLINE FOR PLCC 32L			TOLERANCE .X ±.1 .XX ±.01 .XXX±.002 ANGLE ±2°
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	05-03-'01	inch
			REVISION 2

32-PIN PLASTIC TSOP



Symbol	MILLIMETER			INCH		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.25	0.002	—	0.010
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.30	18.40	18.50	0.720	0.724	0.728
D1	19.80	20.00	20.20	0.780	0.787	0.795
E	7.80	8.00	8.20	0.307	0.315	0.323
θ	0°	—	5°	0°	—	5°
c	—	0.15	—	—	0.006	—
L	0.50	0.60	0.70	0.020	0.024	0.028
b	—	0.20	—	—	0.008	—
e		0.50 BSC.			0.197 BSC.	
JEDEC						

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

MXIC 旺宏電子股份有限公司			DWG. NO.
Macronix International Co., Ltd.			6110-0213
TITLE			TOLERANCE
PACKAGE OUTLINE FOR TSOP(I) 32L (8X20 MM)		ANGLE ±0.05	
		ROUGHNESS	
DRAWN	APPROVED	DATE	UNIT	REVISION
C.L.Chiang	Dennis Chang	05-03-'01	mm	5

REVISION HISTORY

Revision	Description	Page	Date
1.0	To remove "Advanced Information" datasheet marking and contain information on products in full production.	P1	JUL/01/1999
1.1	To improve ICC1:from 40mA @5MHz to 30mA @5MHz	P1,13,14,33	JUL/12/1999
1.2	To add the description for 100K endurance cycle	P1,34	OCT/04/1999
	To modify timing of sector address loading period while operating multi-sector erase from 80us to 30us	P8	
	To modify tBAL from 80us to 100us	P15	
1.3	1.Program/erase cycle times:10K cycles-->100K cycles	P1,34	DEC/17/1999
	2.To remove A9 from "timing waveform for sector protection for system without 12V"	P28	
	To remove A9 from "timing waveform for chip unprotection for system without 12V"	P29	
	3.To add data retention minimum 20 years	P1,34	
1.4	Add erase suspend ready max. 100us in ERASE SUSPEND's section at page 9	P9	MAY/29/2000
1.5	To modify "Package Information"	P35~37	JUN/12/2001
1.6	To add "Ambient temperature with power applied"	P14	AUG/08/2001

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-348-8385
FAX:+65-348-8096

TAIPEI OFFICE:
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw