FAIRCHILD SEMICONDUCTOR™

September 1983
Revised February 1999

# MM74HC138
# 3-to-8 Line Decoder

## General Description

The MM74HC138 decoder utilizes advanced silicon-gate CMOS technology and is well suited to memory address decoding or data routing applications. The circuit features high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM74HC138 has 3 binary select inputs (A, B, and C). If the device is enabled, these inputs determine which one of the eight normally HIGH outputs will go LOW. Two active LOW and one active HIGH enables (G1, $\overline{G2A}$ and $\overline{G2B}$) are provided to ease the cascading of decoders.

The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally and pin equivalent to the 74LS138. All inputs are protected from damage due to static discharge by diodes to $V_{CC}$ and ground.

## Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

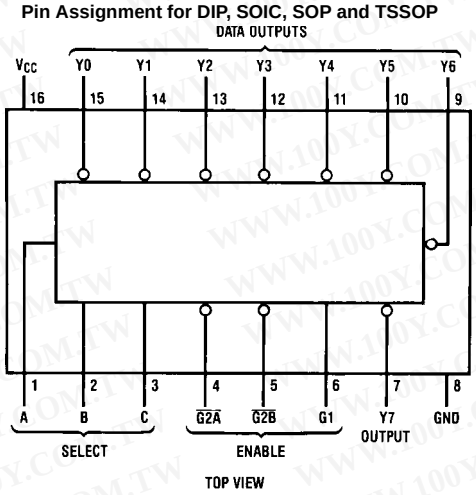
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| MM74HC138M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC138SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC138MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC138N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

## Connection Diagram

**Pin Assignment for DIP, SOIC, SOP and TSSOP**



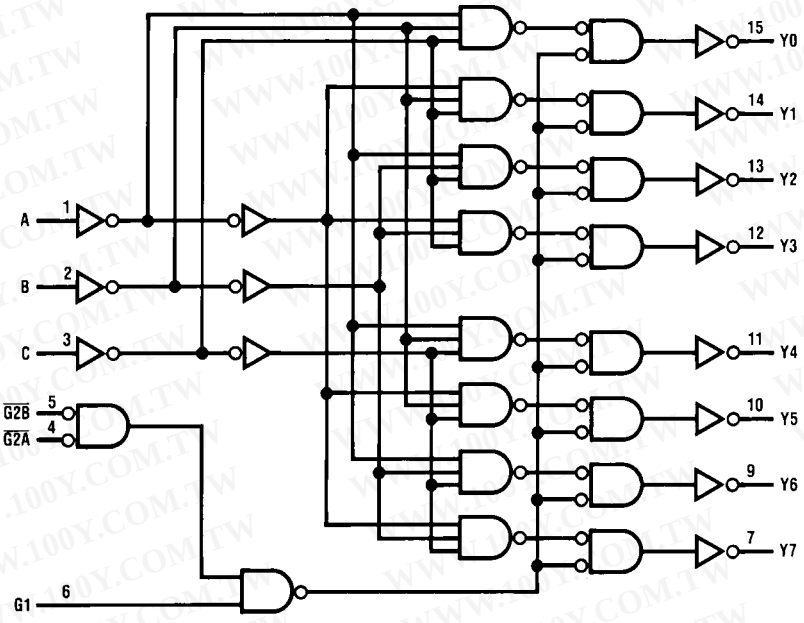
## Truth Table

| Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | Select | | | | | | | | | | |
| G1 | $\overline{G2}$ (Note 1) | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH Level, L = LOW Level, X = don't care

**Note 1:** $\overline{G2}$ = G2A+G2B

## Logic Diagram



## Absolute Maximum Ratings (Note 2)

(Note 3)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | − 0.5 to + 7.0V |
| DC Input Voltage ($V_{IN}$) | − 1.5 to $V_{CC}$ + 1.5V |
| DC Output Voltage ($V_{OUT}$) | − 0.5 to $V_{CC}$ + 0.5V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ± 20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ± 25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ± 50 mA |
| Storage Temperature Range ($T_{STG}$) | − 65°C to + 150°C |
| Power Dissipation ($P_D$) | |
| (Note 4) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature ($T_L$) | |
| (Soldering 10 seconds) | 260°C |

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 2 | 6 | V |
| DC Input or Output Voltage ($V_{IN}$, $V_{OUT}$) | 0 | $V_{CC}$ | V |
| Operating Temperature Range ($T_A$) | −40 | +85 | °C |
| Input Rise or Fall Times ($t_r$, $t_f$) $V_{CC}$ = 2.0V | | 1000 | ns |
| $V_{CC}$ = 4.5V | | 500 | ns |
| $V_{CC}$ = 6.0V | | 400 | ns |

**Note 2:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 3:** Unless otherwise specified all voltages are referenced to ground.

**Note 4:** Power Dissipation temperature derating — plastic "N" package: – 12 mW/°C from 65°C to 85°C.

## DC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40 to 85°C | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | 2.0V | | 1.5 | 1.5 | V |
| | | | 4.5V | | 3.15 | 3.15 | V |
| | | | 6.0V | | 4.2 | 4.2 | V |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | 2.0V | | 0.5 | 0.5 | V |
| | | | 4.5V | | 1.35 | 1.35 | V |
| | | | 6.0V | | 1.8 | 1.8 | V |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ \| $I_{OUT}$ \| ≤ 20 μA | 2.0V | 2.0 | 1.9 | 1.9 | V |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | V |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ \|$I_{OUT}$ \| ≤ 4.0 mA | 4.5V | 4.2 | 3.98 | 3.84 | V |
| | | \| $I_{OUT}$ \| ≤ 5.2 mA | 6.0V | 5.7 | 5.48 | 5.34 | V |
| $V_{OL}$ | Maximum LOW Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ \| $I_{OUT}$ \| ≤ 20 μA | 2.0V | 0 | 0.1 | 0.1 | V |
| | | | 4.5V | 0 | 0.1 | 0.1 | V |
| | | | 6.0V | 0 | 0.1 | 0.1 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ \| $I_{OUT}$ \| ≤ 4.0 mA | 4.5V | 0.2 | 0.26 | 0.33 | V |
| | | \| $I_{OUT}$ \| ≤ 5.2 mA | 6.0V | 0.2 | 0.26 | 0.33 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | ±0.1 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND $I_{OUT}$ = 0 μA | 6.0V | | 8.0 | 80 | μA |

**Note 5:** For a power supply of 5V ± 10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15 pF, $t_r = t_f$ = 6 ns

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $t_{PLH}$ | Maximum Propagation Delay, Binary Select to any Output | | 18 | 25 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Binary Select to any Output | | 28 | 35 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, G1 to any Output | | 18 | 25 | ns |
| $t_{PHL}$ | Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output | | 23 | 30 | ns |
| $t_{PLH}$ | Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output | | 18 | 25 | ns |

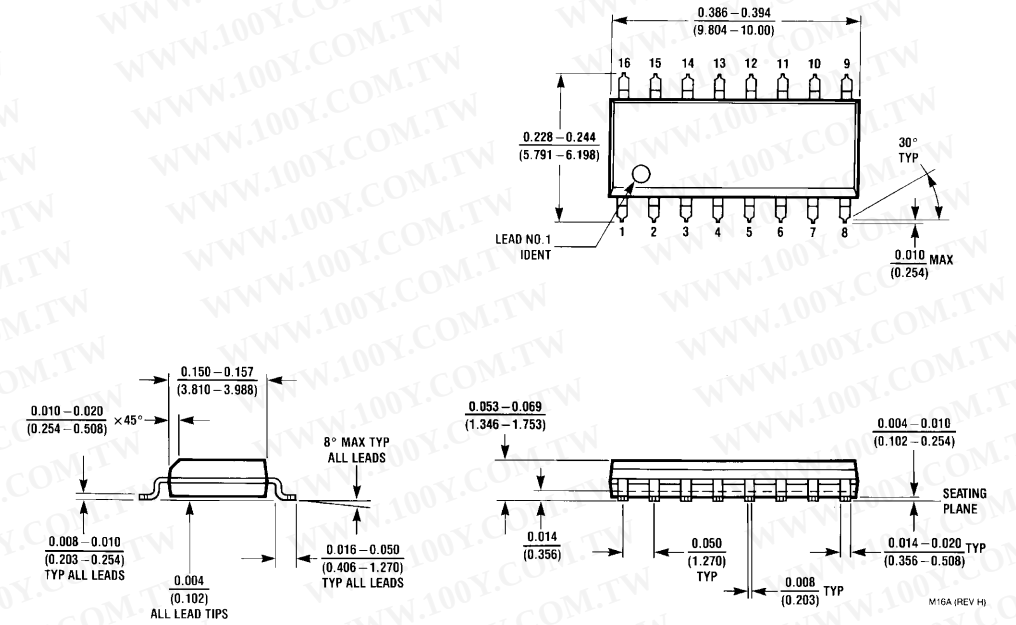
## AC Electrical Characteristics

$C_L$ = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

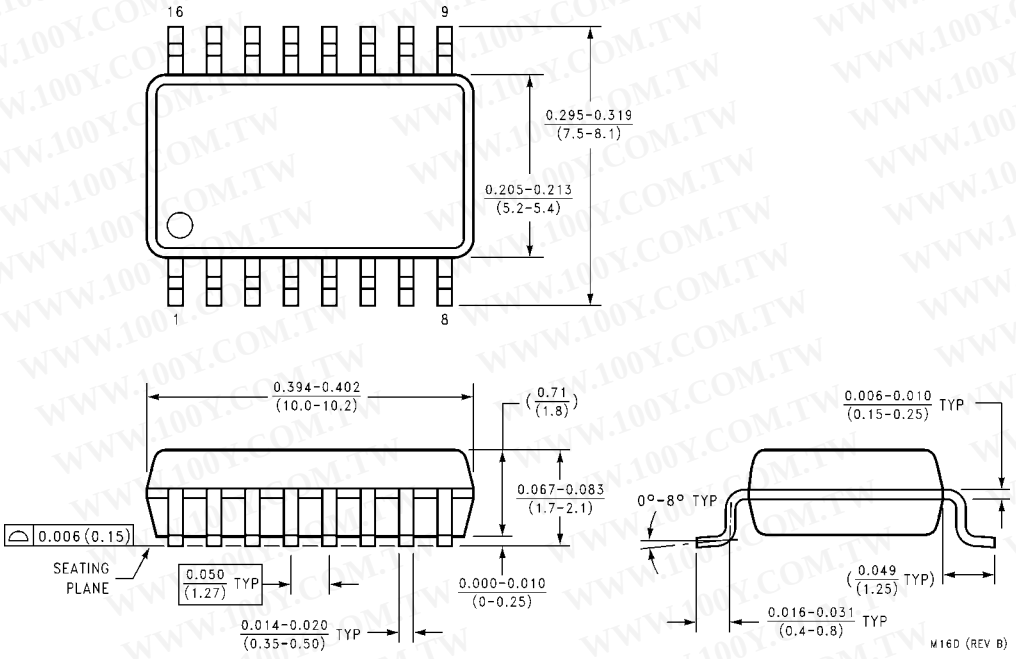
| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$= 25°C | $T_A$= −40 to 85°C | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $t_{PLH}$ | Maximum Propagation | | 2.0V | 75 | 150 | 189 | ns |
| | Delay Binary Select to | | 4.5V | 15 | 30 | 38 | ns |
| | any Output LOW-to-HIGH | | 6.0V | 13 | 26 | 32 | ns |
| $t_{PHL}$ | Maximum Propagation | | 2.0V | 100 | 200 | 252 | ns |
| | Delay Binary Select to any | | 4.5V | 20 | 40 | 50 | ns |
| | Output HIGH-to-LOW | | 6.0V | 17 | 34 | 43 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation | | 2.0V | 75 | 150 | 189 | ns |
| | Delay G1 to any | | 4.5V | 15 | 30 | 38 | ns |
| | Output | | 6.0V | 13 | 26 | 32 | ns |
| $t_{PHL}$ | Maximum Propagation | | 2.0V | 82 | 175 | 221 | ns |
| | Delay $\overline{G2A}$ or $\overline{G2B}$ to | | 4.5V | 28 | 35 | 44 | ns |
| | Output | | 6.0V | 22 | 30 | 37 | ns |
| $t_{PLH}$ | Maximum Propagation | | 2.0V | 75 | 150 | 189 | ns |
| | Delay $\overline{G2A}$ or $\overline{G2B}$ to | | 4.5V | 15 | 30 | 38 | ns |
| | Output | | 6.0V | 13 | 26 | 32 | ns |
| $t_{TLH}$, $t_{THL}$ | Output Rise and | | 2.0V | 30 | 75 | 95 | ns |
| | Fall Time | | 4.5V | 8 | 15 | 19 | ns |
| | | | 6.0V | 7 | 13 | 16 | ns |
| $C_{IN}$ | Maximum Input Capacitance | | | 3 | 10 | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | (Note 6) | | 75 | | | pF |

**Note 6:** $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

## Physical Dimensions inches (millimeters) unless otherwise noted

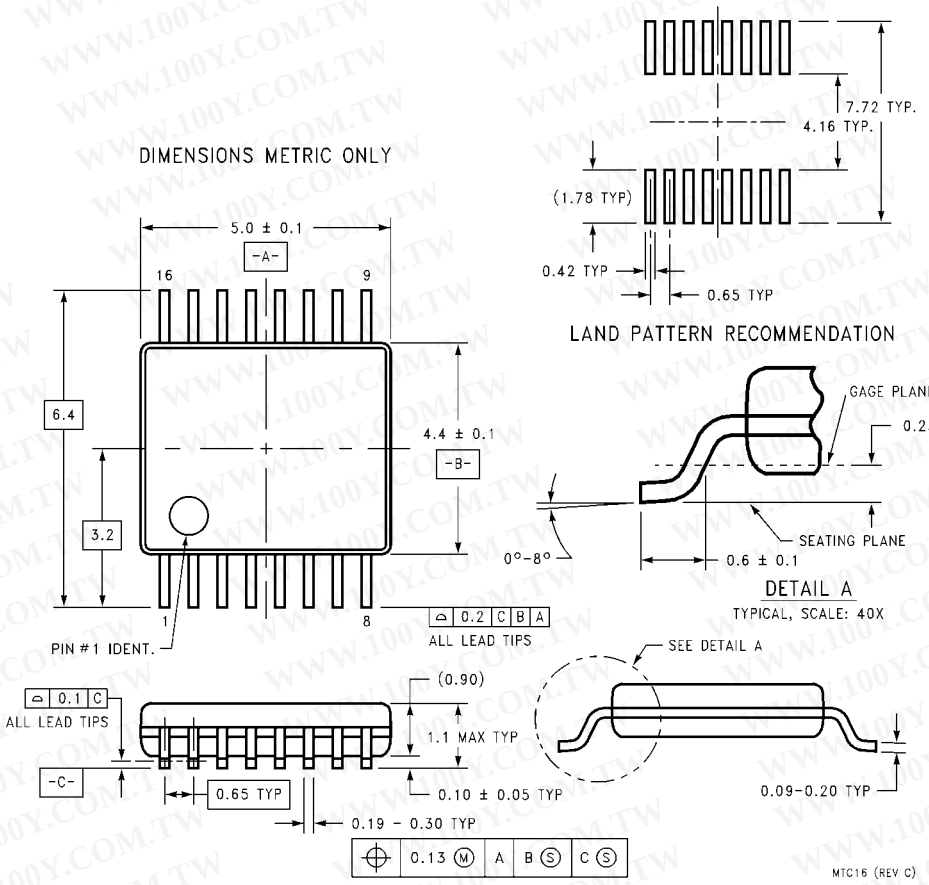



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow**
**Package Number M16A**



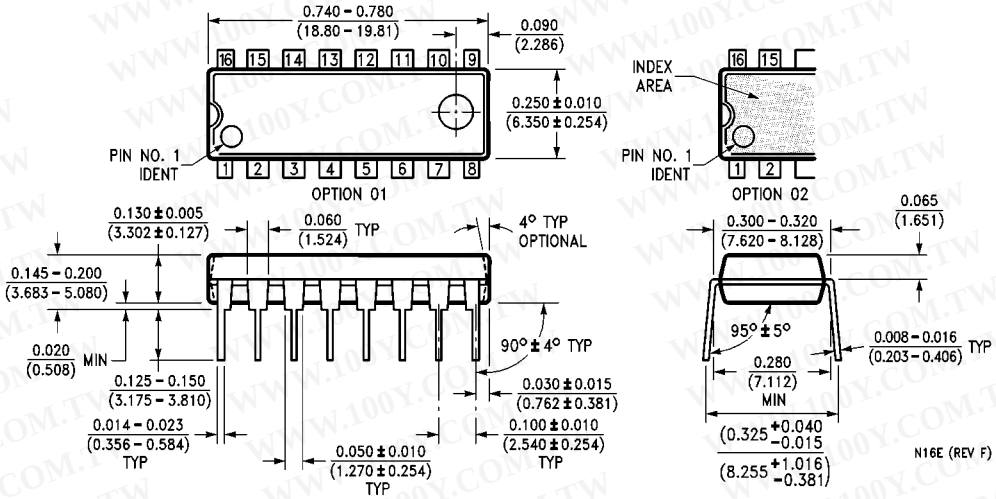

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**



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