19-0230; Rev 2a; 1/97

MAXIM

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

General Description

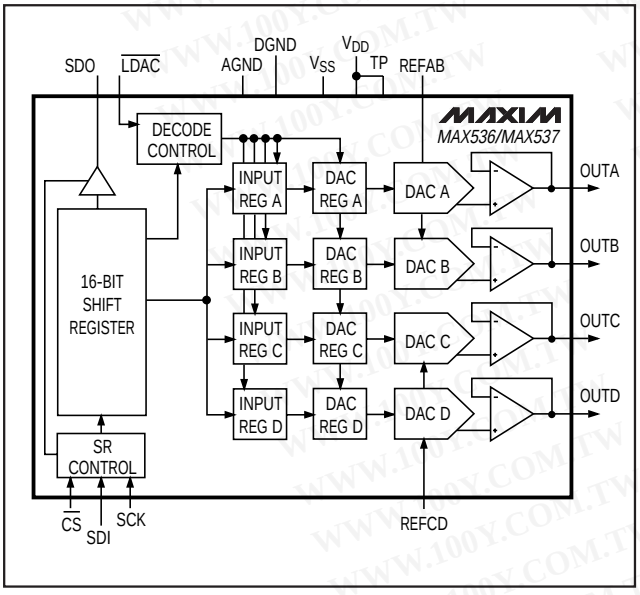
The MAX536/MAX537 combine four 12-bit, voltage-output digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving 16-pin package. Offset, gain, and linearity are factory calibrated to provide the MAX536's ±1LSB total unadjusted error. The MAX537 operates with ±5V supplies, while the MAX536 uses -5V and +12V to +15V supplies.

Each DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word is used to load data into each input/DAC register. The serial interface is compatible with either SPI/QSPI™ or Microwire™, and allows the input and DAC registers to be updated independently or simultaneously with a single software command. The DAC registers can be simultaneously updated with a hardware $\overline{LDAC}$ pin. All logic inputs are TTL/CMOS compatible.

Applications

Industrial Process Controls
Automatic Test Equipment
Digital Offset and Gain Adjustment
Motion Control Devices
Remote Industrial Controls
Microprocessor-Controlled Systems

Functional Diagram



Features

- ♦ **Four 12-Bit DACs with Output Buffers**
- ♦ **Simultaneous or Independent Control of Four DACs via a 3-Wire Serial Interface**
- ♦ **Power-On Reset**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **±1LSB Total Unadjusted Error (MAX536)**
- ♦ **Full 12-Bit Performance without Adjustments**
- ♦ **±5V Supply Operation (MAX537)**
- ♦ **Double-Buffered Digital Inputs**
- ♦ **Buffered Voltage Output**
- ♦ **16-Pin DIP/SO Packages**

Ordering Information

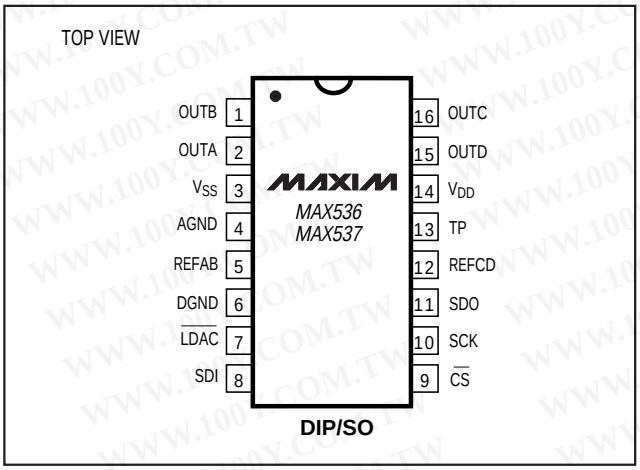
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX536ACPE	0°C to +70°C	16 Plastic DIP	±½
MAX536BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX536ACWE	0°C to +70°C	16 Wide SO	±½
MAX536BCWE	0°C to +70°C	16 Wide SO	±1
MAX536BC/D	0°C to +70°C	Dice*	±1
MAX536AEPE	-40°C to +85°C	16 Plastic DIP	±½
MAX536BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX536AEWE	-40°C to +85°C	16 Wide SO	±½
MAX536BEWE	-40°C to +85°C	16 Wide SO	±1
MAX536AMDE	-55°C to +125°C	16 Ceramic SB**	±½
MAX536BMDE	-55°C to +125°C	16 Ceramic SB**	±1

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND or DGND
  MAX536 ..... -0.3V, +17V
  MAX537 ..... -0.3V, +7V
V_{SS} to AGND or DGND ..... -7V, +0.3V
SDI, SCK, $\overline{CS}$, $\overline{LDAC}$, TP, SDO
  to AGND or DGND ..... -0.3V, (V_{DD} + 0.3V)
REFAB, REFCD to AGND or DGND ..... -0.3V, (V_{DD} + 0.3V)
OUT_ to AGND or DGND ..... V_{DD}, V_{SS}
Maximum Current into Any Pin 50mA

Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
  Wide SO (derate 9.52mW/°C above +70°C) 762mW
  Ceramic SB (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Ranges
  MAX53_AC_E/BC_E ..... 0°C to +70°C
  MAX53_AE_E/BE_E ..... -40°C to +85°C
  MAX53_AMDE/BMDE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX536

(V_{DD} = +15V, V_{SS} = -5V, REFAB/REFCD = 10V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION							
Resolution	N			12			Bits
Total Unadjusted Error (Note 1)	TUE	T_A = +25°C	MAX536A			±1.0	LSB
			MAX536B			±2.0	
		T_A = T_{MIN} to T_{MAX}	MAX536AC			±2.0	
			MAX536BC			±3.0	
			MAX536AE			±2.5	
			MAX536BE			±3.5	
			MAX536AM			±3.0	
			MAX536BM			±4.0	
Integral Nonlinearity	INL	MAX536A			±0.15	±0.50	LSB
		MAX536B				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error		T_A = +25°C	MAX536A			±2.5	mV
			MAX536B			±5.0	
		T_A = T_{MIN} to T_{MAX}	MAX536AC			±5.0	
			MAX536BC			±7.5	
			MAX536AE			±6.1	
			MAX536BE			±8.5	
			MAX536AM			±7.5	
			MAX536BM			±10.0	
Gain Error		R_L = ∞			-0.1	±1.0	LSB
		R_L = 5kΩ	MAX536_C/E		-0.6	±1.5	
			MAX536_M			±2.0	
V_{DD} Power-Supply Rejection Ratio	PSRR	T_A = +25°C, 10.8V < V_{DD} < 16.5V			±0.02	±0.125	LSB/V
V_{SS} Power-Supply Rejection Ratio	PSRR	T_A = +25°C, -5.5V < V_{SS} < -4.5V			±0.03	±0.30	LSB/V

ELECTRICAL CHARACTERISTICS—MAX536 (continued)

(V_{DD} = +15V, V_{SS} = -5V, REFAB/REFCD = 10V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MATCHING PERFORMANCE (T_A = +25°C)						
Total Unadjusted Error	TUE	MAX536A			±1.0	LSB
		MAX536B			±2.0	
Gain Error				±0.1	±1.0	LSB
Offset Error		MAX536A		±1.2	±2.5	mV
		MAX536B		±1.2	±5.0	
Integral Nonlinearity	INL			±0.2	±1.0	LSB
REFERENCE INPUT						
Reference Input Range	REF		0.0		V_{DD} – 4	V
Reference Input Resistance	RREF	Code dependent, minimum at code 555 hex	5			kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference 3dB Bandwidth		V_{REF} = 2Vp-p		700		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 10Vp-p at 400Hz		-100		dB
		Input code = all 0s, V_{REF} = 10Vp-p at 4kHz		-82		
Total Harmonic Distortion Plus Noise	THD + N	V_{REF} = 2.0Vp-p at 50kHz		0.012		%
DIGITAL INPUTS (SDI, SCK, $\overline{CS}$, $\overline{LDAC}$)						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current		V_{IN} = 0V or V_{DD}			1.0	µA
Input Capacitance (Note 2)					10	pF
DIGITAL OUTPUT (SDO)						
Output Low Voltage	V_{OL}	SDO sinking 5mA		0.18	0.40	V
Output Leakage Current		SDO = 0V to V_{DD}			±10	µA
DYNAMIC PERFORMANCE (R_L = 5kΩ, C_L = 100pF)						
Voltage-Output Slew Rate				5		V/µs
Output Settling Time		To ±½LSB of full scale		3		µs
Digital Feedthrough				5		nV-s
Digital Crosstalk (Note 3)		V_{REF} = 5V		8		nV-s
POWER SUPPLIES						
Positive Supply Range	V_{DD}		10.8		16.5	V
Negative Supply Range	V_{SS}		-4.5		-5.5	V
Positive Supply Current (Note 4)	I_{DD}	T_A = +25°C		8	18	mA
		T_A = T_{MIN} to T_{MAX}			25	
Negative Supply Current (Note 4)	I_{SS}	T_A = +25°C		-6	-16	mA
		T_A = T_{MIN} to T_{MAX}			-23	

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX536 (continued)

(V_{DD} = +15V, V_{SS} = -5V, REFAB/REFCD = 10V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Note 5)							
Internal Power-On Reset Pulse Width (Note 2)	t_{POR}					20	µs
SCK Clock Period	t_{CP}			100			ns
SCK Pulse Width High	t_{CH}			30			ns
SCK Pulse Width Low	t_{CL}			30			ns
$\overline{CS}$ Fall to SCK Rise Setup Time	t_{CSS}			20			ns
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}			10			ns
SDI Setup Time	t_{DS}			40	26		ns
SDI Hold Time	t_{DH}			0			ns
SCK Rise to SDO Valid Propagation Delay (Note 6)	t_{DO1}	1kΩ pull-up on SDO to V_{DD}, C_{LOAD} = 50pF	SDO high		78	105	ns
			SDO low		50	80	
SCK Fall to SDO Valid Propagation Delay (Note 7)	t_{DO2}	1kΩ pull-up on SDO to V_{DD}, C_{LOAD} = 50pF	SDO high		81	110	ns
			SDO low		53	85	
$\overline{CS}$ Fall to SDO Enable (Note 8)	t_{DV}				27	45	ns
$\overline{CS}$ Rise to SDO Disable (Note 9)	t_{TR}				40	60	ns
SCK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	Continuous SCK, SCK edge ignored		20			ns
$\overline{CS}$ Rise to SCK Rise Hold Time	t_{CS1}	SCK edge ignored		20			ns
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}			30			ns
$\overline{CS}$ Pulse Width High	t_{CSW}			40			ns

Note 1: TUE is specified with no resistive load.
Note 2: Guaranteed by design.
Note 3: Crosstalk is defined as the glitch energy at any DAC output in response to a full-scale step change on any other DAC.
Note 4: Digital inputs at 2.4V; with digital inputs at CMOS levels, I_{DD} decreases slightly.
Note 5: All input signals are specified with t_R = t_F ≤ 5ns. Logic input swing is 0V to 5V.
Note 6: Serial data clocked out of SDO on SCK's falling edge. (SDO is an open-drain output for the MAX536. The MAX537's SDO pin has an internal active pull-up.)
Note 7: Serial data clocked out of SDO on SCK's rising edge.
Note 8: SDO changes from High-Z state to 90% of final value.
Note 9: SDO rises 10% toward High-Z state.

ELECTRICAL CHARACTERISTICS—MAX537

(V_{DD} = +5V, V_{SS} = -5V, REFAB/REFCD = 2.5V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION							
Resolution	N			12			Bits
Integral Nonlinearity	INL	MAX537A			±0.15	±0.50	LSB
		MAX537B				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error		T_A = +25°C	MAX537A			±3.0	mV
			MAX537B			±6.0	
		T_A = T_{MIN} to T_{MAX}	MAX537AC			±6.0	
			MAX537BC			±9.0	
			MAX537AE			±7.0	
			MAX537BE			±11.0	
			MAX537AM			±9.0	
			MAX537BM			±15.0	
Gain Error		R_L = ∞			-0.3	±1.5	LSB
		R_L = 5kΩ			-0.8	±3.0	
V_{DD} Power-Supply Rejection Ratio	PSRR	T_A = +25°C, 4.5V ≤ V_{DD} ≤ 5.5V			±0.01	±0.5	LSB/V
V_{SS} Power-Supply Rejection Ratio	PSRR	T_A = +25°C, -5.5V ≤ V_{SS} ≤ -4.5V			±0.02	±0.7	LSB/V
MATCHING PERFORMANCE (T_A = +25°C)							
Gain Error					±0.1	±1.25	LSB
Offset Error		MAX537A			±0.3	±3.0	mV
		MAX537B			±0.3	±6.0	
Integral Nonlinearity	INL				±0.35	±1.0	LSB
REFERENCE INPUT							
Reference Input Range	REF			0.0		V_{DD} - 2.2	V
Reference Input Resistance	RREF	Code dependent, minimum at code 555 hex		5			kΩ
MULTIPLYING-MODE PERFORMANCE							
Reference 3dB Bandwidth		V_{REF} = 2V_{p-p}			700		kHz
Reference Feedthrough		Input code = all 0s	V_{REF} = 10V_{p-p} at 400Hz		-100		dB
			V_{REF} = 10V_{p-p} at 4kHz		-82		
Total Harmonic Distortion Plus Noise	THD + N	V_{REF} = 850mV_{p-p} at 100kHz			0.024		%
DIGITAL INPUTS (SDI, SCK, $\overline{CS}$, $\overline{LDAC}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Leakage Current		V_{IN} = 0V or V_{DD}				1.0	µA
Input Capacitance (Note 2)						10	pF

ELECTRICAL CHARACTERISTICS—MAX537 (continued)

(V_{DD} = +5V, V_{SS} = -5V, REFAB/REFCD = 2.5V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL OUTPUT (SDO)							
Output High Voltage	V_{OH}	SDO sourcing 2mA		V_{DD} – 0.5	V_{DD} – 0.25		V
Output Low Voltage	V_{OL}	SDO sinking 2mA			0.13	0.40	V
DYNAMIC PERFORMANCE (R_L = 5kΩ, C_L = 100pF)							
Voltage-Output Slew Rate					5		V/µs
Output Settling Time		To ±½LSB of full scale			5		µs
Digital Feedthrough					5		nV-s
Digital Crosstalk (Note 3)					5		nV-s
POWER SUPPLIES							
Positive Supply Range	V_{DD}			4.5		5.5	V
Negative Supply Range	V_{SS}			-4.5		-5.5	V
Positive Supply Current (Note 4)	I_{DD}	T_A = +25°C			5.5	12	mA
		T_A = T_{MIN} to T_{MAX}				16	
Negative Supply Current (Note 4)	I_{SS}	T_A = +25°C			-4.7	-10	mA
		T_A = T_{MIN} to T_{MAX}				-14	
TIMING CHARACTERISTICS (Note 5)							
Internal Power-On Reset Pulse Width (Note 2)	t_{POR}					50	µs
SCK Clock Period	t_{CP}			100			ns
SCK Pulse Width High	t_{CH}	MAX537_C/E		35			ns
		MAX537_M		40			
SCK Pulse Width Low	t_{CL}	MAX537_C/E		35			ns
		MAX537_M		40			
$\overline{CS}$ Fall to SCK Rise Setup Time	t_{CSS}	MAX537_C/E		40			ns
		MAX537_M		50			
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}			0			ns
SDI Setup Time	t_{DS}	MAX537_C/E		40	24		ns
		MAX537_M		50			
SDI Hold Time	t_{DH}			0			ns
SCK Rise to SDO Valid Propagation Delay (Note 6)	t_{DO1}	C_{LOAD} = 50pF	MAX537_C/E		116	200	ns
			MAX537_M			230	
SCK Fall to SDO Valid Propagation Delay (Note 7)	t_{DO2}	C_{LOAD} = 50pF	MAX537_C/E		123	210	ns
			MAX537_M			250	

ELECTRICAL CHARACTERISTICS—MAX537 (continued)

(V_{DD} = +5V, V_{SS} = -5V, REFAB/REFCD = 2.5V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CS}$ Fall to SDO Enable	t_{DV}	C_{LOAD} = 50pF	MAX537_C/E		75	140	ns
			MAX537_M			170	
$\overline{CS}$ Rise to SDO Disable (Note 10)	t_{TR}	C_{LOAD} = 50pF	MAX537_C/E		70	130	ns
			MAX537_M			165	
SCK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	Continuous SCK, SCK edge ignored	MAX537_C/E	35			ns
			MAX537_M	40			
$\overline{CS}$ Rise to SCK Rise Hold Time	t_{CS1}	SCK edge ignored	MAX537_C/E	35			ns
			MAX537_M	40			
$\overline{LDAC}$ Pulse Width High	t_{LDAC}	MAX537_C/E		50			ns
		MAX537_M		70			
$\overline{CS}$ Pulse Width High	t_{CSW}	MAX537_C/E		100			ns
		MAX537_M		125			

Note 2: Guaranteed by design.
Note 3: Crosstalk is defined as the glitch energy at any DAC output in response to a full-scale step change on any other DAC.
Note 4: Digital inputs at 2.4V; with digital inputs at CMOS levels, I_{DD} decreases slightly.
Note 5: All input signals are specified with t_R = t_F ≤ 5ns. Logic input swing is 0V to 5V.
Note 6: Serial data clocked out of SDO on SCK's falling edge. (SDO is an open-drain output for the MAX536. The MAX537's SDO pin has an internal active pull-up.)
Note 7: Serial data clocked out of SDO on SCK's rising edge.
Note 10: When disabled, SDO is internally pulled high.

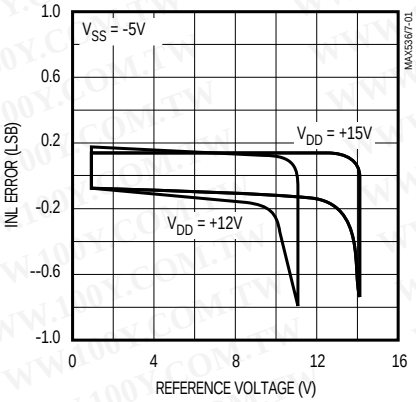
Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics

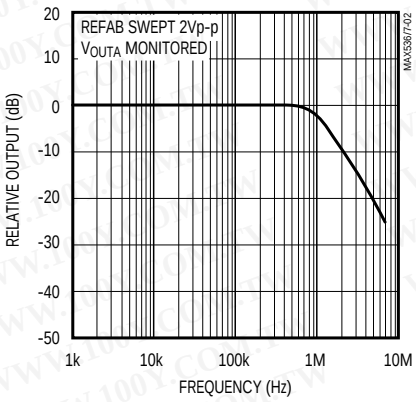
(T_A = +25°C, unless otherwise noted.)

MAX536

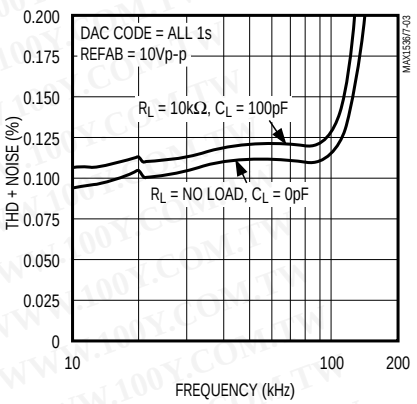
MAX536
INTEGRAL NONLINEARITY ERROR vs. REFERENCE VOLTAGE



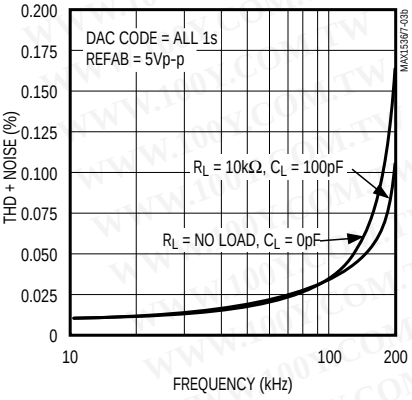
MAX536
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



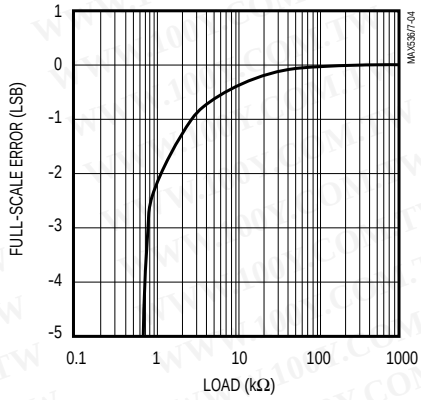
MAX536
TOTAL HARMONIC DISTORTION PLUS NOISE vs. REFERENCE FREQUENCY



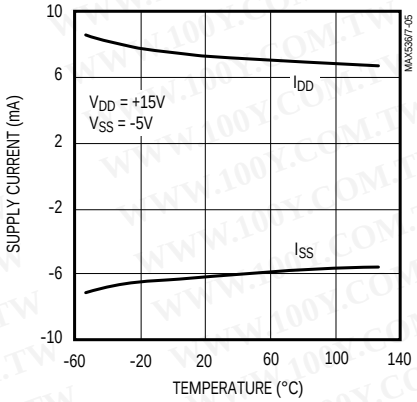
MAX536
TOTAL HARMONIC DISTORTION PLUS NOISE vs. REFERENCE FREQUENCY



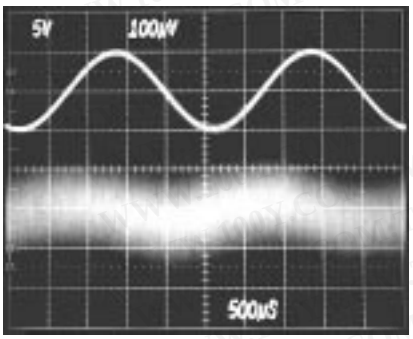
MAX536
FULL-SCALE ERROR vs. LOAD



MAX536
SUPPLY CURRENT vs. TEMPERATURE



MAX536
REFERENCE FEEDTHROUGH AT 400Hz



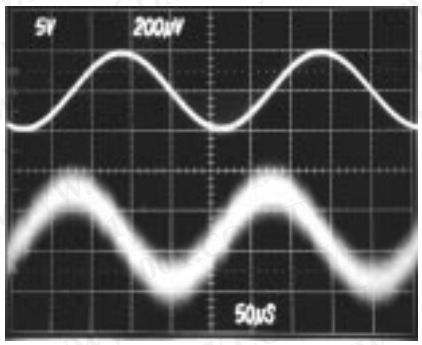
REFAB, 5V/div
0V

OUTA, 100µV/div

500µs/div

INPUT CODE = ALL 0s

MAX536
REFERENCE FEEDTHROUGH AT 4kHz



REFAB, 5V/div
0V

OUTA, 200µV/div

50µs/div

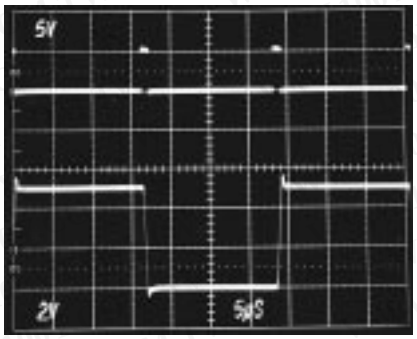
INPUT CODE = ALL 0s

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

MAX536

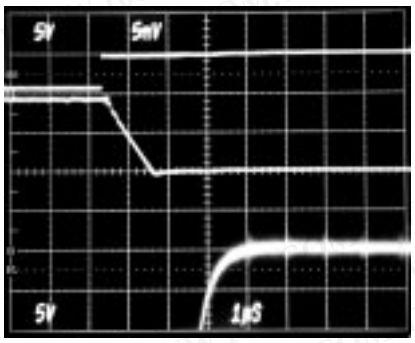
MAX536
DYNAMIC RESPONSE (ALL BITS ON, OFF, ON)



5µs/div

V_{DD} = +15V, V_{SS} = -5V, REFAB = 5V, C_L = 100pF, R_L = 10kΩ

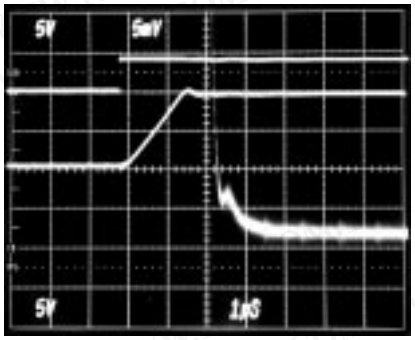
MAX536
NEGATIVE FULL-SCALE SETTLING TIME
(ALL BITS ON TO ALL BITS OFF)



1µs/div

V_{DD} = +15V, V_{SS} = -5V, REFAB = 10V, C_L = 100pF, R_L = 10kΩ

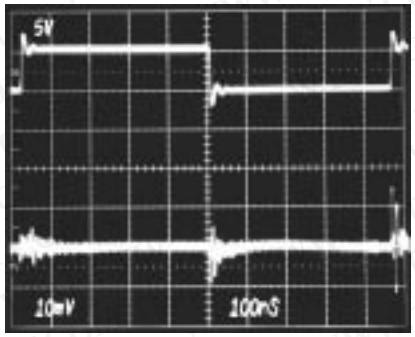
MAX536
POSITIVE FULL-SCALE SETTLING TIME
(ALL BITS OFF TO ALL BITS ON)



1µs/div

V_{DD} = +15V, V_{SS} = -5V, REFAB = 10V, C_L = 100pF, R_L = 10kΩ

MAX536
DIGITAL FEEDTHROUGH



V_{DD} = +15V, V_{SS} = -5V, REFAB = 10V, $\overline{CS}$ = HIGH,
DIN TOGGLING AT ½ THE CLOCK RATE,
OUTA = 5V

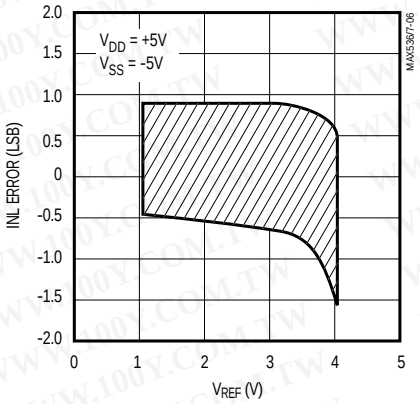
Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

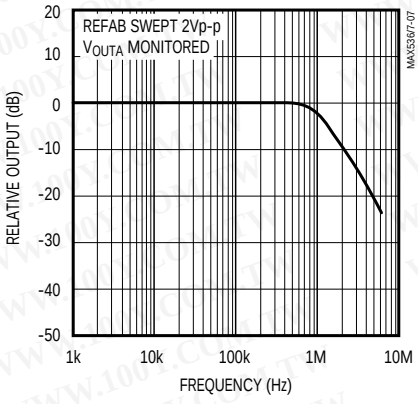
(T_A = +25°C, unless otherwise noted.)

MAX537

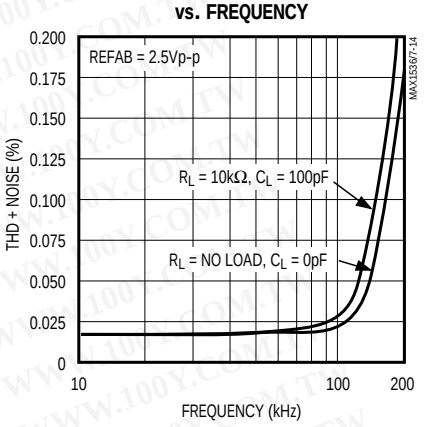
MAX537
INTEGRAL NONLINEARITY ERROR vs. REFERENCE VOLTAGE



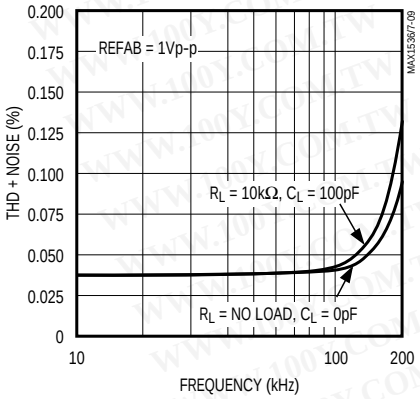
MAX537
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



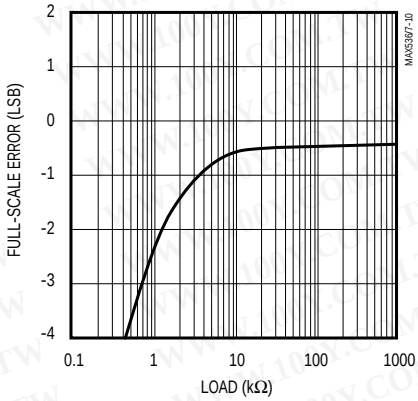
MAX537
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



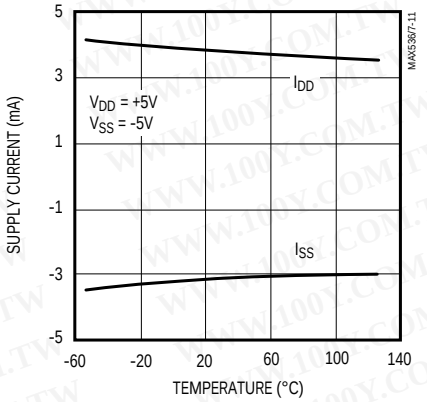
MAX537
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



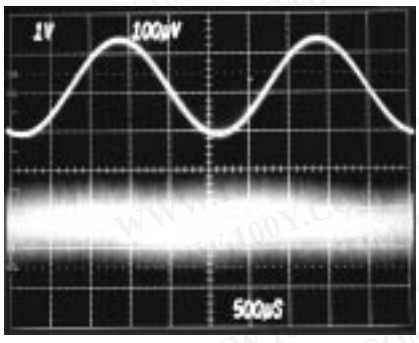
MAX537
FULL-SCALE ERROR vs. LOAD



MAX537
SUPPLY CURRENT vs. TEMPERATURE

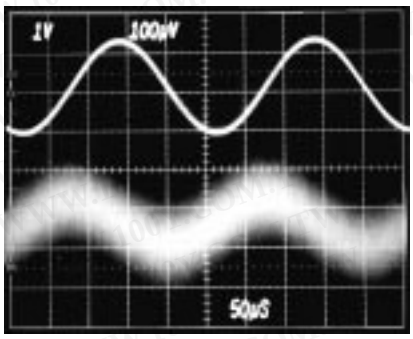


MAX537
REFERENCE FEEDTHROUGH AT 400Hz



REFAB, 1V/div
0V
OUTA, AC-COUPLED, 100µV/div
500µs/div
INPUT CODE = ALL 0s

MAX537
REFERENCE FEEDTHROUGH AT 4kHz



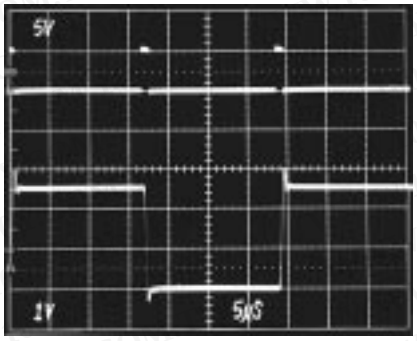
REFAB, 1V/div
0V
OUTA, AC-COUPLED, 100µV/div
50µs/div
INPUT CODE = ALL 0s

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

MAX537

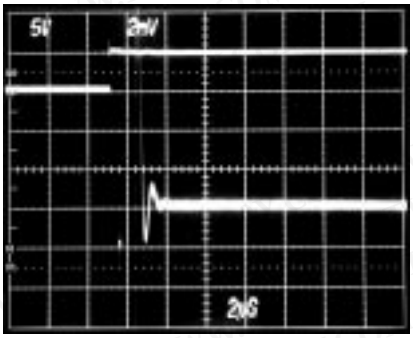
MAX537
DYNAMIC RESPONSE (ALL BITS ON, OFF, ON)



5µs/div

V_{DD} = +5V, V_{SS} = -5V, REFAB = 2.5V, C_L = 100pF, R_L = 10kΩ

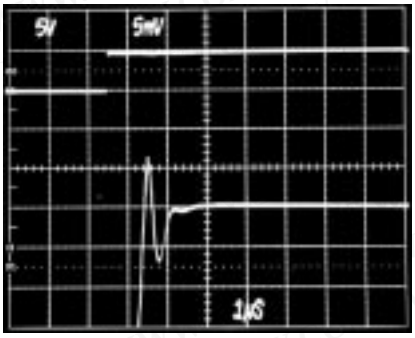
MAX537
NEGATIVE FULL-SCALE SETTLING TIME
(ALL BITS ON TO ALL BITS OFF)



1µs/div

V_{DD} = +5V, V_{SS} = -5V, REFAB = 2.5V, C_L = 100pF, R_L = 10kΩ

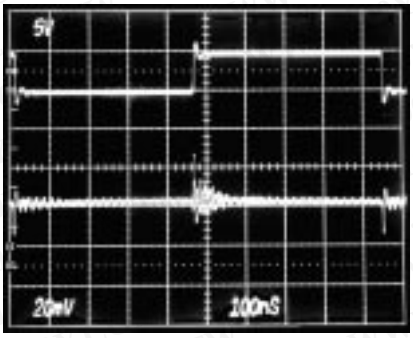
MAX537
POSITIVE FULL-SCALE SETTLING TIME
(ALL BITS OFF TO ALL BITS ON)



1µs/div

V_{DD} = +5V, V_{SS} = -5V, REFAB = 2.5V, C_L = 100pF, R_L = 10kΩ

MAX537
DIGITAL FEEDTHROUGH



100ns/div

V_{DD} = +5V, V_{SS} = -5V, REFAB = 2.5V, $\overline{CS}$ = HIGH,
DIN TOGGLING AT ½ THE CLOCK RATE,
OUTA = 1.25V

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Pin Description

PIN	NAME	FUNCTION
1	OUTB	DAC B Output Voltage
2	OUTA	DAC A Output Voltage
3	V_{SS}	Negative Power Supply
4	AGND	Analog Ground
5	REFAB	Reference Voltage Input for DAC A and DAC B
6	DGND	Digital Ground
7	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of all input registers to their respective DAC registers.
8	SDI	Serial Data Input. Data is shifted into an internal 16-bit shift register on SCK's rising edge.
9	$\overline{CS}$	Chip-Select Input (active low). A low level on $\overline{CS}$ enables the input shift register and SDO. On $\overline{CS}$'s rising edge, data is latched into the appropriate register(s).
10	SCK	Shift Register Clock Input
11	SDO	Serial Data Output. SDO is the output of the internal shift register. SDO is enabled when $\overline{CS}$ is low. For the MAX536, SDO is an open-drain output. For the MAX537, SDO has an active pull-up to V_{DD}.
12	REFCD	Reference Voltage Input for DAC C and DAC D
13	TP	Test Pin. Connect to V_{DD} for proper operation.
14	V_{DD}	Positive Power Supply
15	OUTD	DAC D Output Voltage
16	OUTC	DAC C Output Voltage

Detailed Description

The MAX536/MAX537 contain four 12-bit voltage-output DACs that are easily addressed using a simple 3-wire serial interface. They include a 16-bit data-in/data-out shift register, and each DAC has a double-buffered input composed of an input register and a DAC register (see the *Functional Diagram* on the front page).

The DACs are "inverted" R-2R ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference-voltage inputs. DAC A and DAC B share the REFAB reference input, while DAC C and DAC D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The REFAB/REFCD voltage range is 0V to (V_{DD} - 4V) for the MAX536 and 0V to (V_{DD} - 2.2V) for the MAX537. The output voltages $V_{OUT\_}$ are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = N_B \ (V_{REF}) / 4096$$

where N_B is the numeric value of the DAC's binary input code (0 to 4095) and V_{REF} is the reference voltage.

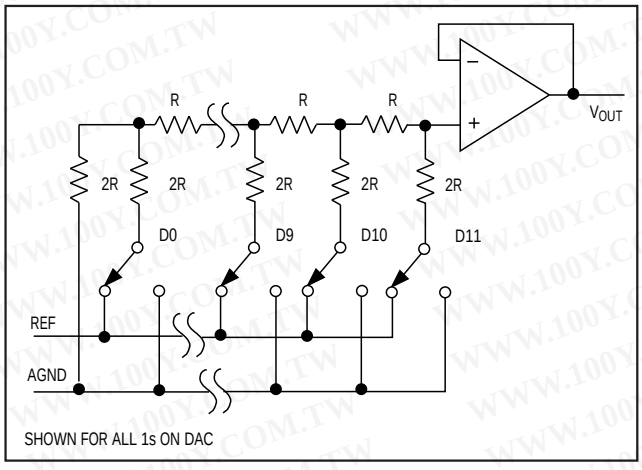


Figure 1. Simplified DAC Circuit Diagram

The input impedance at each reference input is code dependent, ranging from a low value of typically 6kΩ (with an input code of 0101 0101 0101) to a high value of 60kΩ (with an input code of 0000 0000 0000). Since the input impedance at the reference pins is code dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 5kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance becomes 2.5kΩ. A voltage reference with a load regulation of 0.001%/mA, such as the MAX674, would typically deviate by 0.164LSB (0.328LSB worst case) when simultaneously driving both MAX536 reference inputs at 10V.

An op amp, such as the MAX400 or OP07, can be used to buffer the reference to increase reference accuracy. The op amp's closed-loop output impedance should be kept below 0.05Ω to ensure an error of less than 0.08LSB. Reference accuracy is also improved by driving the REFAB and REFCD pins separately, or by using a reference with excellent accuracy and superior load regulation, such as the MAX676/MAX677/MAX678.

The reference input capacitance is also code dependent and typically ranges from 125pF to 300pF.

Output Buffer Amplifiers

All MAX536/MAX537 voltage outputs are internally buffered by precision unity-gain followers with a typical slew rate of 5V/µs for the MAX536 and 3V/µs for the MAX537.

With a full-scale transition at the MAX536 output (0V to 10V or 10V to 0V), the typical settling time to ±1/2LSB is 3µs when loaded with 5kΩ in parallel with 100pF (loads less than 5kΩ degrade performance).

With a full-scale transition at the MAX537 output (0V to 2.5V or 2.5V to 0V), the typical settling time to ±1/2LSB is 5µs when loaded with 5kΩ in parallel with 100pF (loads less than 5kΩ degrade performance).

Output dynamic responses and settling performances of the MAX536/MAX537 output amplifier are shown in the *Typical Operating Characteristics*.

Serial-Interface Configurations

The MAX536/MAX537's 3-wire or 4-wire serial interface is compatible with both Microwire (Figure 2) and SPI/QSPI (Figure 3). In Figures 2 and 3, $\overline{LDAC}$ can be tied either high or low for a 3-wire interface, or used as the fourth input with a 4-wire interface. The connection between SDO and the serial-interface port is not necessary, but may be used for data echo. (Data held in the shift register

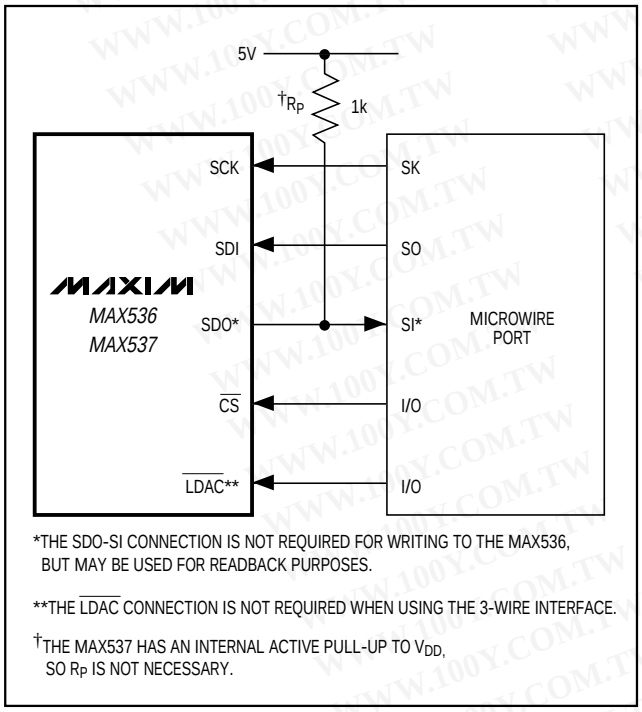


Figure 2. Connections for Microwire

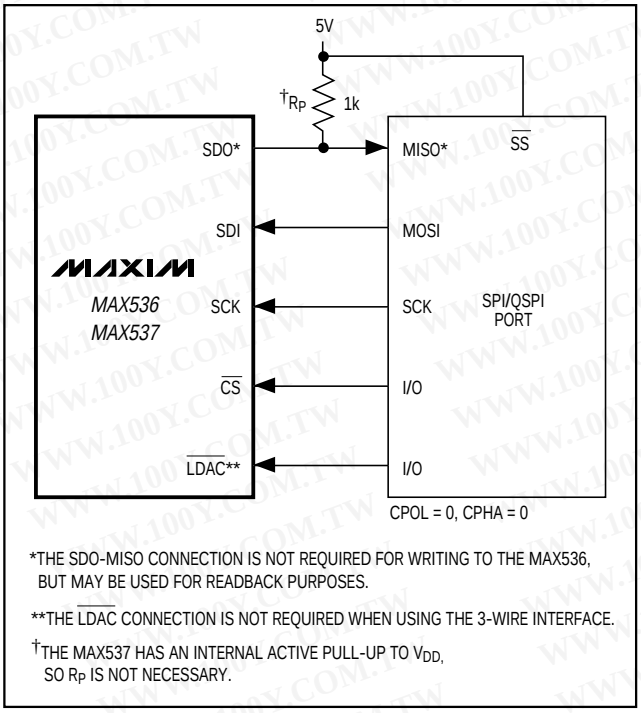


Figure 3. Connections for SPI/QSPI

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

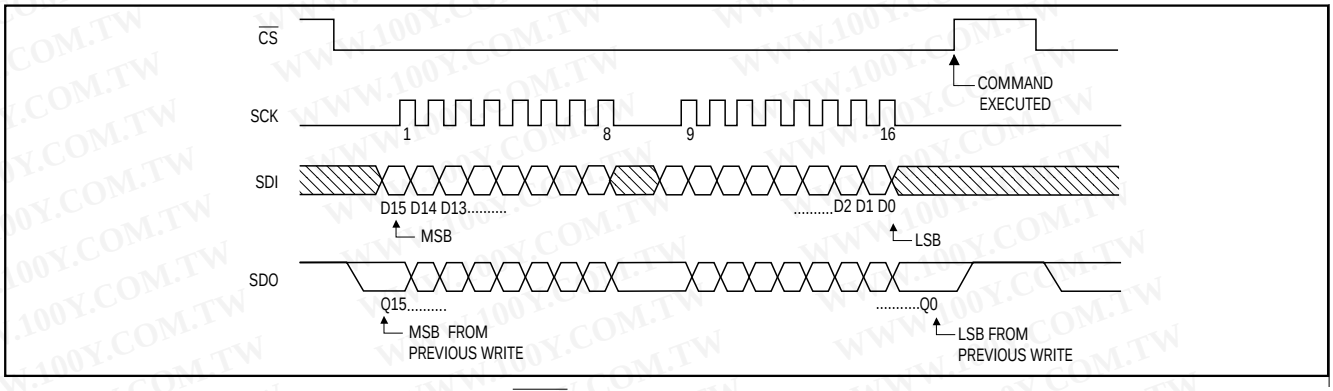


Figure 4. 3-Wire Serial-Interface Timing Diagram ($\overline{LDAC}$ = GND or V_{DD})

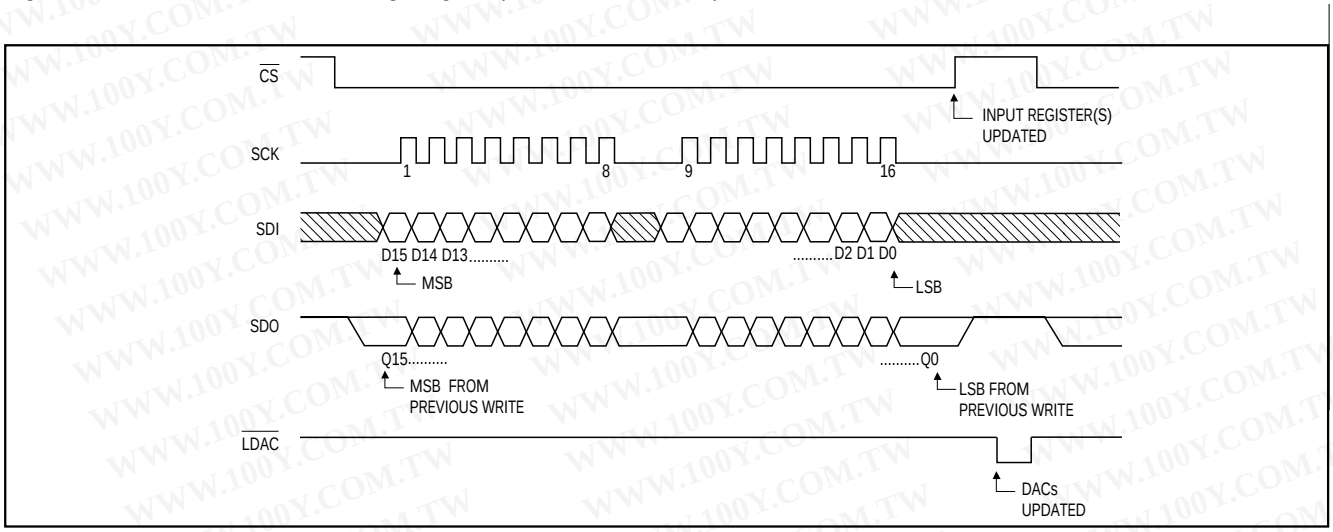


Figure 5. 4-Wire Serial-Interface Timing Diagram for Asynchronous DAC Updating Using $\overline{LDAC}$

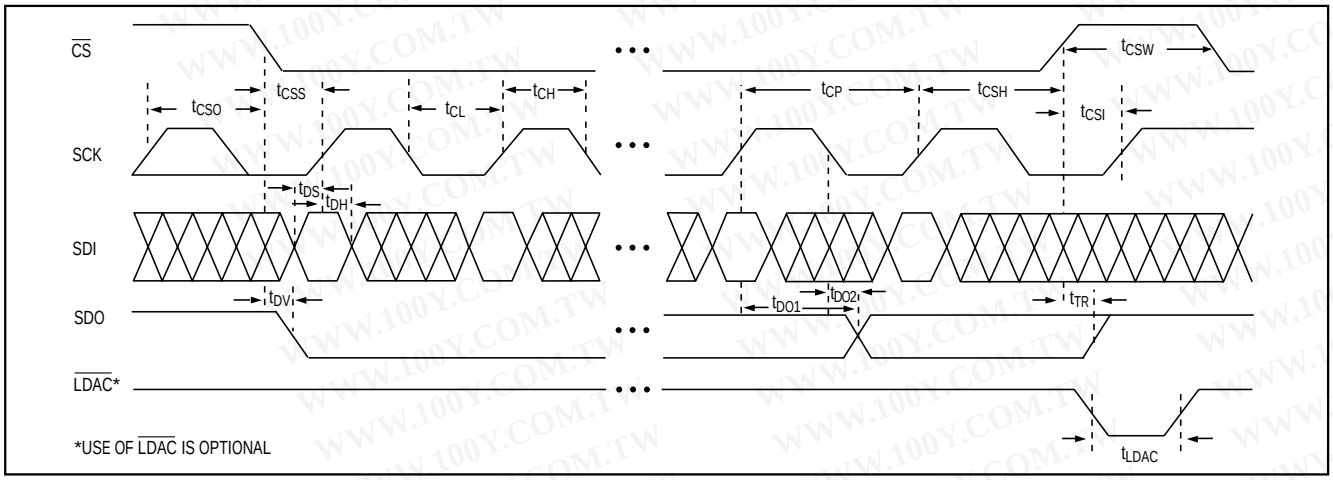


Figure 6. Detailed Serial-Interface Timing Diagram

of the MAX536/MAX537 can be shifted out of SDO and returned to the microprocessor for data verification; data in the MAX536/MAX537 input/DAC registers cannot be read.)

With a 3-wire interface ($\overline{CS}$, SCK, SDI) and $\overline{LDAC}$ tied high, the DACs are double-buffered. In this mode, depending on the command issued through the serial interface, the input register(s) may be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers may be simultaneously updated from the input registers. With a 3-wire interface ($\overline{CS}$, SCK, SDI) and $\overline{LDAC}$ tied low (Figure 4), the DAC registers remain transparent. Any time an input register is updated, the change appears at the DAC output with the rising edge of $\overline{CS}$.

The 4-wire interface ($\overline{CS}$, SCK, SDI, $\overline{LDAC}$) is similar to the 3-wire interface with $\overline{LDAC}$ tied high, except $\overline{LDAC}$ is a hardware input that simultaneously and asynchronously loads all DAC registers from their respective input registers when driven low (Figure 5).

Serial-Interface Description

The MAX536/MAX537 require 16 bits of serial data. Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0), two control bits (C1, C0), and the 12 data bits D11…D0 (Figure 7). The 4-bit address/control code determines the following: 1) the register(s) to be updated and/or the status of the input and DAC registers (i.e., whether they are in transparent or latch mode), and 2) the edge on which data is clocked out of SDO.

MSB ..... LSB			
◄ 16 Bits of Serial Data ►			
Address Bits		Control Bits	Data Bits MSB ..... LSB
A1	A0	C1 C0	D11 ..... D0
◄ 4 Address/ Control Bits ►			◄ 12 Data Bits ►

Figure 7. Serial-Data Format (MSB Sent First)

Figure 6 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled and the serial data output pin (SDO) is driven high (MAX537) or is a high-impedance open drain (MAX536). $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial data input pin (SDI) on SCK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX536/MAX537 input/DAC registers on $\overline{CS}$'s rising edge.

Interface timing is optimized when serial data is clocked out of the microcontroller/microprocessor on one clock edge and clocked into the MAX536/MAX537 on the other edge. Table 1 lists the serial-interface programming commands. For certain commands, the 12 data bits are "don't cares".

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The NOP (no operation) command allows the register contents to be unaffected and is useful when the MAX536/MAX537 are configured in a daisy-chain (see the *Daisy-Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of the MAX536/MAX537 SDO pin also loads data from all input registers to their respective DAC registers.

Serial-Data Output

The serial-data output, SDO, is the internal shift register's output. The MAX536/MAX537 can be programmed so that data is clocked out of SDO on SCK's rising (Mode 1) or falling (Mode 0) edge . In Mode 0, output data at SDO lags input data at SDI by 16.5 clock cycles, maintaining compatibility with Microwire, SPI/QSPI, and other serial interfaces. In Mode 1, output data lags input data by 16 clock cycles. On power-up, SDO defaults to Mode 1 timing.

For the MAX536, SDO is an open-drain output that should be pulled up to +5V. The data sheet timing specifications for SDO use a 1kΩ pull-up resistor. For the MAX537, SDO is a complementary output and does not require an external pull-up.

Test Pin

The test pin (TP) is used for pre-production analysis of the IC. **Connect TP to V_{DD} for proper MAX536/MAX537 operation. Failure to do so affects DAC operation**.

Daisy-Chaining Devices

Any number of MAX536/MAX537s can be daisy-chained by connecting the SDO pin of one device (with a pull-up resistor, if appropriate) to the SDI pin of the following device in the chain (Figure 8).

Since the MAX537's SDO pin has an internal active pull-up, the SDO sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial data out V_{OH} and V_{OL} specifications in the *Electrical Characteristics.*

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					LDAC	FUNCTION
A1	A0	C1	C0	D11...D0		
0	0	0	1	12-bit DAC data	1	Load DAC A input register; DAC output unchanged.
0	1	0	1	12-bit DAC data	1	Load DAC B input register; DAC output unchanged.
1	0	0	1	12-bit DAC data	1	Load DAC C input register; DAC output unchanged.
1	1	0	1	12-bit DAC data	1	Load DAC D input register; DAC output unchanged.
0	0	1	1	12-bit DAC data	1	Load input register A; all DAC registers updated.
0	1	1	1	12-bit DAC data	1	Load input register B; all DAC registers updated.
1	0	1	1	12-bit DAC data	1	Load input register C; all DAC registers updated.
1	1	1	1	12-bit DAC data	1	Load input register D; all DAC registers updated.
X	0	0	0	12-bit DAC data	X	Load all DACs from shift register.
X	1	0	0	XXXXXXXXXXXX	X	No operation (NOP)
0	X	1	0	XXXXXXXXXXXX	1	Update all DACs from their respective input registers.
1	1	1	0	XXXXXXXXXXXX	X	Mode 1 (default condition at power-up), DOUT clocked out on SCK's rising edge. All DACs updated from their respective input registers.
1	0	1	0	XXXXXXXXXXXX	X	Mode 0, DOUT clocked out on SCK's falling edge. All DACs updated from their respective input registers.
0	0	X	1	12-bit DAC data	0	Load DAC A input register; DAC A is immediately updated.
0	1	X	1	12-bit DAC data	0	Load DAC B input register; DAC B is immediately updated.
1	0	X	1	12-bit DAC data	0	Load DAC C input register; DAC C is immediately updated.
1	1	X	1	12-bit DAC data	0	Load DAC D input register; DAC D is immediately updated.

"X" = Don't Care. $\overline{LDAC}$ provides true latch control: when $\overline{LDAC}$ is low, the DAC registers are transparent; when $\overline{LDAC}$ is high, the DAC registers are latched.

When daisy-chaining MAX536s, the delay from $\overline{CS}$ low to SCK high (t_{CSS}) must be the greater of:

$$t_{DV} + t_{DS}$$

or

$$t_{TR} + t_{RC} + t_{DS} - t_{CSW}$$

where t_{RC} is the time constant of the external pull-up resistor (R_p) and the load capacitance (C) at SDO. For t_{RC} < 20ns, t_{CSS} is simply $t_{DV} + t_{DS}$. Calculate t_{RC} from the following equation:

$$t_{RC} = R_p (C) \left[\ln \left(\frac{V_{PULL\text{-}UP}}{V_{PULL\text{-}UP} - 2.4V} \right) \right]$$

where $V_{PULL\text{-}UP}$ is the voltage to which the pull-up resistor is connected.

Additionally, when daisy-chaining devices, the maximum clock frequency is limited to:

$$f_{SCK}(max) = \frac{1}{2\,(t_{DO} + t_{RC} - 38ns + t_{DS})}$$

For example, with t_{RC} = 23ns (5V ±10% supply with R_p = 1kΩ and C = 30pF), the maximum clock frequency is 8.7MHz.

Figure 9 shows an alternate method of connecting several MAX536/MAX537s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy-chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

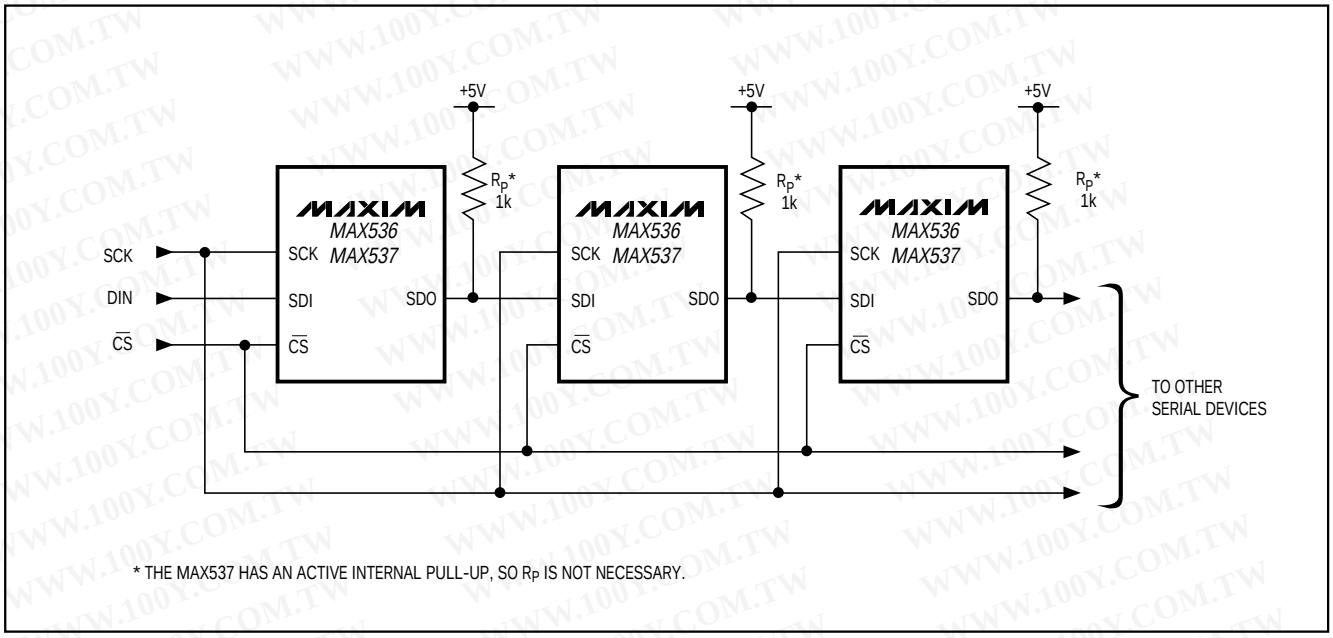


Figure 8. Daisy-Chaining MAX536/MAX537s with a 3-Wire Serial Interface

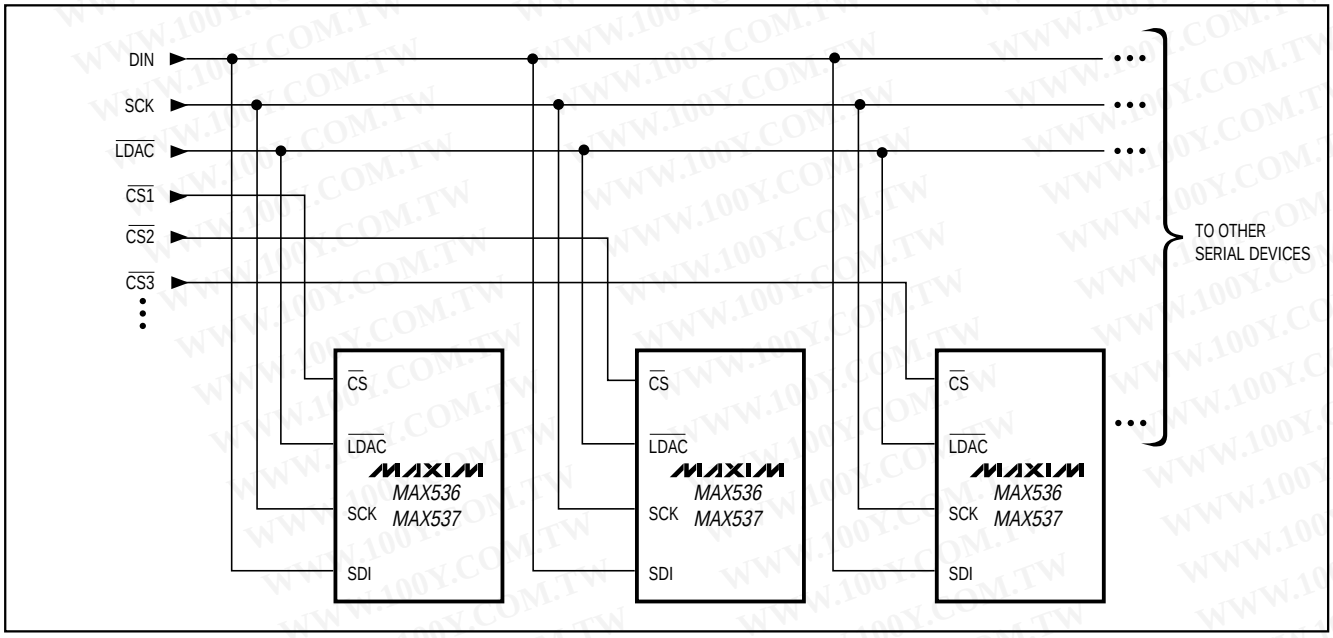


Figure 9. Multiple devices sharing a common DIN line may be simultaneously updated by bringing $\overline{LDAC}$ low. CS1, CS2, CS3… are driven separately, thus controlling which data are written to devices 1, 2, 3…

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Applications Information

Interfacing to the M68HC11*

PORT D of the 68HC11 supports SPI. The four registers used for SPI operation are the Serial Peripheral Control Register, the Serial Peripheral Status Register, the Serial Peripheral Data I/O Register, and PORT D's Data Direction Register. These registers have a default starting location of $1000.

On reset, the PORT D register (memory location $1008) is cleared and bits 5-0 are configured as general-purpose inputs. Setting bit 6 (SPE) of the Serial Peripheral Control Register (SPCR) configures PORT D for SPI as follows:

BIT							
7	6	5	4	3	2	1	0
NAME							
–	–	$\overline{SS}$	SCK	MOSI	MISO	TXD	RXD

Bits 6 and 7 are not used. Writes to these bits are ignored.

The PORT D Data Direction Register (DDRD) determines whether the port bits are inputs or outputs. Its configuration is shown below:

BIT							
7	6	5	4	3	2	1	0
NAME							
–	–	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0

Setting DDD_ = 0 configures the port bit as an input, while setting DDD_ = 1 configures the port bit as an output. Writes to bits 6 and 7 have no effect.

In SPI mode with MSTR = 1, when a PORT D bit is expected to be an input ($\overline{SS}$, MISO, RXD), the corresponding DDRD bit (DDD_) is ignored. If the bit is expected to be an output (SCK, MOSI, TXD), the corresponding DDRD bit must be set for the bit to be an output.

Table 2. Serial Peripheral Control-Register Definitions

NAME	DEFINITION		
SPIE	Serial Peripheral Interrupt Enable. Clearing SPIE disables the SPI hardware-interrupt request; the SPSR is polled to determine when an SPI data transfer is complete. Setting SPIE requests a hardware interrupt when the Serial Peripheral Status Register's SPIF bit or MODF bit is set.		
SPE	Setting SPE (Serial Peripheral System Enable) configures PORT D for SPI. Clearing SPE configures the port as a general-purpose I/O port.		
DWOM	When DWOM is set, the six PORT D outputs are open drain. When DWOM is cleared, the outputs are complementary.		
MSTR	Master/Slave select option		
CPOL	Determines clock polarity. When set, the serial clock idles high while data is not being transferred; when cleared, the clock idles low.		
CPHA	Determines the clock phase.		
SPR1/0	SPI Clock-Rate Select		
	SPR1	SPR0	
	0	0	µP clock divided by 2
	0	1	µP clock divided by 4
	1	0	µP clock divided by 16
	1	1	µP clock divided by 32

Table 3. Serial Peripheral Status-Register Definitions

NAME	DEFINITION
SPIF	SPIF is set when an SPI data transfer is complete. It is cleared by reading the SPSR and then accessing the SPDR.
WCOL	The Write Collision flag is set when a write to the SPDR occurs while a data transfer is in progress. It is cleared by reading the SPSR and then accessing the SPDR.
MODF	The Mode Fault flag detects master/slave conflicts in a multimaster environment. It is set when the "master" controller has its $\overline{SS}$ line (PORT D) pulled low, and cleared by reading the SPSR followed by a write to the SPCR.

*M68HC11 is a Motorola microcontroller. General information about the device was obtained from M68HC11 technical manuals.

Table 4. M68HC11 Programming Code

```
*****************************************************************************************************
* 68HC11 Programming Code for interfacing to the MAX536/MAX537 DACs.
* Data for the MAX536/MAX537 is stored in memory locations $0100 and $0101.
*
* Release Date February 24, 1994
* Revision 0
* Technical support provided by Motorola
* Additional assistance provided by Diane Scott
*****************************************************************************************************
*
*      68HC11 Code                    Instruction
*
STRT    EQU   $0000         ; Memory location for beginning of program
REGBLK  EQU   $1000         ; Starting address for 68HC11 register block
*
*  The following registers will be addressed relative to the start of the
*  register block (REGBLK) using indexed addressing mode.
*  The effective address = contents of Index Register X + offset.
*
PORTD   EQU   $08           ; PORT D memory location
DDRD    EQU   $09           ; PORT D Data Direction Register memory location
SPCR    EQU   $28           ; SPCR memory location
SPSR    EQU   $29           ; SPSR memory location
SPDR    EQU   $2A           ; SPDR memory location
*
*       Start of main program
*
MAIN    ORG   STRT
        LDAA #$74           ; an arbitrary MAX536/MAX537 DAC code (load input
        STAA $0100          ; register B with 1/4 of full-scale value; all DAC
        LDAA #$00           ; registers updated) is loaded into data memory
        STAA $0101          ; locations $0100 and $0101.
*
        LDX   #REGBLK       ; load Index Register X with starting address of register block
        LDAA  #$38          ; SPI outputs (SCK, MOSI, and /SS configured as an output)
*                           ; configured by setting the Data Direction Register bits
        STAA  DDRD,X        ; load data into the Data Direction Register
        LDAA  #$2F          ; set /SS and MOSI high; set SCK low
        STAA  PORTD,X       ; load data into PORTD to set-up SPI control lines
        LDAA  #$51          ; set data for SPCR
        STAA  SPCR,X        ; load data into the SPCR
        BCLR  PORTD,X $20   ; bring /CS low
        LDAA  $0100         ; load high byte of digital data into Accumulator(A)
        STAA  SPDR,X        ; load high byte of MAX536/MAX537 data into SPDR
WAIT1   LDAA  SPSR,X        ; beginning of loop to poll the SPSR
        BITA  #$80          ; mask all bits except SPIF (transfer complete) flag
        BEQ   WAIT1         ; branch if SPIF is not set to beginning of loop
        LDAA  $0101         ; load low byte of digital data into Accumulator(A)
        STAA  SPDR,X        ; load low byte of MAX536/MAX537 data into SPDR
WAIT2   LDAA  SPSR,X        ; beginning of loop to poll the SPSR
        BITA  #$80          ; mask all bits except SPIF (transfer complete) flag
        BEQ   WAIT2         ; branch if SPIF is not set to beginning of loop
        LDAA  SPDR,X        ; read the SPDR to clear the SPIF bit in the SPSR
        BSET  PORTD,X $20   ; bring /CS high to latch data into the MAX536/MAX537
*
* The MAX536/MAX537 is now configured to have V_OUTB = V_REF (1024/4096)
*
*****************************************************************************************************
```

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

$\overline{SS}$ is an input intended for use in a multimaster environment. However, $\overline{SS}$ or unused PORT D bit RXD, TXD, or possibly MISO (if DAC readback is not used) should be configured as a general-purpose output and used as $\overline{CS}$ by setting the appropriate Data Direction Register bit.

The SPCR configuration (memory location $1028) is shown below:

BIT	7	6	5	4	3	2	1	0
NAME	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
SETTING AFTER RESET	0	0	0	0	0	1	U*	U*
SETTING FOR TYPICAL SPI COMMUNICATION	0	1	0	1	0	0	0**	1**

*U = Unknown
**Depends on µP clock frequency.

Always configure the 68HC11 as the "master" controller and the MAX536/MAX537 as the "slave" device.

When MSTR = 1 in the SPCR, a write to the Serial Peripheral Data I/O Register (SPDR), located at memory location $102A, initiates the transmission/reception of data. The data transfer is monitored and the appropriate flags are set in the Serial Peripheral Status Register (SPSR).

The SPSR configuration is shown below:

BIT	7	6	5	4	3	2	1	0
NAME	SPIF	WCOL	–	MODF	–	–	–	–
RESET CONDITIONS	0	0	0	0	0	0	0	0

An example of 68HC11 programming code for a two-byte SPI transfer to the MAX536/MAX537 is given in Table 4. $\overline{SS}$ is used for $\overline{CS}$, the high byte of MAX536/MAX537 digital data is stored in memory location $0100, and the low byte is stored in memory location $0101.

Interfacing to Other Controllers

When using Microwire, refer to the section on *Interfacing to the M68HC11* for guidance, since Microwire can be considered similar to SPI when CPOL = 0 and CPHA = 0. When interfacing to Intel's 80C51/80C31 microcontroller family, use bit-pushing to configure a desired port as the MAX536/MAX537 interface port. Bit-pushing involves arbitrarily assigning I/O port bits as interface control lines, and then writing to the port each time a signal transition is required.

Unipolar Output

For a unipolar output, the output voltages and the reference inputs are the same polarity. Figure 10 shows the MAX536/MAX537 unipolar output circuit, which is also the typical operating circuit. Table 5 lists the unipolar output codes.

Bipolar Output

The MAX536/MAX537 outputs can be configured for bipolar operation using Figure 11's circuit. One op amp and two resistors are required per DAC. With R1 = R2:

$$V_{OUT} = V_{REF}\,[(2N_B / 4096) - 1]$$

where N_B is the numeric value of the DAC's binary input code. Table 6 shows digital codes and corresponding output voltages for Figure 11's circuit.

Table 5. Unipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}\,(\frac{4095}{4096})$
1000	0000	0001	$+V_{REF}\,(\frac{2049}{4096})$
1000	0000	0000	$+V_{REF}\,(\frac{2048}{4096}) = \frac{+V_{REF}}{2}$
0111	1111	1111	$+V_{REF}\,(\frac{2047}{4096})$
0000	0000	0001	$+V_{REF}\,(\frac{1}{4096})$
0000	0000	0000	0V

Table 6. Bipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}\,(\frac{2047}{2048})$
1000	0000	0001	$+V_{REF}\,(\frac{1}{2048})$
1000	0000	0000	0V
0111	1111	1111	$-V_{REF}\,(\frac{1}{2048})$
0000	0000	0001	$-V_{REF}\,(\frac{2047}{2048})$
0000	0000	0000	$-V_{REF}\,(\frac{2048}{2048}) = -V_{REF}$

NOTE: 1LSB = $(V_{REF})\,(\frac{1}{4096})$

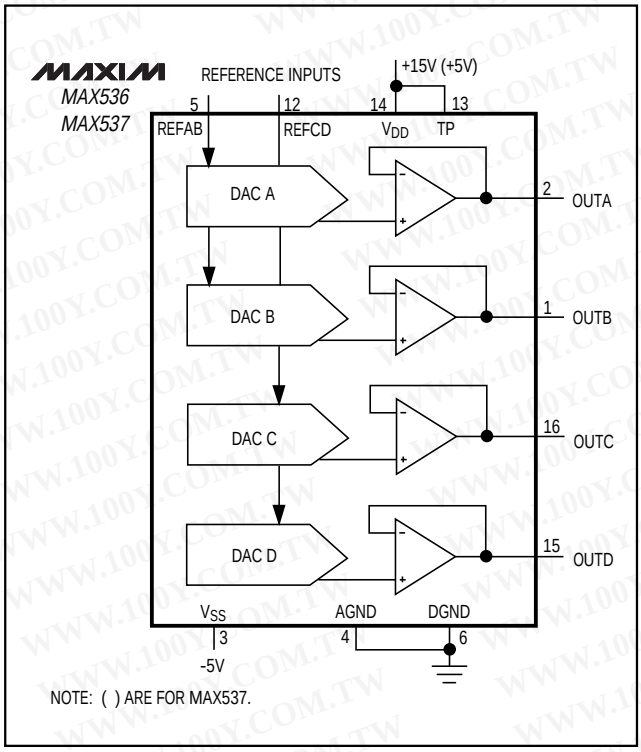


Figure 10. Unipolar Output Circuit

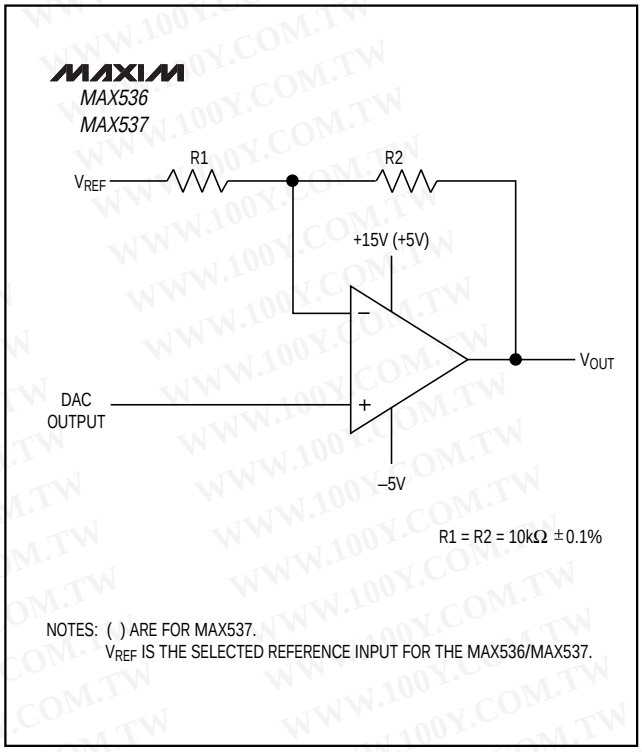


Figure 11. Bipolar Output Circuit

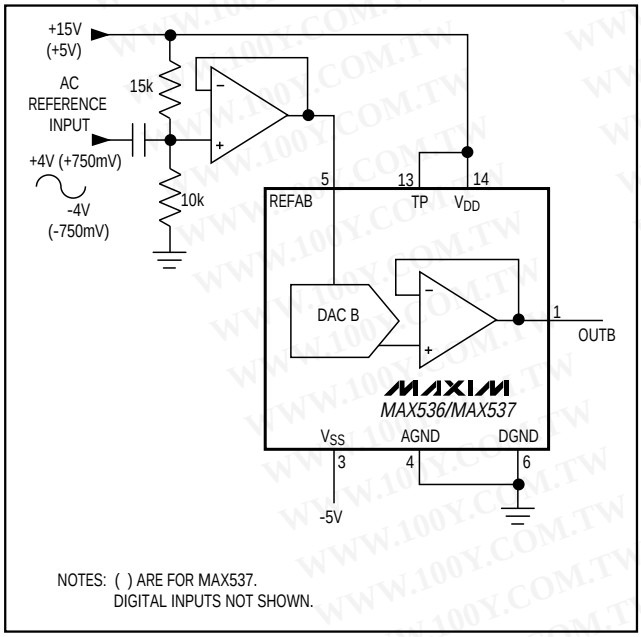


Figure 12. AC Reference Input Circuit

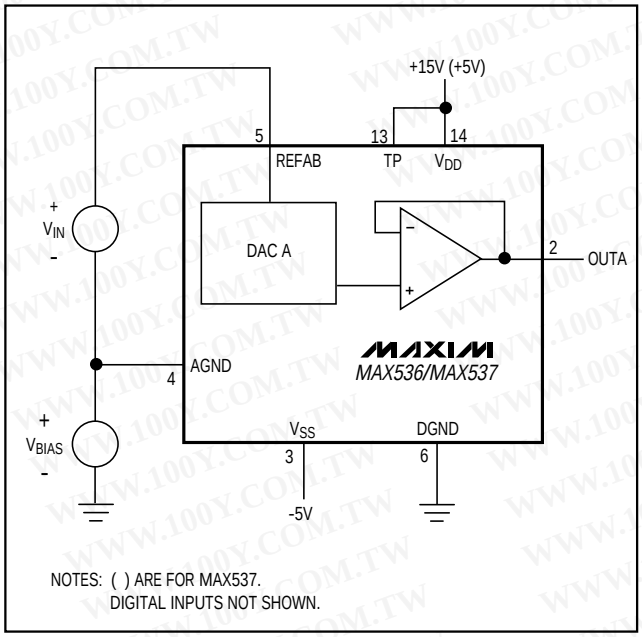


Figure 13. AGND Bias Circuit

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

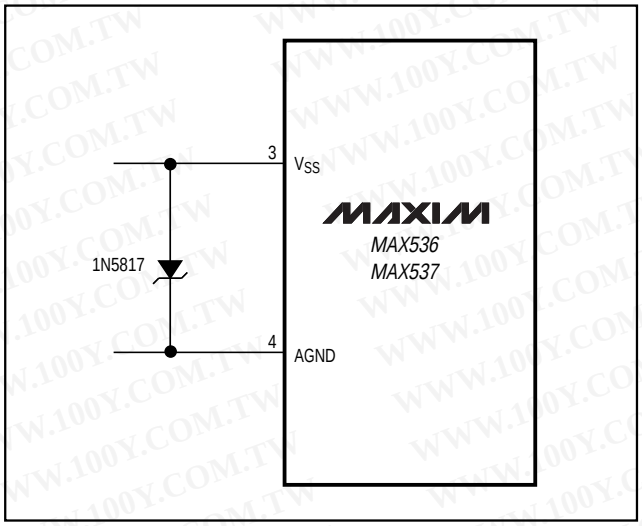


Figure 14. When V_{SS} and V_{DD} cannot be sequenced, tie a Schottky diode between V_{SS} and AGND.

Using an AC Reference

In applications where the reference has AC signal components, the MAX536/MAX537 have multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX536's total harmonic distortion plus noise (THD + N) is typically less than 0.012%, given a 5V_{p-p} signal swing and input frequencies up to 35kHz, or given a 2V_{p-p} swing and input frequencies up to 50kHz. The typical -3dB frequency is 700kHz as shown in the *Typical Operating Characteristics* graphs.

For the MAX537, with an input signal amplitude of 0.85mV_{p-p}, THD + N is typically less than 0.024% with a 5kΩ load in parallel with 100pF and input frequencies up to 100kHz, or with a 2kΩ load in parallel with 100pF and input frequencies up to 95kHz.

Offsetting AGND

AGND can be biased from DGND to the reference voltage to provide an arbitrary nonzero output voltage for a zero input code (Figure 13). The output voltage V_{OUTA} is:

$$V_{OUTA} = V_{BIAS} + N_B (V_{IN})$$

where V_{BIAS} is the positive offset voltage (with respect to DGND) applied to AGND, and N_B is the numeric value of the DAC's binary input code. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. As the voltage at AGND increases, the DAC's resolution decreases because its full-scale voltage swing is effectively reduced. AGND should not be biased more negative than DGND.

Power-Supply Considerations

On power-up, V_{SS} should come up first, V_{DD} next, then REFAB or REFCD. If supply sequencing is not possible, tie an external Schottky diode between V_{SS} and AGND as shown in Figure 14. On power-up, all input and DAC registers are cleared (set to zero code) and SDO is in Mode 0 (serial data is shifted out of SDO on the clock's rising edge).

For rated MAX536 performance, V_{DD} should be 4V higher than REFAB/REFCD and should be between 10.8V and 16.5V. When using the MAX537, V_{DD} should be at least 2.2V higher than REFAB/REFCD and should be between 4.75V and 5.5V. Bypass both V_{DD} and V_{SS} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest quality ground available.

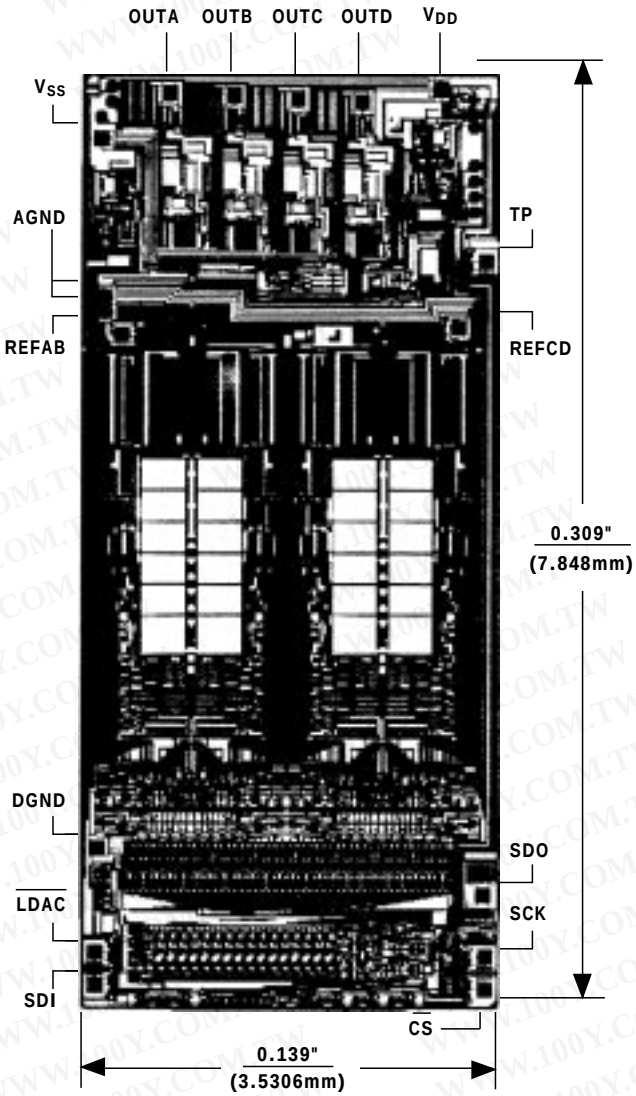
Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX537ACPE	0°C to +70°C	16 Plastic DIP	±½
MAX537BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX537ACWE	0°C to +70°C	16 Wide SO	±½
MAX537BCWE	0°C to +70°C	16 Wide SO	±1
MAX537BC/D	0°C to +70°C	Dice*	±1
MAX537AEPE	-40°C to +85°C	16 Plastic DIP	±½
MAX537BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX537AEWE	-40°C to +85°C	16 Wide SO	±½
MAX537BEWE	-40°C to +85°C	16 Wide SO	±1
MAX537AMDE	-55°C to +125°C	16 Ceramic SB**	±½
MAX537BMDE	-55°C to +125°C	16 Ceramic SB**	±1

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

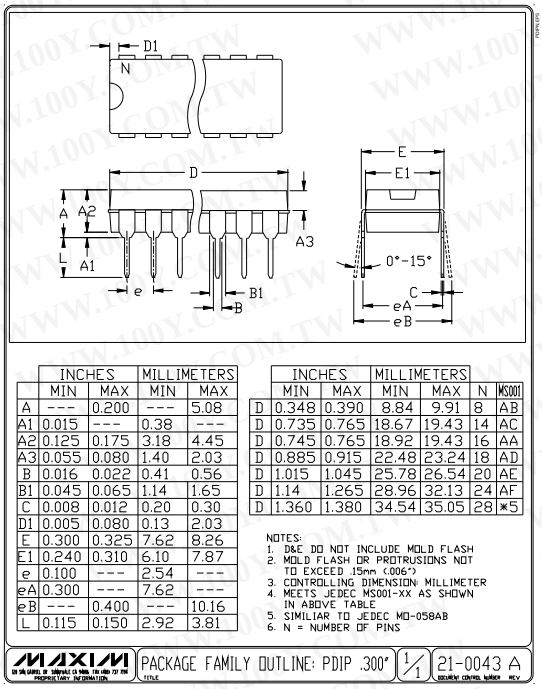
Chip Topography



TRANSISTOR COUNT: 5034
SUBSTRATE CONNECTED TO V_{DD}

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Package Information

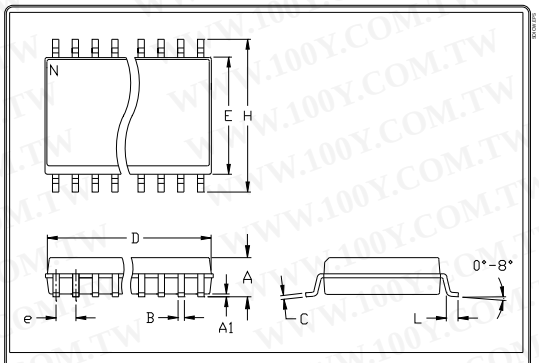


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .300" | 1/1 | 21-0042 A