LPC2212/LPC2214

16/32-bit ARM microcontrollers; 128/256 kB ISP/IAP Flash with 10-bit ADC and external memory interface

Rev. 02 — 23 December 2004 Product data

1. General description

The LPC2212/LPC2214 are based on a 16/32 bit ARM7TDMI-S™ CPU with real-time emulation and embedded trace support, together with 128/256 kilobytes (kB) of embedded high speed flash memory. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at maximum clock rate. For critical code size applications, the alternative 16-bit Thumb® Mode reduces code by more than 30 % with minimal performance penalty.

With their 144 pin package, low power consumption, various 32-bit timers, 8-channel 10-bit ADC, PWM channels and up to 9 external interrupt pins these microcontrollers are particularly suitable for industrial control, medical systems, access control and point-of-sale. Number of available GPIOs ranges from 76 (with external memory) through 112 pins (single-chip). With a wide range of serial communications interfaces, they are also very well suited for communication gateways, protocol converters and embedded soft modems as well as many other general-purpose applications.

2. Features

2.1 Key features

- 16/32-bit ARM7TDMI-S microcontroller in a LQFP144 package.
- 16 kB on-chip Static RAM and 128/256 kB on-chip Flash Program Memory. 128-bit wide interface/accelerator enables high speed 60 MHz operation.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip boot-loader software. Flash programming takes 1 ms per 512 byte line. Single sector or full chip erase takes 400 ms.
- EmbeddedICE-RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor™ software as well as high speed real-time tracing of instruction execution.
- Eight channel 10-bit A/D converter with conversion time as low as 2.44 µs.
- Two 32-bit timers (with 4 capture and 4 compare channels), PWM unit (6 outputs), Real Time Clock and Watchdog.
- Multiple serial interfaces including two UARTs (16C550), Fast I²C (400 kbits/s) and two SPIs.
- Vectored Interrupt Controller with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 Mb and 8/16/32 bit data width.
- Up to 112 general purpose I/O pins (5 V tolerant). Up to 9 edge or level sensitive external interrupt pins available.

- 60 MHz maximum CPU clock available from programmable on-chip Phase-Locked Loop with settling time of 100 μs.
- On-chip crystal oscillator with an operating range of 1 MHz to 30 MHz.
- Two low power modes, Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads. 16/32-bit ARM7TDMI-S processor.

3. Ordering information

Table 1: Ordering information

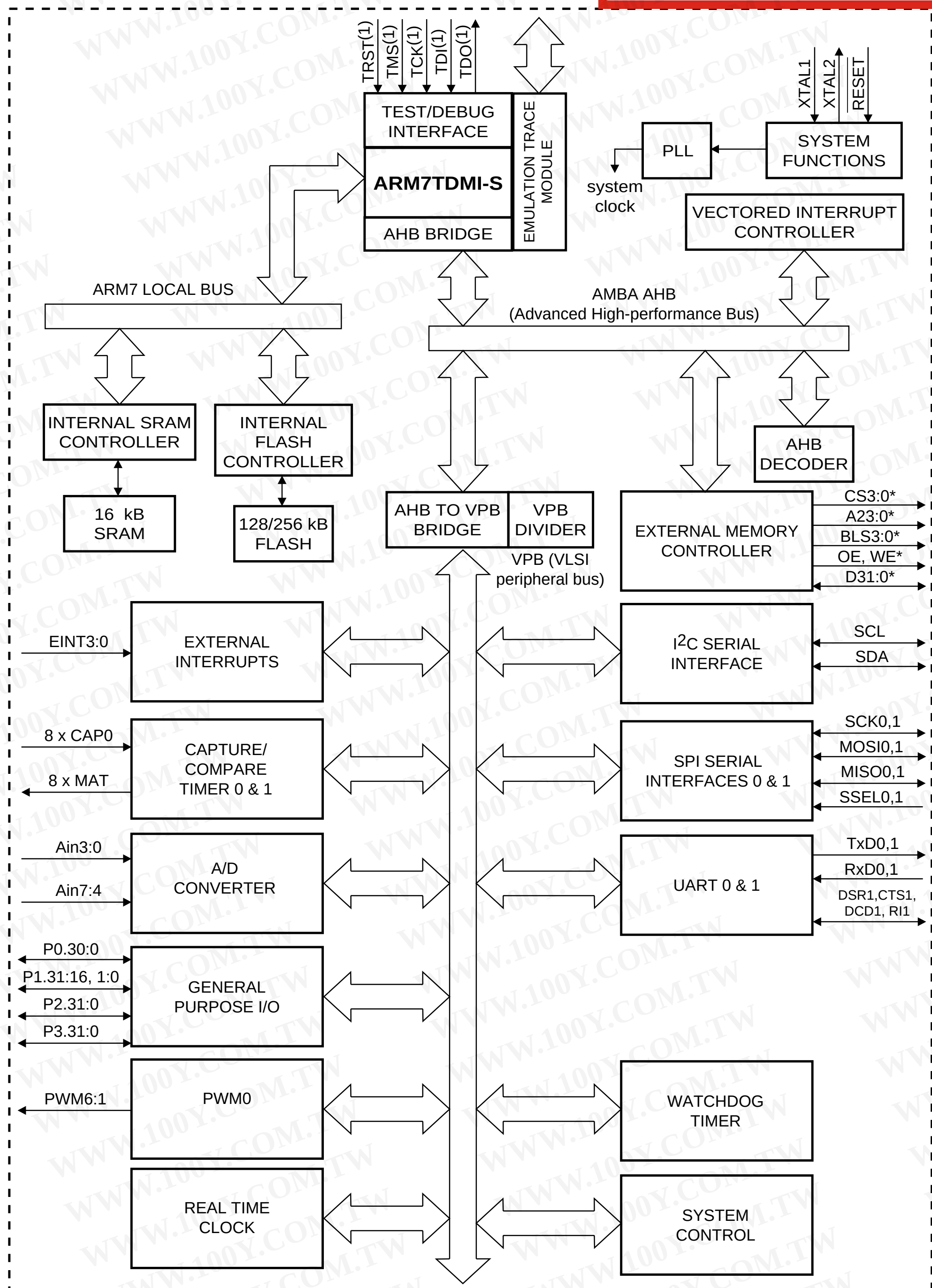
Type number	Package		
	Name	Description	Version
LPC2212FBD144	LQFP144	plastic low-profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2214FBD144	LQFP144	plastic low-profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

3.1 Ordering options

Table 2: Part options

Type number	Flash memory	RAM	CAN	Temperature range (°C)
LPC2212FBD144	128 kB	16 kB	-	–40 to +85
LPC2214FBD144	256 kB	16 kB	-	–40 to +85

4. Block diagram



*Shared with GPIO

(1) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

Fig 1. Block diagram.

5. Pinning information

5.1 Pinning

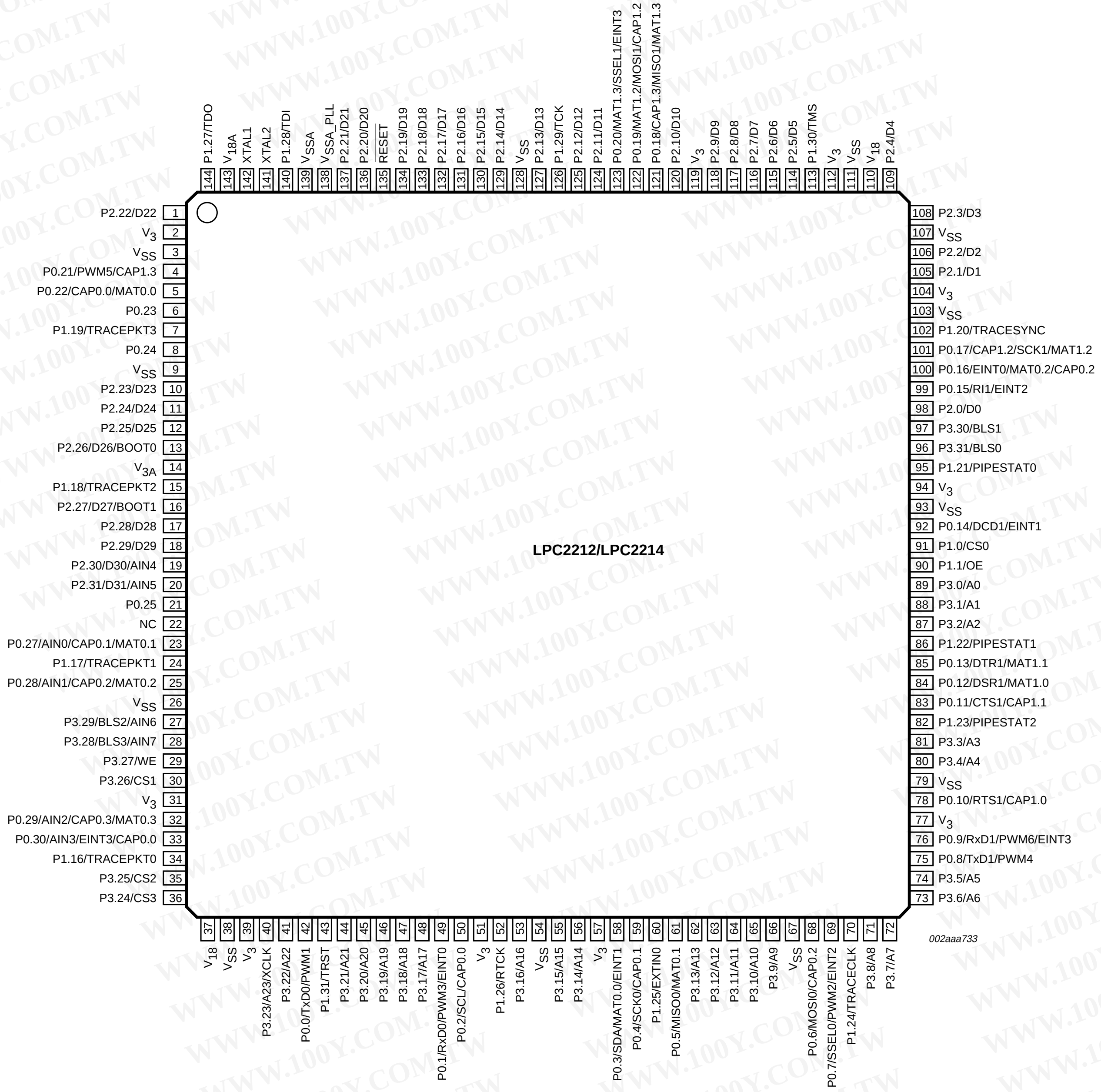


Fig 2. LQFP144 pinning.

5.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit bi-directional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0.0	42	O	**TxD0** — Transmitter output for UART0.
		O	**PWM1** — Pulse Width Modulator output 1.
P0.1	49	I	**RxD0** — Receiver input for UART0.
		O	**PWM3** — Pulse Width Modulator output 3.
		I	**EINT0** — External interrupt 0 input
P0.2	50	I/O	**SCL** — I^2C clock input/output. Open drain output (for I^2C compliance).
		I	**CAP0.0** — Capture input for Timer0, channel 0.
P0.3	58	I/O	**SDA** — I^2C data input/output. Open drain output (for I^2C compliance).
		O	**MAT0.0** — Match output for Timer0, channel 0.
		I	**EINT1** — External interrupt 1 input.
P0.4	59	I/O	**SCK0** — Serial clock for SPI0. SPI™ clock output from master or input to slave.
		I	**CAP0.1** — Capture input for Timer0, channel 1.
P0.5	61	I/O	**MISO0** — Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1** — Match output for Timer0, channel 1.
P0.6	68	I/O	**MOSI0** — Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2** — Capture input for Timer0, channel 2.
P0.7	69	I	**SSEL0** — Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2** — Pulse Width Modulator output 2.
		I	**EINT2** — External interrupt 2 input.
P0.8	75	O	**TxD1** — Transmitter output for UART1.
		O	**PWM4** — Pulse Width Modulator output 4.
P0.9	76	I	**RxD1** — Receiver input for UART1.
		O	**PWM6** — Pulse Width Modulator output 6.
		I	**EINT3** — External interrupt 3 input.
P0.10	78	O	**RTS1** — Request to Send output for UART1.
		I	**CAP1.0** — Capture input for Timer1, channel 0.
P0.11	83	I	**CTS1** — Clear to Send input for UART1.
		I	**CAP1.1** — Capture input for Timer1, channel 1.
P0.12	84	I	**DSR1** — Data Set Ready input for UART1.

Table 3: Pin description...*continued*

Symbol	Pin	Type	Description
		O	**MAT1.0** — Match output for Timer1, channel 0.
P0.13	85	O	**DTR1** — Data Terminal Ready output for UART1.
		O	**MAT1.1** — Match output for Timer1, channel 1.
P0.14	92	I	**DCD1** — Data Carrier Detect input for UART1.
		I	**EINT1** — External interrupt 1 input.
			Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip boot-loader to take over control of the part after reset.
P0.15	99	I	**RI1** — Ring Indicator input for UART1.
		I	**EINT2** — External interrupt 2 input.
P0.16	100	I	**EINT0** — External interrupt 0 input.
		O	**MAT0.2** — Match output for Timer0, channel 2.
		I	**CAP0.2** — Capture input for Timer0, channel 2.
P0.17	101	I	**CAP1.2** — Capture input for Timer1, channel 2.
		I/O	**SCK1** — Serial Clock for SPI1. SPI clock output from master or input to slave.
		O	**MAT1.2** — Match output for Timer1, channel 2.
P0.18	121	I	**CAP1.3** — Capture input for Timer1, channel 3.
		I/O	**MISO1** — Master In Slave Out for SPI1. Data input to SPI master or data output from SPI slave.
		O	**MAT1.3** — Match output for Timer1, channel 3.
P0.19	122	O	**MAT1.2** — Match output for Timer1, channel 2.
		I/O	**MOSI1** — Master Out Slave In for SPI1. Data output from SPI master or data input to SPI slave.
		I	**CAP1.2** — Capture input for Timer1, channel 2.
P0.20	123	O	**MAT1.3** — Match output for Timer1, channel 3.
		I	**SSEL1** — Slave Select for SPI1. Selects the SPI interface as a slave.
		I	**EINT3** — External interrupt 3 input.
P0.21	4	O	**PWM5** — Pulse Width Modulator output 5.
		I	**CAP1.3** — Capture input for TIMER1, channel 3.
P0.22	5	I	**CAP0.0** — Capture input for Timer0, channel 0.
		O	**MAT0.0** — Match output for Timer0, channel 0.
P0.23	6	I/O	General purpose bidirectional digital port only.
P0.24	8	I/O	General purpose bidirectional digital port only.
P0.25	21	I/O	General purpose bidirectional digital port only.
P0.27	23	I	**AIN0** — A/D converter, input 0. This analog input is always connected to its pin.
		I	**CAP0.1** — Capture input for Timer0, channel 1.
		O	**MAT0.1** — Match output for Timer0, channel 1.

Table 3: Pin description *…continued*

Symbol	Pin	Type	Description
P0.28	25	I	**AIN1** — A/D converter, input 1. This analog input is always connected to its pin.
		I	**CAP0.2** — Capture input for Timer0, channel 2.
		O	**MAT0.2** — Match output for Timer0, channel 2.
P0.29	32	I	**AIN2** — A/D converter, input 2. This analog input is always connected to its pin.
		I	**CAP0.3** — Capture input for Timer0, Channel 3.
		O	**MAT0.3** — Match output for Timer0, channel 3.
P0.30	33	I	**AIN3** — A/D converter, input 3. This analog input is always connected to its pin.
		I	**EINT3** — External interrupt 3 input.
		I	**CAP0.0** — Capture input for Timer0, channel 0.
P1.0 to P1.31		I/O	**Port 1:** Port 1 is a 32-bit bi-directional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 0 through 15 of port 1 are not available.
P1.0	91	O	**CS0** — Low-active Chip Select 0 signal. (Bank 0 addresses range 8000 0000 - 80FF FFFF)
P1.1	90	O	**OE** — Low-active Output Enable signal.
P1.16	34	O	**TRACEPKT0** — Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1.17	24	O	**TRACEPKT1** — Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1.18	15	O	**TRACEPKT2** — Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1.19	7	O	**TRACEPKT3** — Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1.20	102	O	**TRACESYNC** — Trace Synchronization. Standard I/O port with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1.25:16 to operate as Trace port after reset.
P1.21	95	O	**PIPESTAT0** — Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1.22	86	O	**PIPESTAT1** — Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1.23	82	O	**PIPESTAT2** — Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1.24	70	O	**TRACECLK** — Trace Clock. Standard I/O port with internal pull-up.
P1.25	60	I	**EXTIN0** — External Trigger Input. Standard I/O with internal pull-up.
P1.26	52	I/O	**RTCK** — Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bi-directional pin with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1.31:26 to operate as Debug port after reset.
P1.27	144	O	**TDO** — Test Data out for JTAG interface.
P1.28	140	I	**TDI** — Test Data in for JTAG interface.
P1.29	126	I	**TCK** — Test Clock for JTAG interface.
P1.30	113	I	**TMS** — Test Mode Select for JTAG interface.
P1.31	43	I	**$\overline{\text{TRST}}$** — Test Reset for JTAG interface.

Table 3: Pin description...*continued*

Symbol	Pin	Type	Description
P2.0 to P2.31		I/O	**Port 2** — Port 2 is a 32-bit bi-directional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2.0	98	I/O	**D0** — External memory data line 0.
P2.1	105	I/O	**D1** — External memory data line 1.
P2.2	106	I/O	**D2** — External memory data line 2.
P2.3	108	I/O	**D3** — External memory data line 3.
P2.4	109	I/O	**D4** — External memory data line 4.
P2.5	114	I/O	**D5** — External memory data line 5.
P2.6	115	I/O	**D6** — External memory data line 6.
P2.7	116	I/O	**D7** — External memory data line 7.
P2.8	117	I/O	**D8** — External memory data line 8.
P2.9	118	I/O	**D9** — External memory data line 9.
P2.10	120	I/O	**D10** — External memory data line 10.
P2.11	124	I/O	**D11** — External memory data line 11.
P2.12	125	I/O	**D12** — External memory data line 12.
P2.13	127	I/O	**D13** — External memory data line 13.
P2.14	129	I/O	**D14** — External memory data line 14.
P2.15	130	I/O	**D15** — External memory data line 15.
P2.16	131	I/O	**D16** — External memory data line 16.
P2.17	132	I/O	**D17** — External memory data line 17.
P2.18	133	I/O	**D18** — External memory data line 18.
P2.19	134	I/O	**D19** — External memory data line 19.
P2.20	136	I/O	**D20** — External memory data line 20.
P2.21	137	I/O	**D21** — External memory data line 21.
P2.22	1	I/O	**D22** — External memory data line 22.
P2.23	10	I/O	**D23** — External memory data line 23.
P2.24	11	I/O	**D24** — External memory data line 24.
P2.25	12	I/O	**D25** — External memory data line 25.
P2.26	13	I/O	**D26** — External memory data line 26.
		I	**BOOT0** — While $\overline{\text{RESET}}$ is low, together with BOOT1 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected.
P2.27	16	I/O	**D27** — External memory data line 27.
		I	**BOOT1** — While $\overline{\text{RESET}}$ is low, together with BOOT0 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected. BOOT1:0=00 selects 8-bit memory on CS0 for boot. BOOT1:0=01 selects 16-bit memory on CS0 for boot. BOOT1:0=10 selects 32-bit memory on CS0 for boot. BOOT1:0=11 selects Internal Flash memory.
P2.28	17	I/O	**D28** — External memory data line 28.

Table 3: Pin description *…continued*

Symbol	Pin	Type	Description
P2.29	18	I/O	**D29** — External memory data line 29.
P2.30	19	I/O	**D30** — External memory data line 30.
		I	**AIN4** — A/D converter, input 4. This analog input is always connected to its pin.
P2.31	20	I/O	**D31** — External memory data line 31.
		I	**AIN5** — A/D converter, input 5. This analog input is always connected to its pin.
P3.0 to P3.31		I/O	**Port 3** — Port 3 is a 32-bit bi-directional I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect Block.
P3.0	89	O	**A0** — External memory address line 0.
P3.1	88	O	**A1** — External memory address line 1.
P3.2	87	O	**A2** — External memory address line 2.
P3.3	81	O	**A3** — External memory address line 3.
P3.4	80	O	**A4** — External memory address line 4.
P3.5	74	O	**A5** — External memory address line 5.
P3.6	73	O	**A6** — External memory address line 6.
P3.7	72	O	**A7** — External memory address line 7.
P3.8	71	O	**A8** — External memory address line 8.
P3.9	66	O	**A9** — External memory address line 9.
P3.10	65	O	**A10** — External memory address line 10.
P3.11	64	O	**A11** — External memory address line 11.
P3.12	63	O	**A12** — External memory address line 12.
P3.13	62	O	**A13** — External memory address line 13.
P3.14	56	O	**A14** — External memory address line 14.
P3.15	55	O	**A15** — External memory address line 15.
P3.16	53	O	**A16** — External memory address line 16.
P3.17	48	O	**A17** — External memory address line 17.
P3.18	47	O	**A18** — External memory address line 18.
P3.19	46	O	**A19** — External memory address line 19.
P3.20	45	O	**A20** — External memory address line 20.
P3.21	44	O	**A21** — External memory address line 21.
P3.22	41	O	**A22** — External memory address line 22.
P3.23	40	O	**A23** — External memory address line 23.
		O	**XCLK** — Clock output.
P3.24	36	O	**CS3** — Low-active Chip Select 3 signal. (Bank 3 addresses range 8300 0000 - 83FF FFFF)
P3.25	35	O	**CS2** — Low-active Chip Select 2signal. (Bank 2 addresses range 8200 0000 - 82FF FFFF)
P3.26	30	O	**CS1** — Low-active Chip Select 1 signal. (Bank 1 addresses range 8100 0000 - 81FF FFFF)
P3.27	29	O	**WE** — Low-active Write enable signal.

Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
P3.28	28	O	**BLS3 —** Low-active Byte Lane Select signal (Bank 3).
		I	**AIN7 —** A/D converter, input 7. This analog input is always connected to its pin.
P3.29	27	O	**BLS2 —** Low-active Byte Lane Select signal (Bank 2).
		I	**AIN6 —** A/D converter, input 6. This analog input is always connected to its pin.
P3.30	97	O	**BLS1 —** Low-active Byte Lane Select signal (Bank 1).
P3.31	96	O	**BLS0 —** Low-active Byte Lane Select signal (Bank 0).
NC	22		Pin not connected.
$\overline{RESET}$	135	I	**External Reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	142	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	141	O	Output from the oscillator amplifier.
V_{SS}	3, 9, 26, 38, 54, 67, 79, 93, 103, 107, 111, 128	I	**Ground:** 0 V reference.
V_{SSA}	139	I	**Analog Ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
V_{SSA_PLL}	138	I	**PLL Analog Ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
V_{18}	37, 110	I	**1.8 V Core Power Supply:** This is the power supply voltage for internal circuitry.
V_{18A}	143	I	**Analog 1.8 V Core Power Supply:** This is the power supply voltage for internal circuitry. This should be nominally the same voltage as V_{18} but should be isolated to minimize noise and error.
V_3	2, 31, 39, 51, 57, 77, 94, 104, 112, 119	I	**3.3 V Pad Power Supply:** This is the power supply voltage for the I/O ports.
V_{3A}	14	I	Analog 3.3 V Pad Power Supply: This should be nominally the same voltage as V_3 but should be isolated to minimize noise and error.

6. Functional description

Details of the LPC2212/LPC2214 systems and peripheral functions are described in the following sections.

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM® architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-Chip Flash program memory

The LPC2212/LPC2214 incorporate a 128 kB and 256 kB Flash memory system respectively. This memory may be used for both code and data storage. Programming of the Flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the Flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When on-chip bootloader is used, 120/248 kB of Flash memory is available for user code.

The LPC2212/LPC2214 Flash memory provides a minimum of 100,000 erase/write cycles and 20 years of data retention.

On-chip bootloader (as of revision 1.60) provides Code Read Protection (CRP) for the LPC2212/LPC2214 on-chip Flash memory. When the CRP is enabled, the JTAG debug port, external memory boot and ISP commands accessing either the on-chip

RAM or Flash memory are disabled. However, the ISP Flash Erase command can be executed at any time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user Flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

6.3 On-Chip static RAM

On-Chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bits, 16-bits, and 32-bits. The LPC2212/LPC2214 provide 16 kB of static RAM.

6.4 Memory map

The LPC2212/LPC2214 memory maps incorporate several distinct regions, as shown in the following figures.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either Flash memory (the default) or on-chip static RAM. This is described in Section 6.20 "System control".

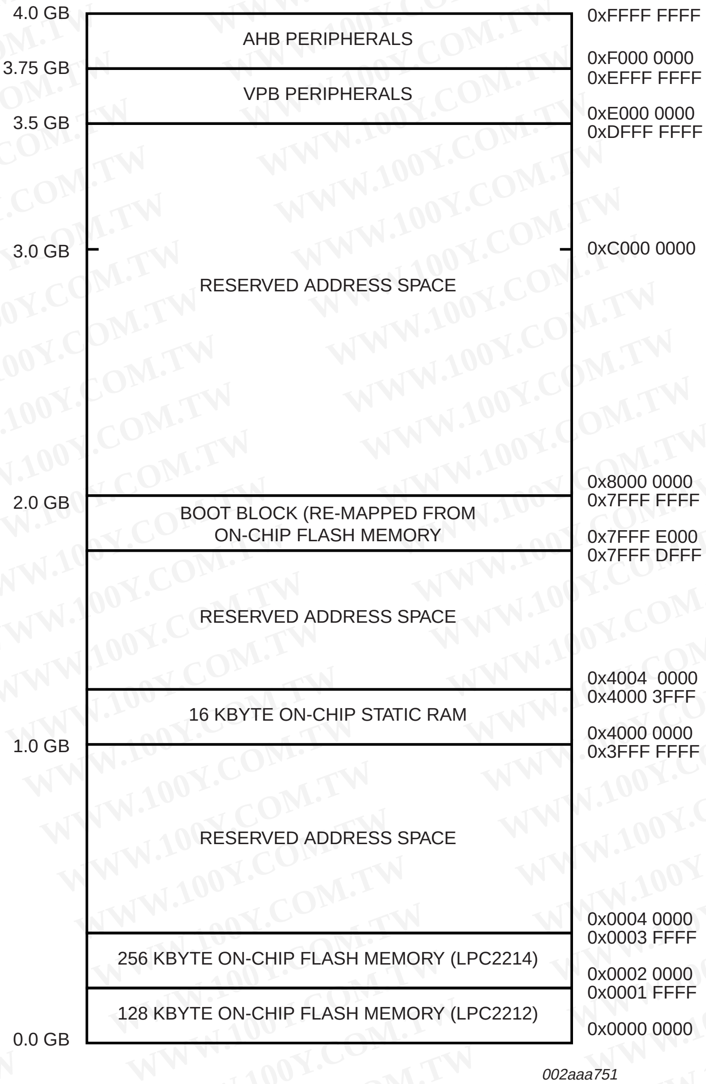


Fig 3. LPC2212/LPC2214 memory map.

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as FIQ, vectored IRQ, and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

Fast Interrupt reQuest (FIQ) has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 4 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 4: Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	Embedded ICE, DbgCommRx	2
ARM Core	Embedded ICE, DbgCommTx	3
Timer0	Match 0 - 3 (MR0, MR1, MR2, MR3)	4
Timer1	Match 0 - 3 (MR0, MR1, MR2, MR3)	5
UART0	Rx Line Status (RLS) Transmit Holding Register empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI)	6
UART1	Rx Line Status (RLS) Transmit Holding Register empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI) Modem Status Interrupt (MSI)	7
PWM0	Match 0 - 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I^2C	SI (state change)	9
SPI0	SPIF, MODF	10
SPI1	SPIF, MODF	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13

Table 4: Interrupt sources *...continued*

Block	Flag(s)	VIC channel #
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
A/D	A/D Converter	18

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The Pin Control Module contains three registers as shown in Table 5.

Table 5:

Address	Name	Description	Access
0xE002C000	PINSEL0	Pin function select register 0	Read/Write
0xE002C004	PINSEL1	Pin function select register 1	Read/Write
0xE002C014	PINSEL2	Pin function select register 2	Read/Write

6.7 Pin function select register 0 (PINSEL0 - 0xE002C000)

The PINSEL0 register controls the functions of the pins as per the settings listed in Table 6. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically. Settings other than those shown in Table 6 are reserved, and should not be used

Table 6: Pin function select register 0 (PINSEL0 - 0xE002C000)

PINSEL0	Pin name	Value		Function	Value after Reset
1:0	P0.0	0	0	GPIO Port 0.0	0
		0	1	TxD (UART0)	
		1	0	PWM1	
		1	1	Reserved	
3:2	P0.1	0	0	GPIO Port 0.1	0
		0	1	RxD (UART0)	
		1	0	PWM3	
		1	1	EINT0	
5:4	P0.2	0	0	GPIO Port 0.2	0
		0	1	SCL (I^2C)	
		1	0	Capture 0.0 (Timer0)	
		1	1	Reserved	

Table 6: Pin function select register 0 (PINSEL0 - 0xE002C000)...*continued*

PINSEL0	Pin name	Value		Function	Value after Reset
7:6	P0.3	0	0	GPIO Port 0.3	0
		0	1	SDA (I^2C)	
		1	0	Match 0.0 (Timer0)	
		1	1	EINT1	
9:8	P0.4	0	0	GPIO Port 0.4	0
		0	1	SCK (SPI0)	
		1	0	Capture 0.1 (Timer0)	
		1	1	Reserved	
11:10	P0.5	0	0	GPIO Port 0.5	0
		0	1	MISO (SPI0)	
		1	0	Match 0.1 (Timer0)	
		1	1	Reserved	
13:12	P0.6	0	0	GPIO Port 0.6	0
		0	1	MOSI (SPI0)	
		1	0	Capture 0.2 (Timer0)	
		1	1	Reserved	
15:14	P0.7	0	0	GPIO Port 0.7	0
		0	1	SSEL (SPI0)	
		1	0	PWM2	
		1	1	EINT2	
17:16	P0.8	0	0	GPIO Port 0.8	0
		0	1	TxD UART1	
		1	0	PWM4	
		1	1	Reserved	
19:18	P0.9	0	0	GPIO Port 0.9	0
		0	1	RxD (UART1)	
		1	0	PWM6	
		1	1	EINT3	
21:20	P0.10	0	0	GPIO Port 0.10	0
		0	1	RTS (UART1)	
		1	0	Capture 1.0 (Timer1)	
		1	1	Reserved	
23:22	P0.11	0	0	GPIO Port 0.11	0
		0	1	CTS (UART1)	
		1	0	Capture 1.1 (Timer1)	
		1	1	Reserved	
25:24	P0.12	0	0	GPIO Port 0.12	0
		0	1	DSR (UART1)	
		1	0	Match 1.0 (Timer1)	
		1	1	Reserved	

Table 6: Pin function select register 0 (PINSEL0 - 0xE002C000)...*continued*

PINSEL0	Pin name	Value		Function	Value after Reset
27:26	P0.13	0	0	GPIO Port 0.13	0
		0	1	DTR (UART1)	
		1	0	Match 1.1 (Timer1)	
		1	1	Reserved	
29:28	P0.14	0	0	GPIO Port 0.14	0
		0	1	DCD (UART1)	
		1	0	EINT1	
		1	1	Reserved	
31:30	P0.15	0	0	GPIO Port 0.15	0
		0	1	RI (UART1)	
		1	0	EINT2	
		1	1	Reserved	

6.8 Pin function select register 1 (PINSEL1 - 0xE002C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in Table 7. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in the table are reserved, and should not be used.

Table 7: Pin function select register 1 (PINSEL1 - 0xE002C004)

PINSEL1	Pin Name	Value		Function	Value after Reset
1:0	P0.16	0	0	GPIO Port 0.16	0
		0	1	EINT0	
		1	0	Match 0.2 (Timer0)	
		1	1	Capture 0.2 (Timer0)	
3:2	P0.17	0	0	GPIO Port 0.17	0
		0	1	Capture 1.2 (Timer1)	
		1	0	SCK (SPI1)	
		1	1	Match 1.2 (Timer1)	
5:4	P0.18	0	0	GPIO Port 0.18	0
		0	1	Capture 1.3 (Timer1)	
		1	0	MISO (SPI1)	
		1	1	Match 1.3 (Timer1)	
7:6	P0.19	0	0	GPIO Port 0.19	0
		0	1	Match 1.2 (Timer1)	
		1	0	MOSI (SPI1)	
		1	1	Capture 1.2 (Timer1)	
9:8	P0.20	0	0	GPIO Port 0.20	0
		0	1	Match 1.3 (Timer1)	
		1	0	SSEL (SPI1)	
		1	1	EINT3	

Table 7: Pin function select register 1 (PINSEL1 - 0xE002C004)...*continued*

PINSEL1	Pin Name	Value		Function	Value after Reset
11:10	P0.21	0	0	GPIO Port 0.21	0
		0	1	PWM5	
		1	0	Reserved	
		1	1	Capture 1.3 (Timer1)	
13:12	P0.22	0	0	GPIO Port 0.22	0
		0	1	Reserved	
		1	0	Capture 0.0 (Timer0)	
		1	1	Match 0.0 (Timer0)	
15:14	P0.23	0	0	GPIO Port 0.23	0
		0	1	Reserved	
		1	0	Reserved	
		1	1	Reserved	
17:16	P0.24	0	0	GPIO Port 0.24	0
		0	1	Reserved	
		1	0	Reserved	
		1	1	Reserved	
19:18	P0.25	0	0	GPIO Port 0.25	0
		0	1	Reserved	
		1	0	Reserved	
		1	1	Reserved	
21:20	P0.26	0	0	Reserved	0
		0	1	Reserved	
		1	0	Reserved	
		1	1	Reserved	
23:22	P0.27	0	0	GPIO Port 0.27	1
		0	1	AIN0 (A/D input 0)	
		1	0	Capture 0.1 (Timer0)	
		1	1	Match 0.1 (Timer0)	
25:24	P0.28	0	0	GPIO Port 0.28	1
		0	1	AIN1 (A/D input 1)	
		1	0	Capture 0.2 (Timer0)	
		1	1	Match 0.2 (Timer0)	
27:26	P0.29	0	0	GPIO Port 0.29	1
		0	1	AIN2 (A/D input 2)	
		1	0	Capture 0.3 (Timer0)	
		1	1	Match 0.3 (Timer0)	
29:28	P0.30	0	0	GPIO Port 0.30	1
		0	1	AIN3 (A/D input 0)	
		1	0	EINT3	
		1	1	Capture 0.0 (Timer0)	

Table 7: Pin function select register 1 (PINSEL1 - 0xE002C004)...*continued*

PINSEL1	Pin Name	Value		Function	Value after Reset
31:30	P0.31	0	0	Reserved	0
		0	1	Reserved	
		1	0	Reserved	
		1	1	Reserved	

6.9 Pin function select register 2 (PINSEL2 - 0xE002C014)

The PINSEL2 register controls the functions of the pins as per the settings listed in Table 8. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in the table are reserved, and should not be used.

Table 8: Pin function select register 2 (PINSEL2 - 0xE002C014)

PINSEL2 bits	Description	Reset value
1:0	Reserved.	-
2	When 0, pins P1.36:26 are used as GPIO pins. When 1, P1.31:26 are used as a Debug port.	P1.26/RTCK
3	When 0, pins P1.25:16 are used as GPIO pins. When 1, P1.25:16 are used as a Trace port.	P1.20/ TRACESYNC
5:4	Controls the use of the data bus and strobe pins: Pins P2.7:0 — 11 = P2.7:0 — 0x or 10 = D7:0 Pin P1.0 — 11 = P1.0 — 0x or 10 = CS0 Pin P1.1 — 11 = P1.1 — 0x or 10 = OE Pin P3.31 — 11 = P3.31 — 0x or 10 = BLS0 Pins P2.15:8 — 00 or 11 = P2.15:8 — 01 or 10 = D15:8 Pin P3.30 — 00 or 11 = P3.30 — 01 or 10 = BLS1 Pins P2.27:16 — 0x or 11 = P2.27:16 — 10 = D27:16 Pins P2.29:28 — 0x or 11 = P2.29:28 or reserved — 10 = D29:28 Pins P2.31:30 — 0x or 11 = P2.31:30 or AIN5:4 — 10 = D31:30 Pins P3.29:28 — 0x or 11 = P3.29:28 or AIN6:7 — 10 = BLS2:3	BOOT1:0
6	If bits 5:4 are not 10, controls the use of pin P3.29: 0 enables P3.29, 1 enables AIN6.	1
7	If bits 5:4 are not 10, controls the use of pin P3.28: 0 enables P3.28, 1 enables AIN7.	1
8	Controls the use of pin P3.27: 0 enables P3.27, 1 enables WE.	0
10:9	Reserved.	-
11	Controls the use of pin P3.26: 0 enables P3.26, 1 enables CS1.	0
12	Reserved.	-
13	If bits 25:23 are not 111, controls the use of pin P3.23/A23/XCLK: 0 enables P3.23, 1 enables XCLK.	0
15:14	Controls the use of pin P3.25: 00 enables P3.25, 01 enables CS2, 10 and 11 are reserved values.	00
17:16	Controls the use of pin P3.24: 00 enables P3.24, 01 enables CS3, 10 and 11 are reserved values.	00

Table 8: Pin function select register 2 (PINSEL2 - 0xE002C014) *…continued*

PINSEL2 bits	Description	Reset value
19:18	Reserved.	-
20	If bits 5:4 are not 10, controls the use of pin P2.29:28: 0 enables P2.29:28, 1 is reserved	0
21	If bits 5:4 are not 10, controls the use of pin P2.30: 0 enables P2.30, 1 enables AIN4.	1
22	If bits 5:4 are not 10, controls the use of pin P2.31: 0 enables P2.31, 1 enables AIN5.	1
23	Controls whether P3.0/A0 is a port pin (0) or an address line (1).	1 if BOOT1:0=00 at $\overline{RESET}$=0, 0 otherwise
24	Controls whether P3.1/A1 is a port pin (0) or an address line (1).	$\overline{BOOT1}$ during Reset
27:25	Controls the number of pins among P3.23/A23/XCLK and P3.22:2/A2.22:2 that are address lines: 000 = None; 100 = A11:2 are address lines. 001 = A3:2 are address lines.; 101 = A15:2 are address lines. 010 = A5:2 are address lines.; 110 = A19:2 are address lines. 011 = A7:2 are address lines.; 111 = A23:2 are address lines.	000 if BOOT1:0=11 at Reset, 111 otherwise
31:28	Reserved.	

6.10 External memory controller

The external Static Memory Controller is a module which provides an interface between the system bus and external (off-chip) memory devices. It provides support for up to four independently configurable memory banks (16 MBytes each with byte lane enable control) simultaneously. Each memory banks is capable of supporting SRAM, ROM, Flash EPROM, Burst ROM memory, or some external I/O devices.

Each memory bank may be 8, 16, or 32 bits wide.

6.11 General purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.11.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.12 10-bit A/D converter

The LPC2212/LPC2214 each contain single 10-bit successive approximation analog to digital converter with eight multiplexed channels.

6.12.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400,000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

6.13 UARTs

The LPC2212/LPC2214 each contain two UARTs. One UART provides a full modem control handshake interface, the other provides only transmit and receive data lines.

6.13.1 Features

- 16 byte Receive and Transmit FIFOs.
- Register locations conform to '550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes
- Built-in baud rate generator.
- Standard modem interface signals included on UART1.

6.14 I^2C serial I/O controller

I^2C is a bi-directional bus for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g. an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. I^2C is a multi-master bus, it can be controlled by more than one bus master connected to it.

I^2C implemented in LPC2212/LPC2214 supports bit rate up to 400 kbit/s (Fast I^2C).

6.14.1 Features

- Standard I^2C compliant bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.

- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C bus may be used for test and diagnostic purposes.

6.15 SPI serial I/O controller

The LPC2212/LPC2214 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.15.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex, Communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.16 General purpose timers

The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

6.16.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.17 Watchdog timer

The purpose of the Watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate a system reset if the user program fails to 'feed' (or reload) the Watchdog within a predetermined amount of time.

6.17.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a Watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate Watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($t_{pclk} \times 256 \times 4$) to ($t_{pclk} \times 2^{32} \times 4$) in multiples of $t_{pclk} \times 4$.

6.18 Real time clock

The Real Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.18.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra Low Power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

6.19 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2212/LPC2214. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.19.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.

- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.20 System control

6.20.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 30 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as cclk for purposes of rate equations, etc. f_{osc} and cclk are the same value unless the PLL is running and connected. Refer to Section 6.20.2 “PLL” for additional information.

6.20.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip Reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.20.3 Reset and wake-up timer

Reset has two sources on the LPC2212/LPC2214: the $\overline{\text{RESET}}$ pin and Watchdog Reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip Reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip Flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.20.4 External interrupt inputs

The LPC2212/LPC2214 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

6.20.5 Memory Mapping Control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x00000000. Vectors may be mapped to the bottom of the on-chip Flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.20.6 Power Control

The LPC2212/LPC2214 support two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

6.20.7 VPB bus

The VPB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The VPB divider serves two purposes. The first is to provide peripherals with the desired PCLK via VPB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the VPB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the VPB bus must work properly at power-up (and its timing cannot be altered if it does not work since the VPB divider control registers reside on the VPB bus), the default condition at reset is for the VPB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the VPB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the VPB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.21 Emulation and debugging

The LPC2212/LPC2214 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.21.1 Embedded ICE

Standard ARM EmbeddedICE® logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

6.21.2 Embedded trace

Since the LPC2212/LPC2214 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell™ provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.21.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2212/LPC2214 contain a specific configuration of RealMonitor software programmed into the on-chip Flash memory.

7. Limiting values

Table 9: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{18}	Supply voltage, internal rail		–0.5	+2.5	V
V_3	Supply voltage, external rail		–0.5	+3.6	V
V_{3A}	Analog 3.3 V pad supply voltage		–0.5	4.6	V
AV_{IN}	Analog input voltage on A/D related pins		–0.5	5.1	V
V_i	DC input voltage, 5 V tolerant I/O pins[3][4]		–0.5	6.0	V
V_i	DC input voltage, other I/O pins[2][3]		–0.5	V_3 + 0.5	V
I	DC supply current per supply pin[5]		-	100	mA
I	DC ground current per ground pin[5]		-	100	mA
T_{stg}	Storage temperature[6]		–65	150	°C
P	Power dissipation (based on package heat transfer, not device power consumption)		1.5	-	W

[1] The following applies to the Limiting values:

a) Stresses above those listed under Limiting values may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Section 8 "Static characteristics" and Section 9 "Dynamic characteristics" of this specification is not implied.

b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Not to exceed 4.6 V.

[3] Including voltage on outputs in 3-state mode.

[4] Only valid when the V_3 supply voltage is present.

[5] The peak current is limited to 25 times the corresponding maximum current.

[6] Dependent on package type.

8. Static characteristics

Table 10: Static characteristics

T_{amb} = –40 °C to +85 °C for commercial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{18}	Supply voltage		1.65	1.8	1.95	V
V_3	External rail supply voltage		3.0	3.3	3.6	V
V_{3A}	Analog 3.3 V pad supply voltage		2.5	3.3	3.6	V
Standard Port pins, $\overline{\text{RESET}}$, RTCK						
I_{IL}	Low level input current, no pull-up	V_i = 0	-	-	3	µA
I_{IH}	High level input current, no pull down	$V_i = V_3$	-	-	3	µA
I_{OZ}	3-state output leakage, no pull-up/down	V_o = 0, $V_o = V_3$	-	-	3	µA
$I_{latchup}$	I/O latch-up current	–(0.5 V_3) < V < (1.5 V_3) T_j < 125 °C	100	-	-	mA
V_i	Input voltage[3][4][5]		0	-	5.5	V
V_o	Output voltage, output active		0	-	V_3	V
V_{IH}	High level input voltage		2.0	-	-	V
V_{IL}	Low level input voltage		-	-	0.8	V
V_{hys}	Hysteresis voltage		-	0.4	-	V
V_{OH}	High level output voltage[6]	I_{OH} = –4 mA	V_3 – 0.4	-	-	V
V_{OL}	Low level output voltage[6]	I_{OL} = –4 mA	-	-	0.4	V
I_{OH}	High level output current[6]	$V_{OH} = V_3$ – 0.4 V	–4	-	-	mA
I_{OL}	Low level output current[6]	V_{OL} = 0.4 V	4	-	-	mA
I_{OH}	High level short circuit current[7]	V_{OH} = 0	-	-	–45	mA
I_{OL}	Low level short circuit current[7]	$V_{OL} = V_3$	-	-	50	mA
I_{PD}	Pull-down current	V_i = 5 V[8]	10	50	150	µA
I_{PU}	Pull-up current (applies to P1.16 - P1.25)	V_i = 0	–15	–50	–85	µA
		$V_3 < V_i <$ 5 V[8]	0	0	0	µA
I_{18}	Active Mode	V_{18} = 1.8 V, cclk = 60 MHz, T_{amb} = 25 °C, code while(1){} executed from FLASH, no active peripherals	-	60	-	mA
	Power-down Mode	V_{18} = 1.8 V, T_{amb} = +25 °C,	-	10	-	µA
		V_{18} = 1.8 V, T_{amb} = +85 °C	-	110	500	µA
I^2C pins						
V_{IH}	High level input voltage	V_{TOL} is from 4.5 V to 5.5 V	0.7 V_{TOL}	-	-	V
V_{IL}	Low level input voltage	V_{TOL} is from 4.5 V to 5.5 V	-	-	0.3 V_{TOL}	V
V_{hys}	Hysteresis voltage	V_{TOL} is from 4.5 V to 5.5 V	-	0.5 V_{TOL}	-	V

Table 10: Static characteristics *…continued*

T_{amb} = –40 °C to +85 °C for commercial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{OL}	Low level output voltage[6]	I_{OL} = 3 mA	-	-	0.4	V
I_{lkg}	Input leakage to V_{SS}	$V_i = V_3$	-	2	4	µA
		V_i = 5 V	-	10	22	µA
Oscillator pins						
	X1 input Voltages		0	-	V_{18}	
	X2 output Voltages		0	-	V_{18}	
On-chip Flash program memory						
	endurance (write and erase)		100,000	-	-	cycles
	data retention		20	-	-	years

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Pin capacitance is characterized but not tested.

[3] Including voltage on outputs in 3-state mode.

[4] V_3 supply voltages must be present.

[5] 3-state outputs go into 3-state mode when V_3 is grounded.

[6] Accounts for 100 mV voltage drop in all supply lines.

[7] Only allowed for a short time period.

[8] Minimum condition for V_i = 4.5 V, maximum condition for V_i = 5.5 V.

Table 11: A/D converter DC electrical characteristics

V_{3A} = 2.5 V to 3.6 V unless otherwise specified; T_{amb} = –40 °C to +85 °C unless otherwise specified; A/D converter frequency 4.5 MHz.

Symbol	Parameter	Min	Max	Unit
AV_{IN}	Analog input voltage	0	V_{3A}	V
C_{IN}	Analog input capacitance	-	1	pF
DL_e	Differential non-linearity[1][2][3]	-	±1	LSB
IL_e	Integral non-linearity[1][4]	-	±2	LSB
OS_e	Offset error[1][5]	-	±3	LSB
G_e	Gain error[1][6]	-	±0.5	%
A_e	Absolute error[1][7]	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{3A} = 3.3 V.

[2] The A/D is monotonic, there are no missing codes.

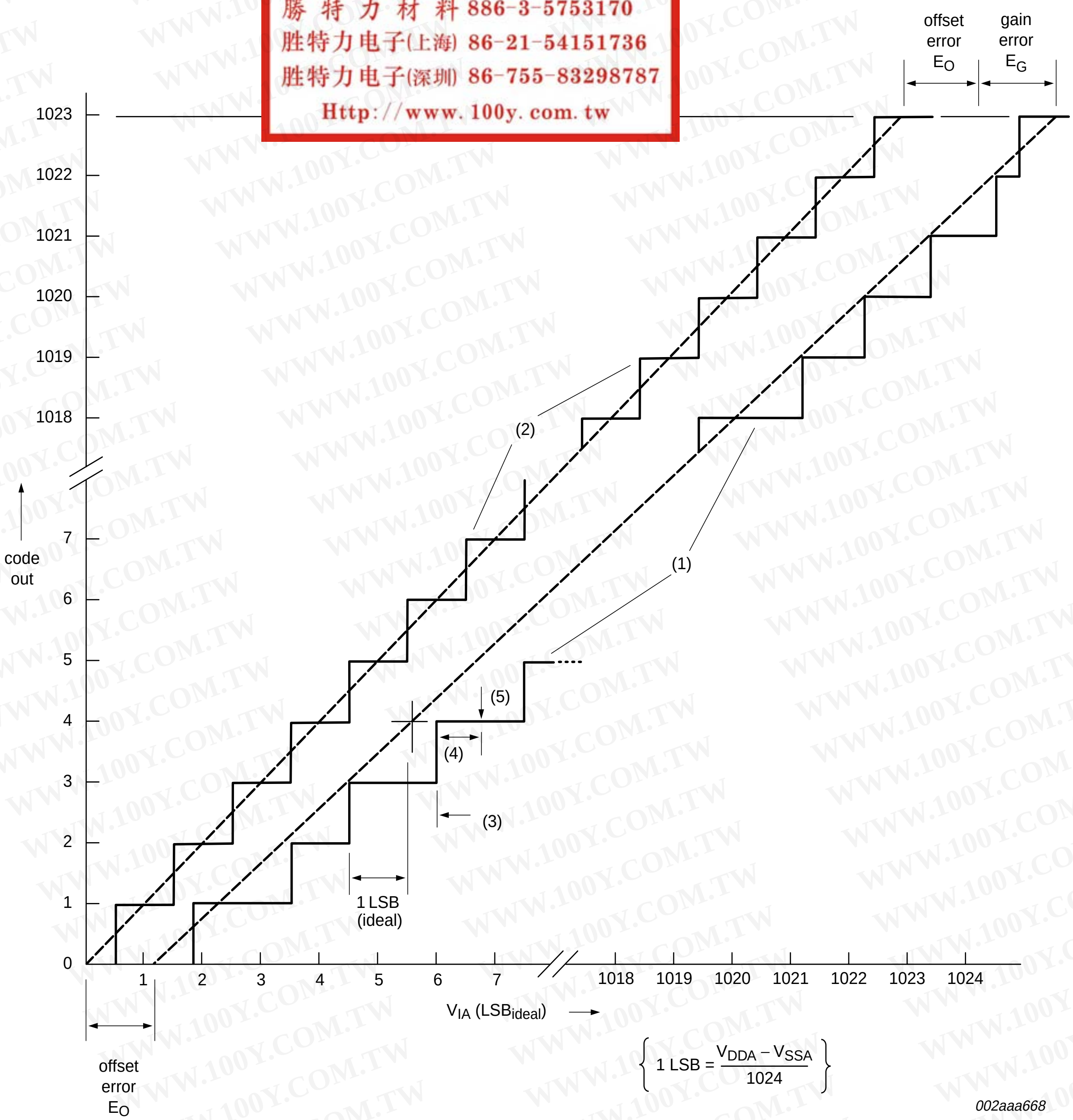
[3] The differential non-linearity (DLe) is the difference between the actual step width and the ideal step width. See Figure 4.

[4] The integral no-linearity (ILe) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 4.

[5] The offset error (OSe) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 4.

[6] The gain error (Ge) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 4.

[7] The absolute voltage error (Ae) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated A/D and the ideal transfer curve. See Figure 4.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential non-linearity (DL_e).

(4) Integral non-linearity (IL_e).

(5) Center of a step of the actual transfer curve.

Fig 4. A/D conversion characteristics.

9. Dynamic characteristics

Table 12: Characteristics

T_{amb} = 0 °C to +70 °C for commercial, –40 °C to +85 °C for industrial, V_{18}, V_3 over specified ranges[1]

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
External Clock						
f_{osc}	Oscillator frequency supplied by an external oscillator (signal generator)		1	-	50	MHz
	External clock frequency supplied by an external crystal oscillator		1	-	30	MHz
	External clock frequency if on-chip PLL is used		10	-	25	MHz
	External clock frequency if ISP is used for initial code download		10	-	25	MHz
t_C	Oscillator clock period		20	-	1000	ns
t_{CHCX}	Clock high time		$t_c \times 0.4$	-	-	ns
t_{CLCX}	Clock low time		$t_c \times 0.4$	-	-	ns
t_{CLCH}	Clock rise time		-	-	5	ns
t_{CHCL}	Clock fall time		-	-	5	ns
Port Pins						
t_{RISE}	Port output rise time (except P0.2, P0.3)		-	10	-	ns
t_{FALL}	Port output fall time (except P0.2, P0.3)		-	10	-	ns
I^2C pins						
t_f	Output fall time from V_{IH} to V_{IL}		20 + $0.1 \times C_b$[2]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

Table 13: External memory interface AC characteristics. C_L = 25 pF. T_{amb} = 40 °C

Symbol	Description	Min	Max	Unit
Common to Read and Write Cycles				
t_{CHAVR}	XCLK HIGH to Address Valid	-	10	ns
t_{CHCSL}	XCLK HIGH to CS LOW	-	10	ns
t_{CHCSH}	XCLK HIGH to CS HIGH	-	10	ns
t_{CHANV}	XCLK HIGH to Address Invalid	-	10	ns
Read Cycle Parameters				
t_{CSLAV}	CS LOW to Address Valid	–5[1]	10	ns
t_{OELAVR}	OE LOW to Address Valid	–5[1]	10	ns
t_{CSLOEL}	CS LOW to OE LOW	–5	5	ns
t_{AVDV}	Memory Access Time (latest of Address Valid, CS LOW, OE LOW to Data Valid)	(t_{CYC}*(2 + WST1)) + (–20)	-	ns

Table 13: External memory interface AC characteristics. C_L = 25 pF. T_{amb} = 40 °C...*continued*

Symbol	Description	Min	Max	Unit
t_{AVDV}	Burst-ROM Initial Memory Access Time (latest of Address Valid, CS LOW, OE LOW to Data Valid)	$(t_{CYC}*(2 + WST1)) + (-20)$	-	ns
t_{AVDV}	Burst-ROM Subsequent Memory Access Time (Address Valid to Data Valid)	$t_{CYC} + (-20)$	-	ns
t_{STHDNV}	Data Hold Time (earliest of CS HIGH, OE HIGH, Address Change to Data Invalid)	0	-	ns
t_{CSHOEH}	CS HIGH to OE HIGH	–5	5	ns
t_{OEHANV}	OE HIGH to Address Invalid	–5	5	ns
t_{CHOEL}	XCLK HIGH to OE LOW	–5	5	ns
t_{CHOEH}	XCLK HIGH to OE HIGH	–5	5	ns
Write Cycle Parameters				
t_{AVCSLW}	Address Valid to CS LOW	$t_{CYC} - 10$ [1]	-	ns
t_{CSLDVW}	CS LOW to Data Valid	–5	5	ns
t_{CSLWEL}	CS LOW to WE LOW	–5	5	ns
$t_{CSLBLSL}$	CS LOW to BLS LOW	–5	5	ns
t_{WELDV}	WE LOW to Data Valid	–5	5	ns
t_{CSLDV}	CS LOW to Data Valid	–5	5	ns
t_{WELWEH}	WE LOW to WE HIGH	$t_{CYC} \times (1 + WST2) - 5$	$t_{CYC}*(1 + WST2) + 5$	ns
t_{WELWEH}	BLS LOW to BLS HIGH	$t_{CYC} \times (1 + WST2) - 5$	$t_{CYC}*(1 + WST2) + 5$	ns
t_{WEHANV}	WE HIGH to Address Invalid	$t_{CYC}-5$	$t_{CYC} + 5$	ns
t_{WEHDNV}	WE HIGH to Data Invalid	$(2 \times t_{CYC})-5$	$(2 \times t_{CYC}) + 5$	ns
$t_{BLSHANV}$	BLS HIGH to Address Invalid	$t_{CYC}-5$	$t_{CYC} + 5$	ns
$t_{BLSHDNV}$	BLS HIGH to Data Invalid	$(2 \times t_{CYC})-5$	$(2 \times t_{CYC}) + 5$	ns
t_{CHDV}	XCLK HIGH to Data Valid	-	10	ns
t_{CHWEL}	XCLK HIGH to WE LOW	-	10	ns
$t_{CHHBLSL}$	XCLK HIGH to BLS LOW	-	10	ns
t_{AVCSL}	XCLK HIGH to WE HIGH	-	10	ns
t_{AVCSL}	XCLK HIGH to BLS HIGH	-	10	ns
t_{AVCSL}	XCLK HIGH to Data Invalid	-	10	ns

[1] Except on initial access, in which case the address is set up t_{CYC} earlier.

Table 14: Standard read access specifications

Access cycle	Max frequency	WST setting WST ≥ 0; round up to integer	Memory access time requirement
Standard read	$f_{MAX} \le \frac{2 + WST1}{t_{RAM} + 20ns}$	$WST1 \ge \frac{t_{RAM} + 20ns}{t_{CYC}} - 2$	$t_{RAM} \le t_{CYC} \times (2 + WST1) - 20ns$
Standard write	$f_{MAX} \le \frac{1 + WST2}{t_{WRITE} + 5ns}$	$WST2 \ge \frac{t_{WRITE} - t_{CYC} + 5}{t_{CYC}}$	$t_{WRITE} \le t_{CYC} \times (1 + WST2) - 5ns$
Burst read - initial	$f_{MAX} \le \frac{2 + WST1}{t_{INIT} + 20ns}$	$WST1 \ge \frac{t_{INIT} + 20ns}{t_{CYC}} - 2$	$t_{INIT} \le t_{CYC} \times (2 + WST1) - 20ns$
Burst read - subsequent 3×	$f_{MAX} \le \frac{1}{t_{ROM} + 20ns}$	N/A	$t_{ROM} \le t_{CYC} - 20ns$

9.1 Timing

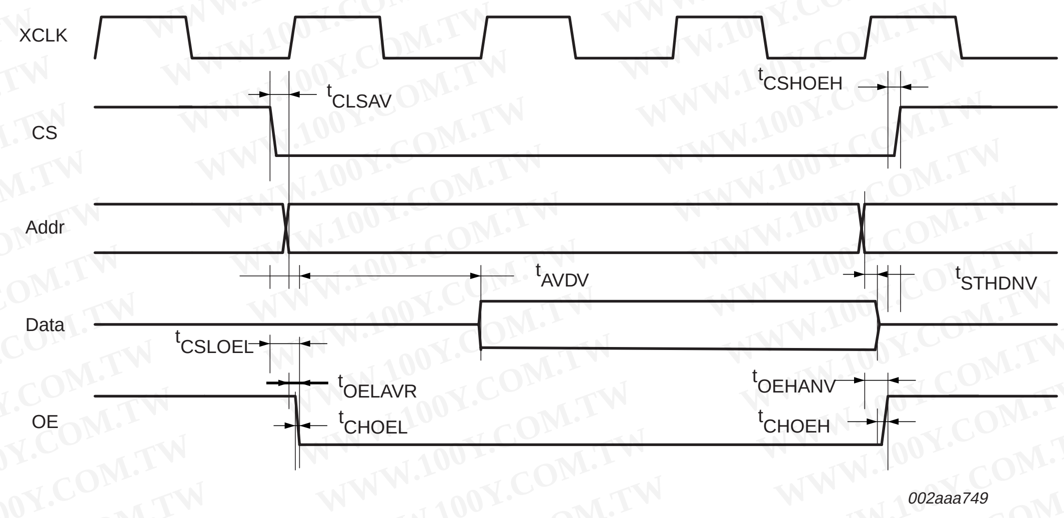


Fig 5. External memory read access.

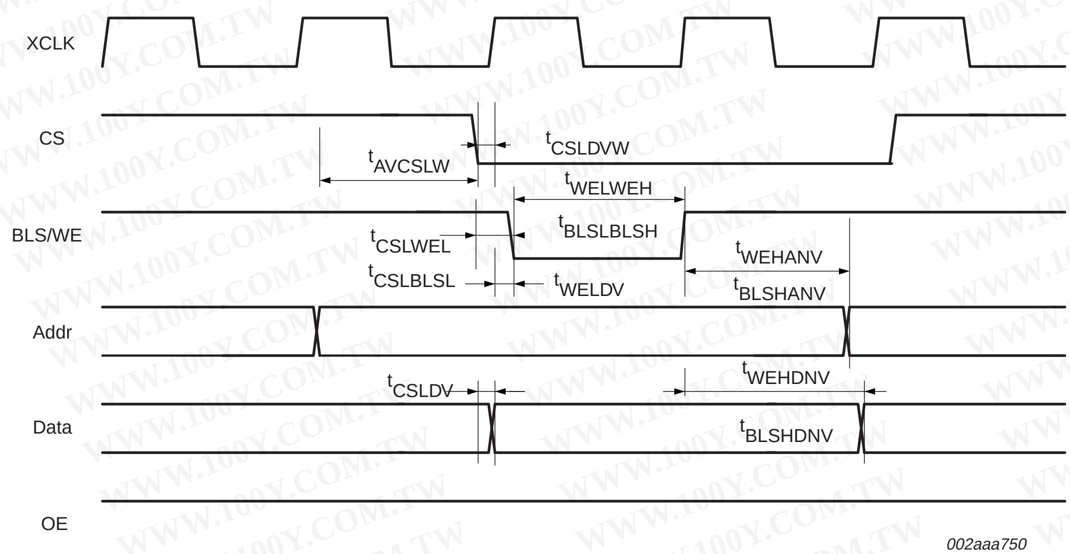


Fig 6. External memory write access.

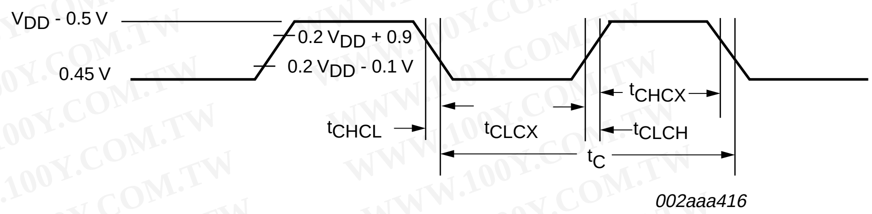
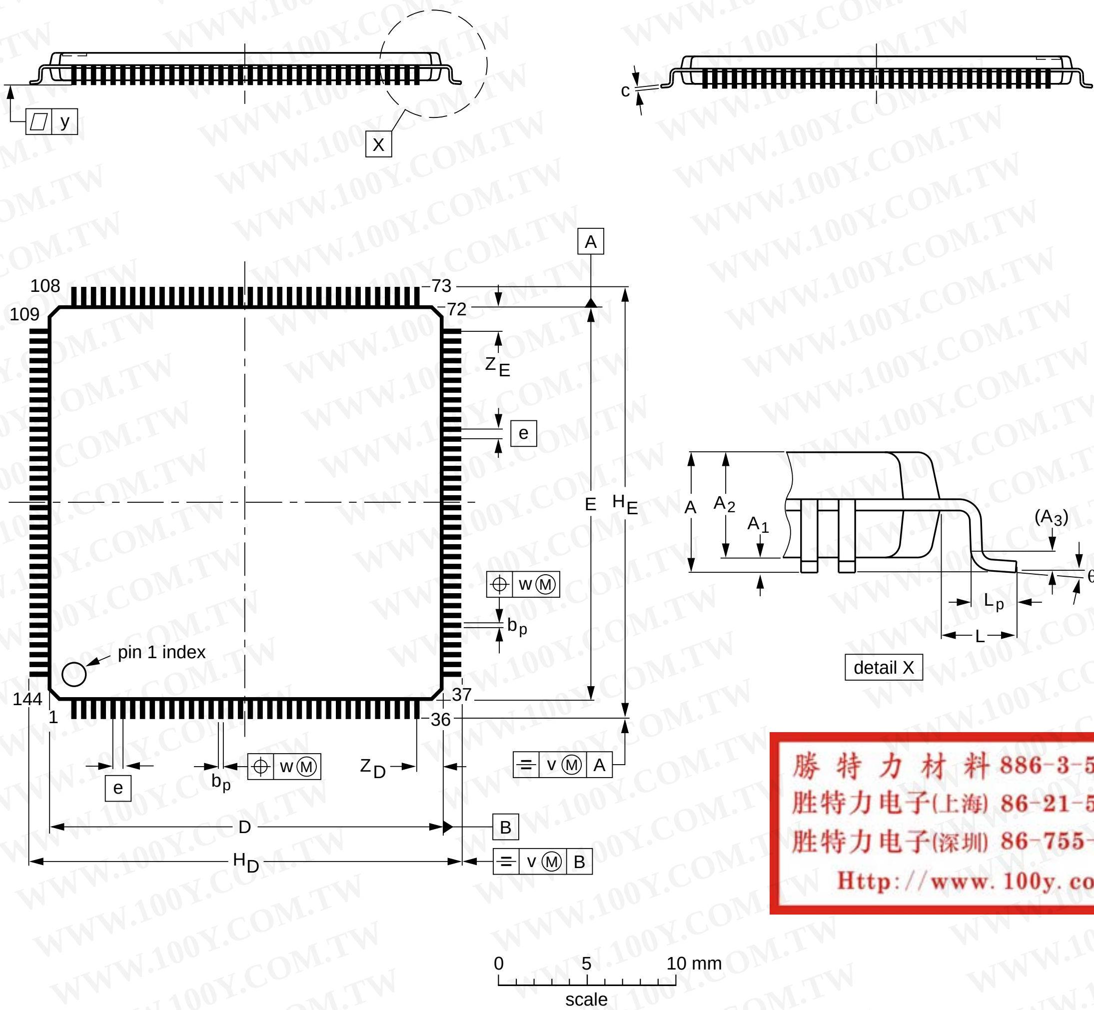


Fig 7. External clock timing.

9397 750 13149

10. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D[(1)]	E[(1)]	e	H_D	H_E	L	L_p	v	w	y	Z_D[(1)]	Z_E[(1)]	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^{o} 0^{o}

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 8. SOT486-1 (LQFP144).

11. Revision history

Table 15: Revision history

Rev	Date	CPCN	Description
02	20041223	-	**Product data (9397 750 13149)** Modifications: • Section 6.2 “On-Chip Flash program memory” on page 11; updated text. • Section 6.20.2 “PLL” on page 25; updated text. • Section 6.20.7 “VPB bus” on page 26; updated text. • Table 9 “Limiting values” on page 28; updated storage temperature specs. • Table 10 “Static characteristics” on page 29; adjusted I_{18} typical value; added On-chip Flash program memory specs.
01	20040202	-	**Preliminary data (9397 750 12747)**

12. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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