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Intel® Embedded Flash Memory (J3 v. D)

32, 64, 128, and 256 Mbit

Datasheet

Product Features

- Architecture
  - High-density symmetrical 128-Kbyte blocks
  - 256 Mbit (256 blocks)
  - 128 Mbit (128 blocks)
  - 64 Mbit (64 blocks)
  - 32 Mbit (32 blocks)
- Performance
  - 75 ns Initial Access Speed (128/64/32 -Mbit densities)
  - 95 ns Initial Access Speed (256 Mbit only)
  - 25 ns 8-word and 4-word Asynchronous page-mode reads
  - 32-Byte Write buffer
  - 4 µs per Byte Effective programming time
- System Voltage and Power
  - V_{CC} = 2.7 V to 3.6 V
  - V_{CCQ} = 2.7 V to 3.6 V
- Packaging
  - 56-Lead TSOP package (32, 64, 128 Mbit only)
  - 64-Ball Intel® Easy BGA package (32, 42, 128 and 256 Mbit)
- Security
  - Enhanced security options for code protection
  - 128-bit Protection Register
  - 64-bit Unique device identifier
  - 64-bit User-programmable OTP cells
  - Absolute protection with V_{PEN} = GND
  - Individual block locking
  - Block erase/program lockout during power transitions
- Software
  - Program and erase suspend support
  - Flash Data Integrator (FDI), Common Flash Interface (CFI) Compatible
- Quality and Reliability
  - Operating temperature: -40 °C to +85 °C
  - 100K Minimum erase cycles per block
  - 0.13 µm ETOX™ VIII Process

Document Number: 308551-004US
February 2007

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Contents

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Revision History

Date	Revision	Description
July 2005	001	Initial release
September 2005	002	Changed Marketing name from 28FxxxJ3 to J3 v. D. Updated the following: • Table 18, "Command Bus Operations" on page 36 • Section 9.2.2, "Read Status Register" on page 39 • Section 9.3.2, "Buffered Programming" on page 41 • Table 26, "Valid Commands During Suspend" on page 43 Added Table 27, "STS Configuration Register" on page 44.
February 2006	003	Section 5.3.1, "Power-Up/Down Characteristics" on page 20 was modified. Notes on Table 8, "DC Voltage Characteristics" on page 22 were updated Table 10, "Read Operations" on page 25 was updated with R16 value Table 12, "Configuration Performance" on page 30 was updated Note 1 of Table 28, "STS Configuration Coding Definitions" on page 45 was updated.
February 2007	004	Added 256-Mbit Updated format.

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1.0 Introduction

This document contains information pertaining to the Intel® Embedded Flash Memory (J3 v. D) device features, operation, and specifications.

The Intel® Embedded Flash Memory J3 Version D (J3 v. D) provides improved mainstream performance with enhanced security features, taking advantage of the high quality and reliability of the NOR-based Intel 0.13 µm ETOX™ VIII process technology. Offered in 128-Mbit (16-Mbyte), 64-Mbit, and 32-Mbit densities, the Intel® Embedded Flash Memory (J3 v. D) device brings reliable, low-voltage capability (3 V read, program, and erase) with high speed, low-power operation. The Intel® Embedded Flash Memory (J3 v. D) device takes advantage of the proven manufacturing experience and is ideal for code and data applications where high density and low cost are required, such as in networking, telecommunications, digital set top boxes, audio recording, and digital imaging. Intel Flash Memory components also deliver a new generation of forward-compatible software support. By using the Common Flash Interface (CFI) and Scalable Command Set (SCS), customers can take advantage of density upgrades and optimized write capabilities of future Intel® Flash Memory devices.

1.1 Nomenclature

AMIN:	All Densities	AMIN = A0 for x8
	All Densities	AMIN = A1 for x16
AMAX:	32 Mbit	AMAX = A21
	64 Mbit	AMAX = A22
	128 Mbit	AMAX = A23
Block:	A group of flash cells that share common erase circuitry and erase simultaneously	
Clear:	Indicates a logic zero (0)	
Program:	To write data to the flash array	
Set:	Indicates a logic one (1)	
VPEN:	Refers to a signal or package connection name	
V_{PEN}:	Refers to timing or voltage levels	

1.2 Acronyms

CUI:	Command User Interface
OTP:	One Time Programmable
PLR:	Protection Lock Register
PR:	Protection Register
PRD:	Protection Register Data
RFU:	Reserved for Future Use

SR:	Status Register
SRD:	Status Register Data
WSM:	Write State Machine
ECR:	Enhanced Configuration Register

1.3 Conventions

h:	Hexadecimal Affix
k (noun):	1,000
M (noun):	1,000,000
Nibble	4 bits
Byte:	8 bits
Word:	16 bits
Kword:	1,024 words
Kb:	1,024 bits
KB:	1,024 bytes
Mb:	1,048,576 bits
MB:	1,048,576 bytes
Brackets:	Square brackets ([]) will be used to designate group membership or to define a group of signals with similar function (i.e. A[21:1], SR[4,1] and D[15:0]).
00FFh:	Denotes 16-bit hexadecimal numbers
00FF 00FFh:	Denotes 32-bit hexadecimal numbers
DQ[15:0]:	Data I/O signals

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2.0 Functional Overview

The Intel® Embedded Flash Memory (J3 v. D) family contains high-density memory organized in any of the following configurations:

- 32 Mbytes or 16 Mword (256-Mbit), organized as two-hundred-fifty-six 128-Kbyte (131,072 bytes) erase blocks- Users should be aware that this density is not offered in a monolithic part and the device is made up of 2x128-Mb devices.
- 16 Mbytes or 8 Mword (128-Mbit), organized as one-hundred-twenty-eight 128-Kbyte erase blocks
- 8 Mbytes or 4 Mword (64-Mbit), organized as sixty-four 128-Kbyte erase blocks
- 4 Mbytes or 2 Mword (32-Mbit), organized as thirty-two 128-Kbyte erase blocks

These devices can be accessed as 8- or 16-bit words. See Figure 1, “Intel® Embedded Flash Memory (J3 v. D) Memory Block Diagram (32, 64 and 128 Mbit)” on page 10 for further details.

A 128-bit Protection Register has multiple uses, including unique flash device identification.

The Intel® Embedded Flash Memory (J3 v. D) device includes new security features that were not available on the (previous) 0.25µm and 0.18µm versions of the J3 family. These new security features prevent altering of code through different protection schemes that can be implemented, based on user requirements.

The Intel® Embedded Flash Memory (J3 v. D) device optimized architecture and interface dramatically increases read performance by supporting page-mode reads. This read mode is ideal for non-clock memory systems.

A Common Flash Interface (CFI) permits software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

Scalable Command Set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant flash memory devices, independent of system-level packaging (e.g., memory card, SIMM, or direct-to-board placement). Additionally, SCS provides the highest system/device data transfer rates and minimizes device and system-level implementation costs.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device’s 128-Kbyte blocks typically within one second, independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or program data from any other block. Similarly, program suspend allows system software to suspend programming (byte/word program and write-to-buffer operations) to read data or execute code from any other block that is not being suspended.

Each device incorporates a Write Buffer of 32 bytes (16 words) to allow optimum programming performance. By using the Write Buffer, data is programmed in buffer increments.

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Blocks are selectively and individually lockable in-system. Individual block locking uses block lock-bits to lock and unlock blocks. Block lock-bits gate block erase and program operations. Lock-bit configuration operations set and clear lock-bits (using the Set Block Lock-Bit and Clear Block Lock-Bits commands).

The Status Register indicates when the WSM's block erase, program, or lock-bit configuration operation is finished.

The STS (STATUS) output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status indication using STS minimizes both CPU overhead and system power consumption. When configured in level mode (default mode), it acts as a RY/BY# signal. When low, STS indicates that the WSM is performing a block erase, program, or lock-bit configuration. STS-high indicates that the WSM is ready for a new command, block erase is suspended (and programming is inactive), program is suspended, or the device is in reset/power-down mode. Additionally, the configuration command allows the STS signal to be configured to pulse on completion of programming and/or block erases.

Three CE signals are used to enable and disable the device. A unique CE logic design (see Table 15, "Chip Enable Truth Table" on page 32) reduces decoder logic typically required for multi-chip designs. External logic is not required when designing a single chip, a dual chip, or a 4-chip miniature card or SIMM module.

The BYTE# signal allows either x8 or x16 read/writes to the device:

- BYTE#-low enables 8-bit mode; address A0 selects between the low byte and high byte.
- BYTE#-high enables16-bit operation; address A1 becomes the lowest order address and address A0 is not used (don't care).

Figure 1, "Intel® Embedded Flash Memory (J3 v. D) Memory Block Diagram (32, 64 and 128 Mbit)" on page 10 shows a device block diagram.

When the device is disabled (see Table 15, "Chip Enable Truth Table" on page 32), with CEx at VIH and RP# at VIH, the standby mode is enabled. When RP# is at VIL, a further power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (tPHQV) is required from RP# going high until data outputs are valid. Likewise, the device has a wake time (tPHWL) from RP#-high until writes to the CUI are recognized. With RP# at VIL, the WSM is reset and the Status Register is cleared.

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2.1 Block Diagram

Figure 1. Intel® Embedded Flash Memory (J3 v. D) Memory Block Diagram (32, 64 and 128 Mbit)

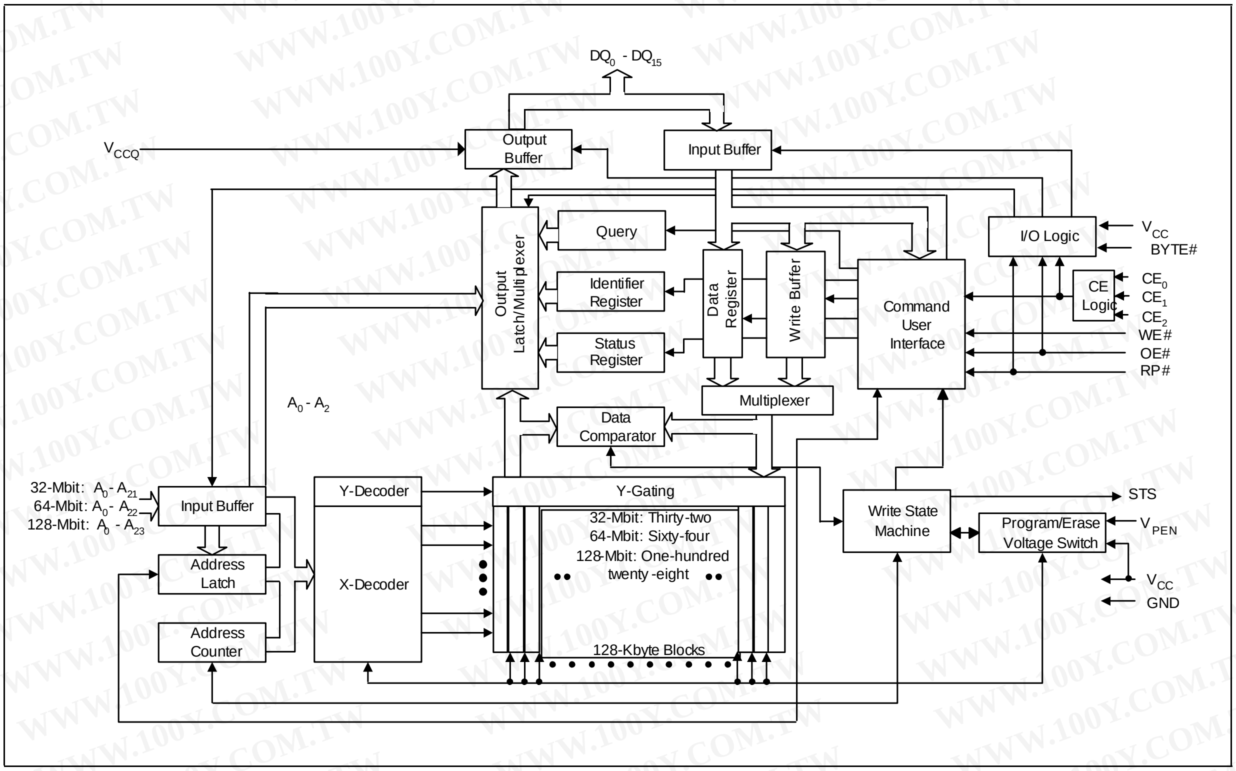
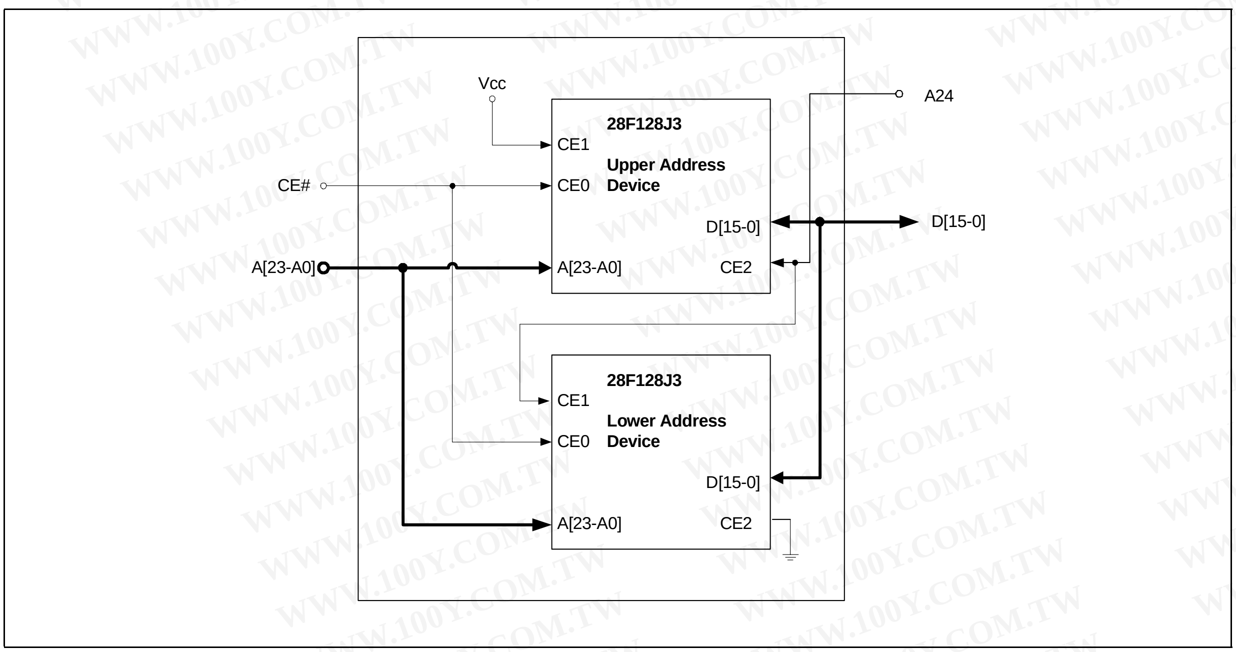


Figure 2. Intel® Embedded Flash Memory (J3 v. D) Memory Block Diagram (256 Mbit)



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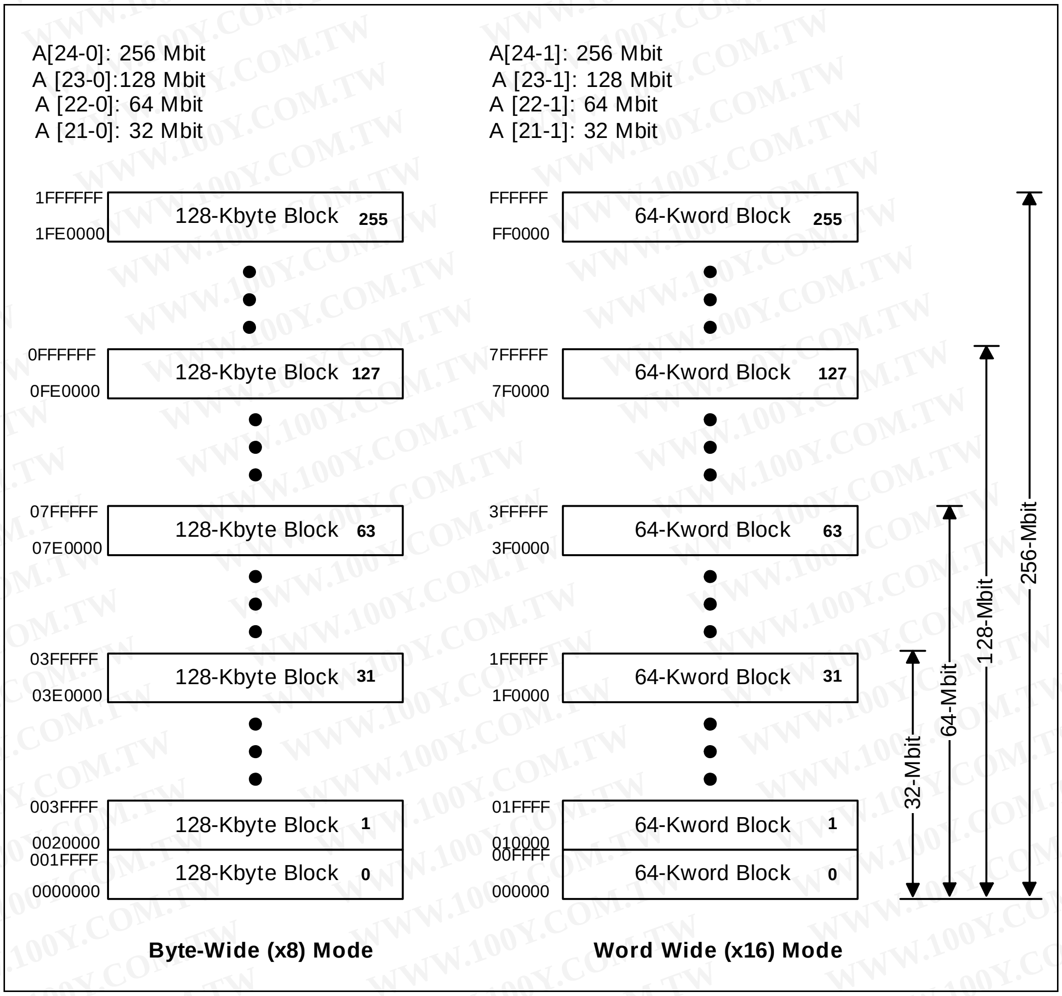
2.2 Memory Map

Figure 3. Intel® Embedded Flash Memory (J3 v. D) Memory Map



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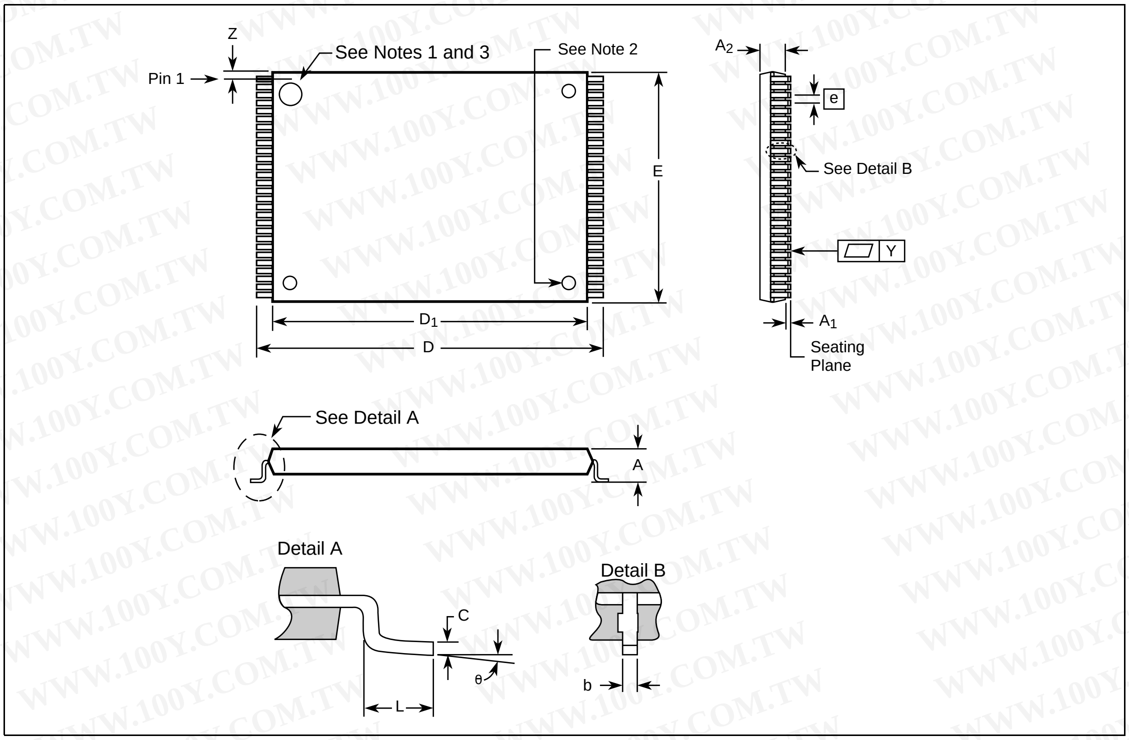
3.0 Package Information

3.1 56-Lead TSOP Package (32, 64, 128 Mbit)

Figure 4. 56-Lead TSOP Package Mechanical



Notes:

1. One dimple on package denotes Pin 1.
2. If two dimples, then the larger dimple denotes Pin 1.
3. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.

Table 1. 56-Lead TSOP Dimension Table

Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A			1.200			0.047
Standoff	A_1	0.050			0.002		
Package Body Thickness	A_2	0.965	0.995	1.025	0.038	0.039	0.040
Lead Width	b	0.100	0.150	0.200	0.004	0.006	0.008
Lead Thickness	c	0.100	0.150	0.200	0.004	0.006	0.008
Package Body Length	D_1	18.200	18.400	18.600	0.717	0.724	0.732
Package Body Width	E	13.800	14.000	14.200	0.543	0.551	0.559
Lead Pitch	e		0.500			0.0197	
Terminal Dimension	D	19.800	20.00	20.200	0.780	0.787	0.795
Lead Tip Length	L	0.500	0.600	0.700	0.020	0.024	0.028

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Table 1. 56-Lead TSOP Dimension Table

Parameter	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Lead Count	N		56			56	
Lead Tip Angle	q	0°	3°	5°	0°	3°	5°
Seating Plane Coplanarity	Y			0.100			0.004
Lead to Package Offset	Z	0.150	0.250	0.350	0.006	0.010	0.014

3.2 Easy BGA Package (32, 64, 128 and 256 Mbit)

Figure 5. Easy BGA Mechanical Specifications

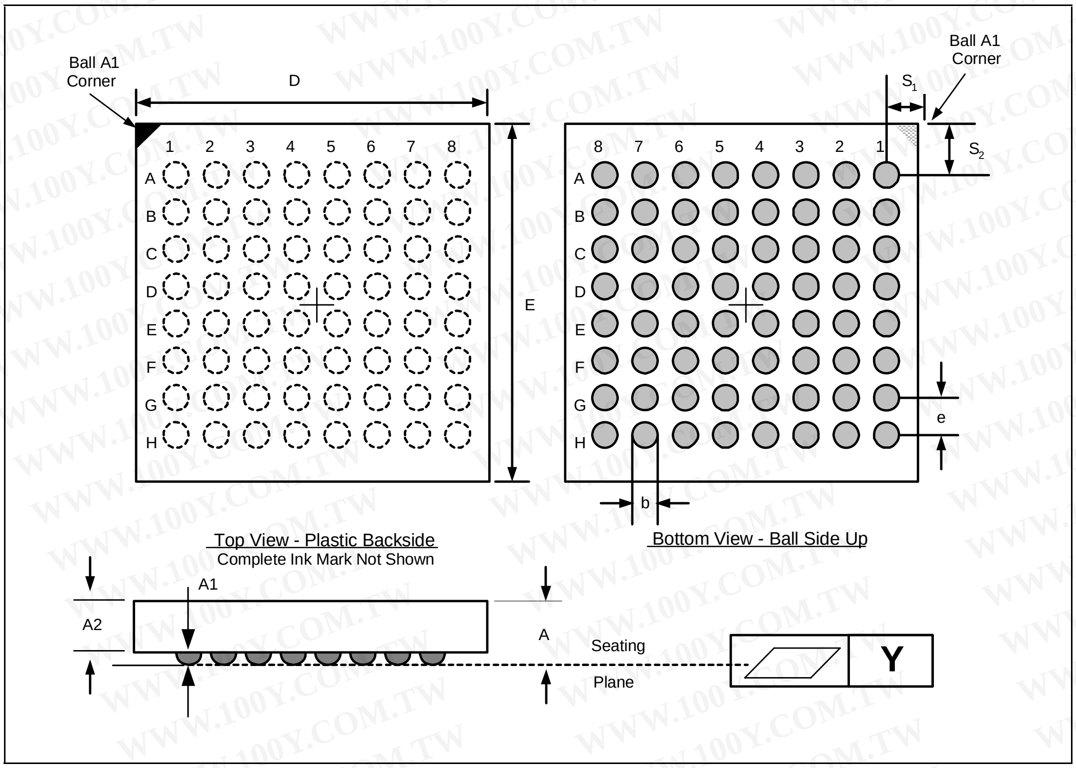

Table 2. Easy BGA Package Dimensions Table (Sheet 1 of 2)

Parameter	Symbol	Millimeters				Inches		
		Min	Nom	Max	Notes	Min	Nom	Max
Package Height (32, 64, 128- Mbit)	A			1.200				0.0472
Package Height (256- Mbit)	A			1.300				0.0512
Ball Height	A1	0.250				0.0098		
Package Body Thickness (32, 64, 128- Mbit)	A2		0.780				0.0307	

Table 2. Easy BGA Package Dimensions Table (Sheet 2 of 2)

Parameter	Symbol	Millimeters Min	Millimeters Nom	Millimeters Max	Notes	Inches Min	Inches Nom	Inches Max
Package Body Thickness (256- Mbit)	A2		0.910				0.0358	
Ball (Lead) Width	b	0.330	0.430	0.530		0.0130	0.0169	0.0209
Package Body Width	D	9.900	10.000	10.100	1	0.3898	0.3937	0.3976
Package Body Length	E	12.900	13.000	13.100	1	0.5079	0.5118	0.5157
Pitch	[e]		1.000				0.0394	
Ball (Lead) Count	N		64				64	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along D (32/64/128 Mb)	S1	1.400	1.500	1.600	1	0.0551	0.0591	0.0630
Corner to Ball A1 Distance Along E (32/64/128 Mb)	S2	2.900	3.000	3.100	1	0.1142	0.1181	0.1220

Notes:
1. For Daisy Chain Evaluation Unit information refer to the Intel Flash Memory Packaging Technology Web page at: www.intel.com/design/packtech/index.htm
2. For Packaging Shipping Media information refer to the Intel Flash Memory Packaging Technology Web page at: www.intel.com/design/packtech/index.htm

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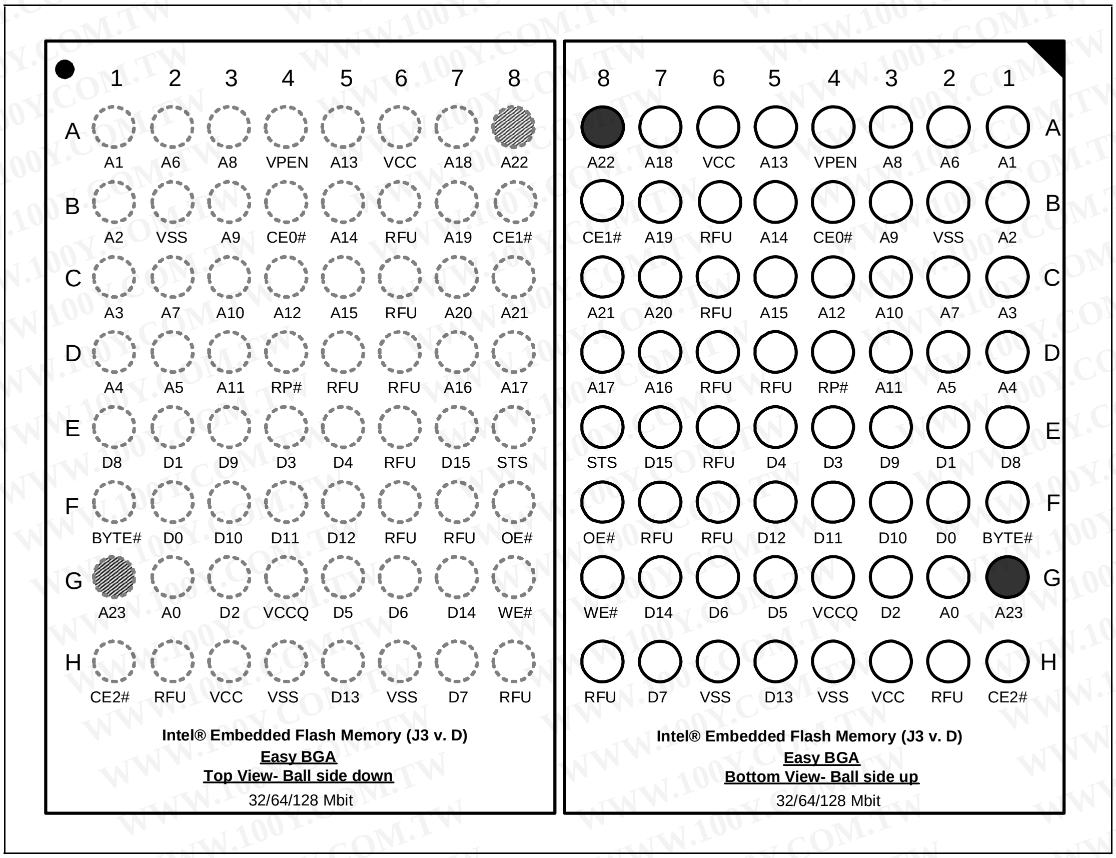
4.0 Ballouts and Signal Descriptions

Intel® Embedded Flash Memory (J3 v. D) is available in two package types. All densities of the Intel® Embedded Flash Memory (J3 v. D) are supported on both 64-ball Easy BGA and 56-lead Thin Small Outline Package (TSOP) packages, except the 256 Mbit density that is available only in Easy BGA. Figure 6, Figure 7 and Figure 8 show the ballouts.

4.1 Easy BGA Ballout (32/64/128 Mbit)

Figure 6. Easy BGA Ballout (32/64/128 Mbit)



Notes:
1. Address A22 is only valid on 64-Mbit densities and above, otherwise, it is a no connect (NC).
2. Address A23 is only valid on 128-Mbit densities and above, otherwise, it is a no connect (NC).

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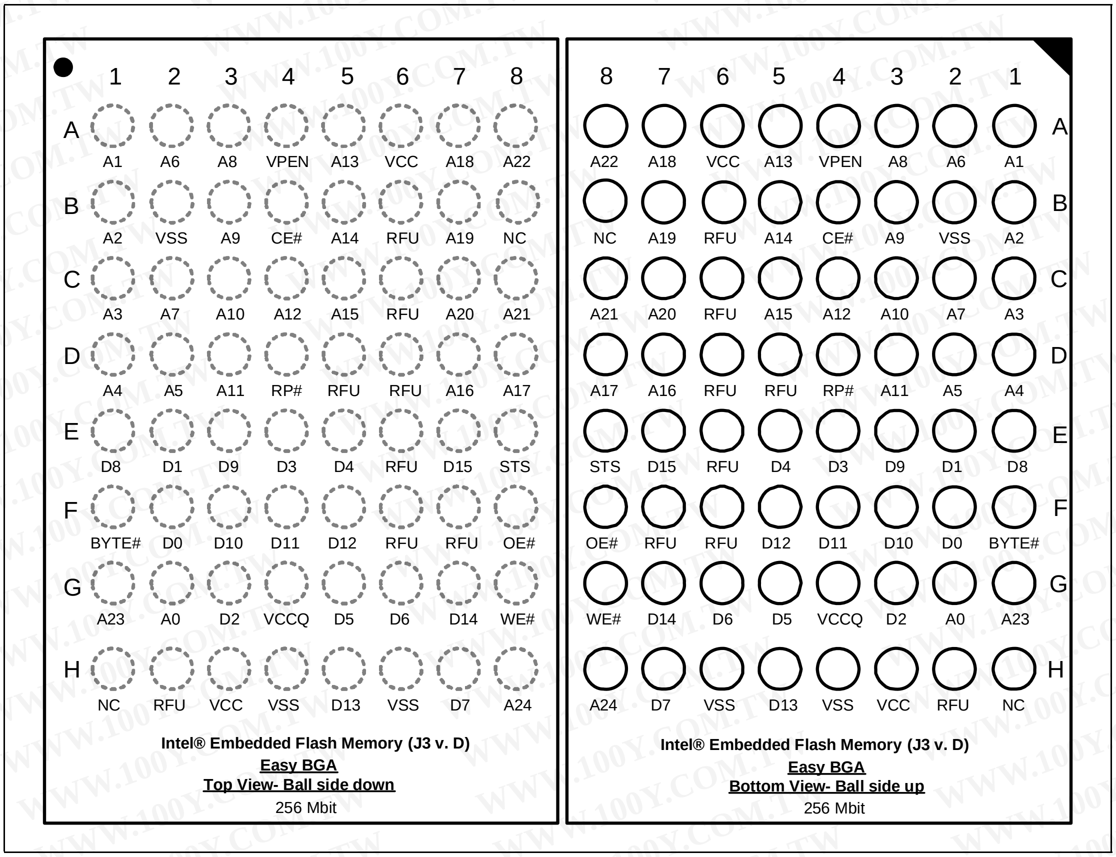
Figure 7. Easy BGA Ballout (256 Mbit)



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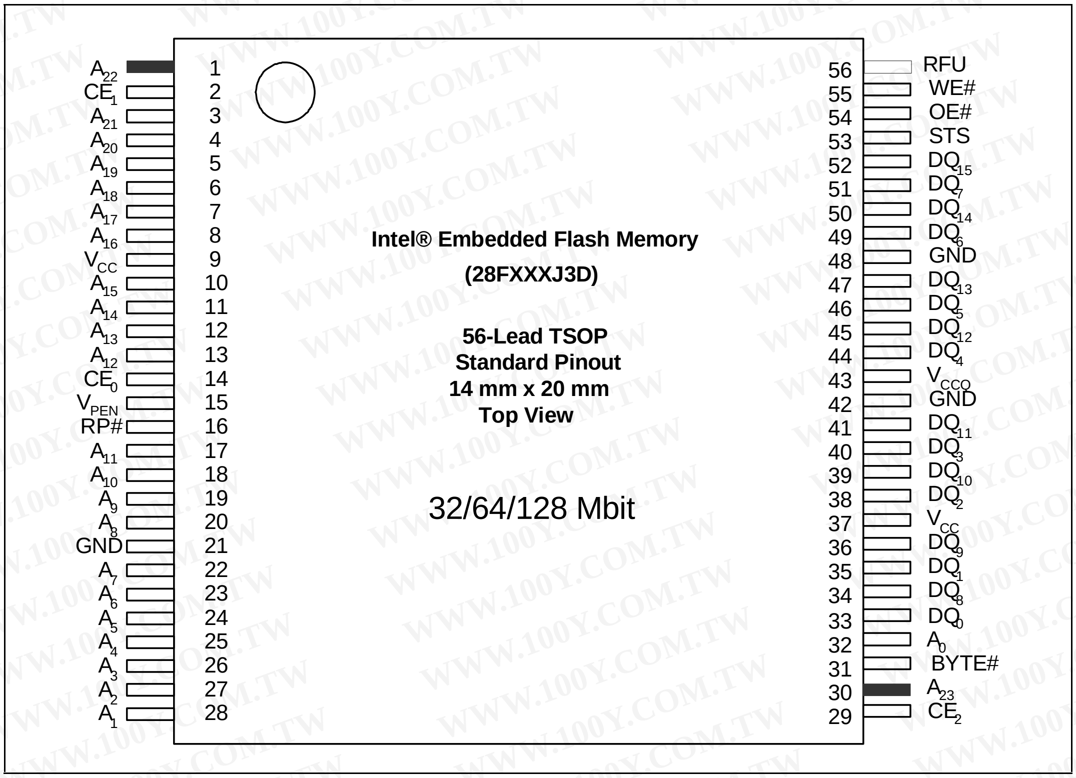
4.2 56-Lead TSOP Package Pinout (32/64/128 Mbit)

Figure 8. 56-Lead TSOP Package Pinout (32/64/128 Mbit)



Notes:
1. A22 exists on 64- and 128- densities. On 32-Mbit density this signal is a no-connect (NC).
2. A23 exists on 128-Mbit densities. On 32- and 64-Mbit densities this signal is a no-connect (NC)

4.3 Signal Descriptions

Table 3 lists the active signals used on Intel® Embedded Flash Memory (J3 v. D) and provides a description of each.

Table 3. Signal Descriptions for Intel® Embedded Flash Memory (J3 v. D) (Sheet 1 of 2)

Symbol	Type	Name and Function
A0	Input	**BYTE-SELECT ADDRESS:** Selects between high and low byte when the device is in x8 mode. This address is latched during a x8 program cycle. Not used in x16 mode (i.e., the A0 input buffer is turned off when BYTE# is high).
A[MAX:1]	Input	**ADDRESS INPUTS:** Inputs for addresses during read and program operations. Addresses are internally latched during a program cycle: 32-Mbit — A[21:1] 64-Mbit— A[22:1] 128-Mbit — A[23:1] 256-Mbit — A[24:1] A24 acts as a virtual CE for the two devices. A24 at V_{IL} selects the lower die and A24 at V_{IH} selects the upper die. See Figure 2 on page 10
D[7:0]	Input/ Output	**LOW-BYTE DATA BUS:** Inputs data during buffer writes and programming, and inputs commands during CUI writes. Outputs array, CFI, identifier, or status data in the appropriate read mode. Data is internally latched during write operations.

Table 3. Signal Descriptions for Intel® Embedded Flash Memory (J3 v. D) (Sheet 2 of 2)

Symbol	Type	Name and Function
D[15:8]	Input/ Output	**HIGH-BYTE DATA BUS:** Inputs data during x16 buffer writes and programming operations. Outputs array, CFI, or identifier data in the appropriate read mode; not used for Status Register reads. Data is internally latched during write operations in x16 mode. D[15-8] float in x8 mode
CE[2:0]	Input	**CHIP ENABLE:** Activate the 32-, 64- and 128 Mbit devices' control logic, input buffers, decoders, and sense amplifiers. When the device is de-selected (see Table 15, "Chip Enable Truth Table" on page 32), power reduces to standby levels. All timing specifications are the same for these three signals. Device selection occurs with the first edge of CE0, CE1, or CE2 that enables the device. Device deselection occurs with the first edge of CE0, CE1, or CE2 that disables the device (see Table 15, "Chip Enable Truth Table" on page 32).
CE#	Input	**CHIP ENABLE:** Activates the 256Mbit devices' control logic, input buffers, decoders, and sense amplifiers. Device selection occurs with the first edge of CE# that enables the device. Device deselection occurs with the first edge of CE# that disables the device.s
RP#	Input	**RESET:** RP#-low resets internal automation and puts the device in power-down mode. RP#-high enables normal operation. Exit from reset sets the device to read array mode. When driven low, RP# inhibits write operations which provides data protection during power transitions.
OE#	Input	**OUTPUT ENABLE:** Activates the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	Input	**WRITE ENABLE:** Controls writes to the CUI, the Write Buffer, and array blocks. WE# is active low. Addresses and data are latched on the rising edge of WE#.
STS	Open Drain Output	**STATUS:** Indicates the status of the internal state machine. When configured in level mode (default), it acts as a RY/BY# signal. When configured in one of its pulse modes, it can pulse to indicate program and/or erase completion. For alternate configurations of the STATUS signal, see the Configurations command and Section 9.6, "Status Signal (STS)" on page 44. STS is to be tied to VCCQ with a pull-up resistor.
BYTE#	Input	**BYTE ENABLE:** BYTE#-low places the device in x8 mode; data is input or output on D[7:0], while D[15:8] is placed in High-Z. Address A0 selects between the high and low byte. BYTE#-high places the device in x16 mode, and turns off the A0 input buffer. Address A1 becomes the lowest-order address bit.
VPEN	Input	**ERASE / PROGRAM / BLOCK LOCK ENABLE:** For erasing array blocks, programming data, or configuring lock-bits. With $V_{PEN} \le V_{PENLK}$, memory contents cannot be altered.
VCC	Power	**CORE Power Supply:** Core (logic) source voltage. Writes to the flash array are inhibited when $V_{CC} \le V_{LKO}$. Caution: Device operation at invalid Vcc voltages should not be attempted.
VCCQ	Power	**I/O Power Supply:** Power supply for Input/Output buffers.This ball can be tied directly to V_{CC}.
GND	Supply	**Ground:** Ground reference for device logic voltages. Connect to system ground.
NC	—	**No Connect:** Lead is not internally connected; it may be driven or floated.
RFU	—	**Reserved for Future Use:** Balls designated as RFU are reserved by Intel for future device functionality and enhancement.

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5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Temperature under Bias Expanded (T_A, Ambient)	–40	+85	°C	—
Storage Temperature	–65	+125	°C	—
VCC Voltage	–2.0	+5.6	V	2
VCCQ	–2.0	+5.6	V	2
Voltage on any input/output signal (except VCC, VCCQ)	–2.0	V_{CCQ} (max) + 2.0	V	1
I_{SH} Output Short Circuit Current	—	100	mA	3

Notes:

1. Voltage is referenced to V_{SS}. During infrequent non-periodic transitions, the voltage potential between V_{SS} and input/output pins may undershoot to –2.0 V for periods < 20 ns or overshoot to V_{CCQ} (max) + 2.0 V for periods < 20 ns.
2. During infrequent non-periodic transitions, the voltage potential between V_{CC} and the supplies may undershoot to –2.0 V for periods < 20 ns or V_{SUPPLY} (max) + 2.0 V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time

5.2 Operating Conditions

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability

Table 5. Temperature and V_{CC} Operating Condition of Intel® Embedded Flash Memory (J3 v. D)

Symbol	Parameter	Min	Max	Unit	Test Condition
T_A		-40.0	+85	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage	2.70	3.6	V	—
V_{CCQ}	V_{CCQ} Supply Voltage	2.70	3.6	V	—

5.3 Power Up/Down

This section provides an overview of system level considerations with regards to the flash device. It includes a brief description of power-up, power-down and decoupling design considerations.

5.3.1 Power-Up/Down Characteristics

To prevent conditions that could result in spurious program or erase operations, the power-up/power-down sequence shown in Table 6 is recommended. For DC voltage characteristics refer to Table 8. Note that each power supply must reach its minimum voltage range before applying/removing the next supply voltage.

Table 6. Power-Up/Down Sequence

<table>
<tr><th>Power Supply Voltage</th><th colspan="4">Power-UpSequence</th><th colspan="4">Power-Down Sequence</th></tr>
<tr><td>$V_{CC(min)}$</td><td>1st</td><td>1st</td><td rowspan="2">1st†</td><td rowspan="3">Sequencing not required†</td><td>3rd</td><td>2nd</td><td rowspan="2">2nd†</td><td rowspan="3">Sequencing not required†</td></tr>
<tr><td>$V_{CCQ(min)}$</td><td>2nd</td><td rowspan="2">2nd†</td><td>2nd</td><td rowspan="2">1st†</td></tr>
<tr><td>$V_{PEN(min)}$</td><td>3rd</td><td>2nd</td><td>1st</td><td>1st</td></tr>
</table>

† Power supplies connected or sequenced together.

Device inputs must not be driven until all supply voltages reach their minimum range. RP# should be low during power transitions.

5.3.2 Power Supply Decoupling

When the device is enabled, many internal conditions change. Circuits are energized, charge pumps are switched on, and internal voltage nodes are ramped. All of this internal activities produce transient signals. The magnitude of the transient signals depends on the device and system loading. To minimize the effect of these transient signals, a 0.1 µF ceramic capacitor is required across each VCC/VSS and VCCQ signal. Capacitors should be placed as close as possible to device connections.

Additionally, for every eight flash devices, a 4.7 µF electrolytic capacitor should be placed between VCC and VSS at the power supply connection. This 4.7 µF capacitor should help overcome voltage slumps caused by PCB (printed circuit board) trace inductance.

5.4 Reset

By holding the flash device in reset during power-up and power-down transitions, invalid bus conditions may be masked. The flash device enters reset mode when RP# is driven low. In reset, internal flash circuitry is disabled and outputs are placed in a high-impedance state. After return from reset, a certain amount of time is required before the flash device is able to perform normal operations. After return from reset, the flash device defaults to asynchronous page mode. If RP# is driven low during a program or erase operation, the program or erase operation will be aborted and the memory contents at the aborted block or address are no longer valid. See Figure 16, "AC Waveform for Reset Operation" on page 30 for detailed information regarding reset timings.

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6.0 Electrical Characteristics

6.1 DC Current Specifications

Table 7. DC Current Characteristics (Sheet 1 of 2)

Symbol	Parameter		Typ	Max	Unit	Test Conditions	Notes
	V_{CCQ}		2.7 - 3.6V				
	V_{CC}		2.7 - 3.6V				
I_{LI}	Input and V_{PEN} Load Current			±1	µA	V_{CC} = V_{CC} Max; V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	1
I_{LO}	Output Leakage Current			±10	µA	V_{CC} = V_{CC} Max; V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	1
I_{CCS}	V_{CC} Standby Current	32, 64, 128 Mbit	50	120	µA	CMOS Inputs, V_{CC} = V_{CC} Max; Vccq = VccqMax Device is disabled (see Table 15, "Chip Enable Truth Table" on page 32), RP# = V_{CCQ} ± 0.2 V	1,2,3
		256 Mbit	100	240			
		32, 64, 128 Mbit	0.71	2	mA	TTL Inputs, V_{CC} = V_{CC} Max, Vccq = VccqMax Device is disabled (see Table 15, "Chip Enable Truth Table" on page 32), RP# = V_{IH}	
		256 Mbit	1.42	4			
I_{CCD}	V_{CC} Power-Down Current		50	120	µA	RP# = GND ± 0.2 V, I_{OUT} (STS) = 0 mA	
I_{CCR}	V_{CC} Page Mode Read Current	4-Word Page	15	20	mA	CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max Device is enabled (see Table 15, "Chip Enable Truth Table" on page 32) f = 5 MHz, I_{OUT} = 0 mA	1,3
			24	29	mA	CMOS Inputs,V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max Device is enabled (see Table 15, "Chip Enable Truth Table" on page 32) f = 33 MHz, I_{OUT} = 0 mA	
		8-Word Page	10	15	mA	CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 8 word page mode reads. Device is enabled (see Table 15, "Chip Enable Truth Table" on page 32) f = 5 MHz, I_{OUT} = 0 mA	
			30	54	mA	CMOS Inputs,V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 8 word page mode reads. Device is enabled (see Table 15, "Chip Enable Truth Table" on page 32) f = 33 MHz, I_{OUT} = 0 mA	
I_{CCW}	V_{CC} Program or Set Lock-Bit Current		35	60	mA	CMOS Inputs, V_{PEN} = V_{CC}	1,4
			40	70	mA	TTL Inputs, V_{PEN} = V_{CC}	

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Table 7. DC Current Characteristics (Sheet 2 of 2)

V_{CCQ}		2.7 - 3.6V			Test Conditions	Notes
V_{CC}		2.7 - 3.6V				
Symbol	Parameter	Typ	Max	Unit		
I_{CCE}	V_{CC} Block Erase or Clear Block Lock-Bits Current	35	70	mA	CMOS Inputs, $V_{PEN} = V_{CC}$	1,4
		40	80	mA	TTL Inputs, $V_{PEN} = V_{CC}$	
I_{CCWS} I_{CCES}	V_{CC} Program Suspend or Block Erase Suspend Current		10	mA	Device is enabled (see Table 15, "Chip Enable Truth Table" on page 32)	1,5

Notes:
1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds). Contact Intel's Application Support Hotline or your local sales office for information about typical specifications.
2. Includes STS.
3. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL inputs are either V_{IL} or V_{IH}.
4. Sampled, not 100% tested.
5. I_{CCWS} and I_{CCES} are specified with the device selected. If the device is read or written while in erase suspend mode, the device's current draw is I_{CCR} and I_{CCWS}.

6.2 DC Voltage specifications

Table 8. DC Voltage Characteristics (Sheet 1 of 2)

V_{CCQ}		2.7 - 3.6 V			Test Conditions	Notes
V_{CC}		2.7 - 3.6 V				
Symbol	Parameter	Min	Max	Unit		
V_{IL}	Input Low Voltage	–0.5	0.8	V		2, 5, 6
V_{IH}	Input High Voltage	2.0	V_{CCQ} + 0.5V	V		2, 5, 6
V_{OL}	Output Low Voltage		0.4	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$ Min I_{OL} = 2 mA	1, 2
			0.2	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$ Min I_{OL} = 100 µA	
V_{OH}	Output High Voltage	0.85 × V_{CCQ}		V	$V_{CC} = V_{CCMIN}$ $V_{CCQ} = V_{CCQ}$ Min I_{OH} = –2.5 mA	1, 2
		V_{CCQ} – 0.2		V	$V_{CC} = V_{CCMIN}$ $V_{CCQ} = V_{CCQ}$ Min I_{OH} = –100 µA	
V_{PENLK}	V_{PEN} Lockout during Program, Erase and Lock-Bit Operations		2.2	V		2, 3

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Table 8. DC Voltage Characteristics (Sheet 2 of 2)

V_{CCQ}		2.7 - 3.6 V			Test Conditions	Notes
V_{CC}		2.7 - 3.6 V				
Symbol	**Parameter**	**Min**	**Max**	**Unit**		
V_{PENH}	V_{PEN} during Block Erase, Program, or Lock-Bit Operations	2.7	3.6	V		3
V_{LKO}	V_{CC} Lockout Voltage	2.0		V		4

Notes:

1. Includes STS.
2. Sampled, not 100% tested.
3. Block erases, programming, and lock-bit configurations are inhibited when $V_{PEN} \leq V_{PENLK}$, and not guaranteed in the range between V_{PENLK} (max) and V_{PENH} (min), and above V_{PENH} (max).
4. Block erases, programming, and lock-bit configurations are inhibited when $V_{CC} < V_{LKO}$, and not guaranteed in the range between V_{LKO} (min) and V_{CC} (min), and above V_{CC} (max).
5. Includes all operational modes of the device including standby and power-up sequences
6. Input/Output signals can undershoot to -1.0v referenced to V_{SS} and can overshoot to V_{CCQ} = 1.0v for duration of 2ns or less, the V_{CCQ} valid range is referenced to V_{SS}.

6.3 Capacitance

Table 9. Intel® Embedded Flash Memory (J3 v. D) Capacitance

Symbol	Parameter[1]		Type	Max	Unit	Condition[2]
C_{IN}	Input Capacitance	32, 64, 128 Mb	6	8	pF	V_{IN} = 0.0 V
		256 Mb	12	16		
C_{OUT}	Output Capacitance	32, 64, 128 Mb	8	12	pF	V_{OUT} = 0.0 V
		256 Mb	16	24		

Notes:

1. sampled. not 100% tested.
2. T_A = +25 °C, f = 1 MHZ

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7.0 AC Characteristics

Timing symbols used in the timing diagrams within this document conform to the following convention:

Figure 9. Timing Signal Naming Convention

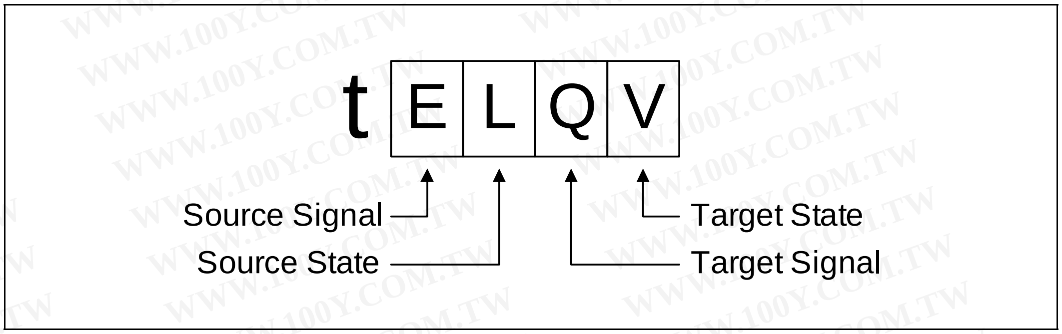

Figure 10. Timing Signal Name Decoder

Signal	Code	State	Code
Address	A	High	H
Data - Read	Q	Low	L
Data - Write	D	High-Z	Z
Chip Enable (CE#)	E	Low-Z	X
Output Enable (OE#)	G	Valid	V
Write Enable (WE#)	W	Invalid	I
Address Valid (ADV#)	V		
Reset (RST#)	P		
Clock (CLK)	C		
WAIT	T		

Note: Exceptions to this convention include tACC and tAPA. tACC is a generic timing symbol that refers to the aggregate initial-access delay as determined by tAVQV, tELQV, and tGLQV (whichever is satisfied last) of the flash device. tAPA is specified in the flash device's data sheet, and is the address-to-data delay for subsequent page-mode reads.

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7.1 Read Specifications

Table 10. Read Operations

Asynchronous Specifications V_{CC} = 2.7 V–3.6 V [(3)] and V_{CCQ} = 2.7 V–3.6 V[(3)]							
#	**Sym**	**Parameter**	**Density**	**Min**	**Max**	**Unit**	**Notes**
R1	t_{AVAV}	Read/Write Cycle Time	32 Mbit	75		ns	1,2
			64 Mbit	75			1,2
			128 Mbit	75			1,2
			256 Mbit	95			1,2
R2	t_{AVQV}	Address to Output Delay	32 Mbit		75	ns	1,2
			64 Mbit		75		1,2
			128 Mbit		75		1,2
			256 Mbit		95		1,2
R3	t_{ELQV}	CEx to Output Delay	32 Mbit		75	ns	1,2
			64 Mbit		75		1,2
			128 Mbit		75		1,2
			256 Mbit		95		1,2
R4	t_{GLQV}	OE# to Non-Array Output Delay			25	ns	1,2,4
R5	t_{PHQV}	RP# High to Output Delay	32 Mbit		150	ns	1,2
			64 Mbit		180		1,2
			128 Mbit		210		1,2
			256 Mbit		210		1,2
R6	t_{ELQX}	CEx to Output in Low Z	All	0		ns	1,2,5
R7	t_{GLQX}	OE# to Output in Low Z		0		ns	1,2,5
R8	t_{EHQZ}	CEx High to Output in High Z			25	ns	1,2,5
R9	t_{GHQZ}	OE# High to Output in High Z			15	ns	1,2,5
R10	t_{OH}	Output Hold from Address, CEx, or OE# Change, Whichever Occurs First		0		ns	1,2,5
R11	t_{ELFL}/t_{ELFH}	CEx Low to BYTE# High or Low			10	ns	1,2,5
R12	t_{FLQV}/t_{FHQV}	BYTE# to Output Delay			1	µs	1,2
R13	t_{FLQZ}	BYTE# to Output in High Z			1	µs	1,2,5
R14	t_{EHEL}	CEx High to CEx Low	All	0		ns	1,2,5
R15	t_{APA}	Page Address Access Time			25	ns	5, 6
R16	t_{GLQV}	OE# to Array Output Delay	All		25	ns	1,2,4

Notes:
1. CE_X low is defined as the first edge of CE0, CE1, CE2 or CE# that enables the device. CE_X high is defined at the first edge of CE0, CE1, CE2 or CE# that disables the device (see Table 15, "Chip Enable Truth Table" on page 32).
2. See AC Input/Output Reference Waveforms for the maximum allowable input slew rate.
3. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the first edge of CE0, CE1, CE2 or CE# that enables the device (see Table 15, "Chip Enable Truth Table" on page 32) without impact on t_{ELQV}.
4. See Figure 17, "AC Input/Output Reference Waveform" on page 31 and Figure 18, "Transient Equivalent Testing Load Circuit" on page 31 for testing characteristics.
5. Sampled, not 100% tested.
6. For devices configured to standard word/byte read mode, R15 (t_{APA}) will equal R2 (t_{AVQV}).

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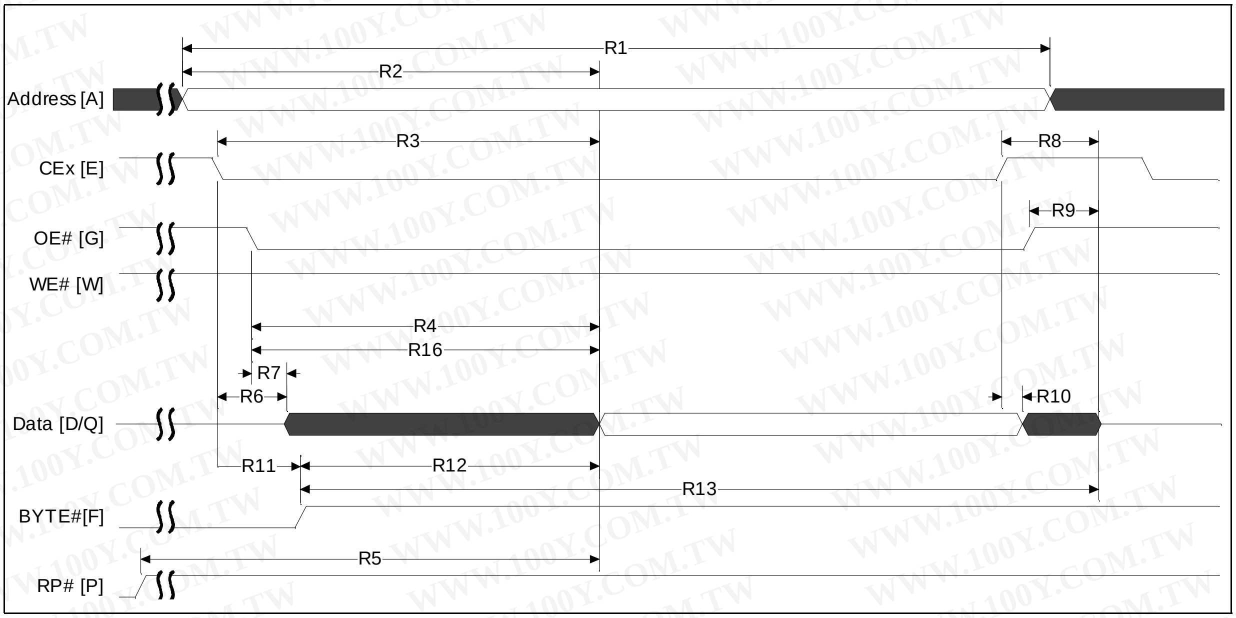
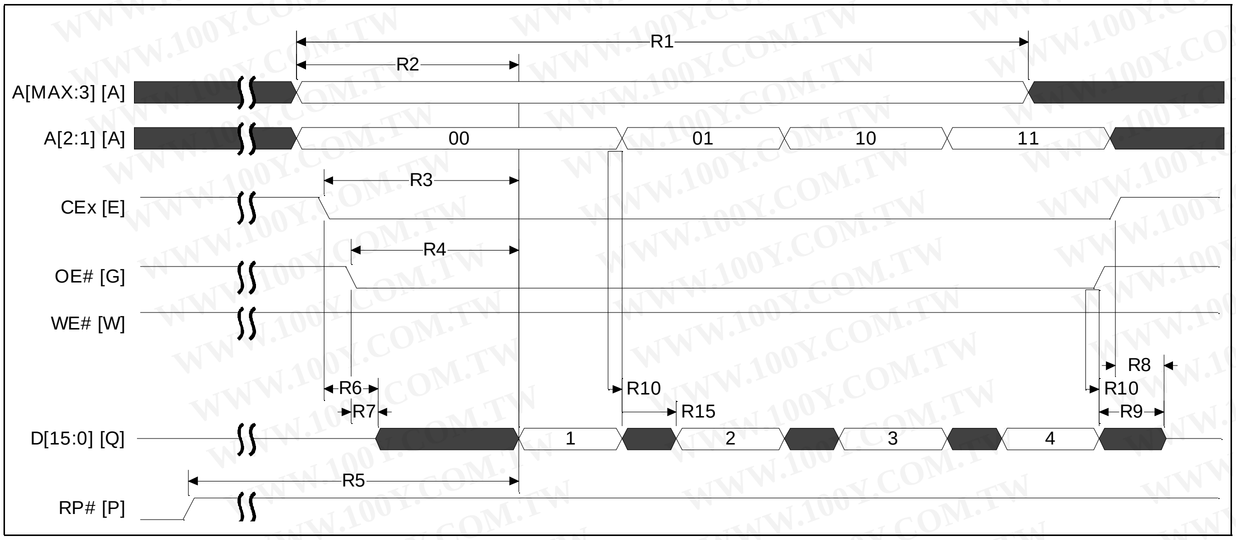
Figure 11. Single Word Asynchronous Read Waveform



Notes:

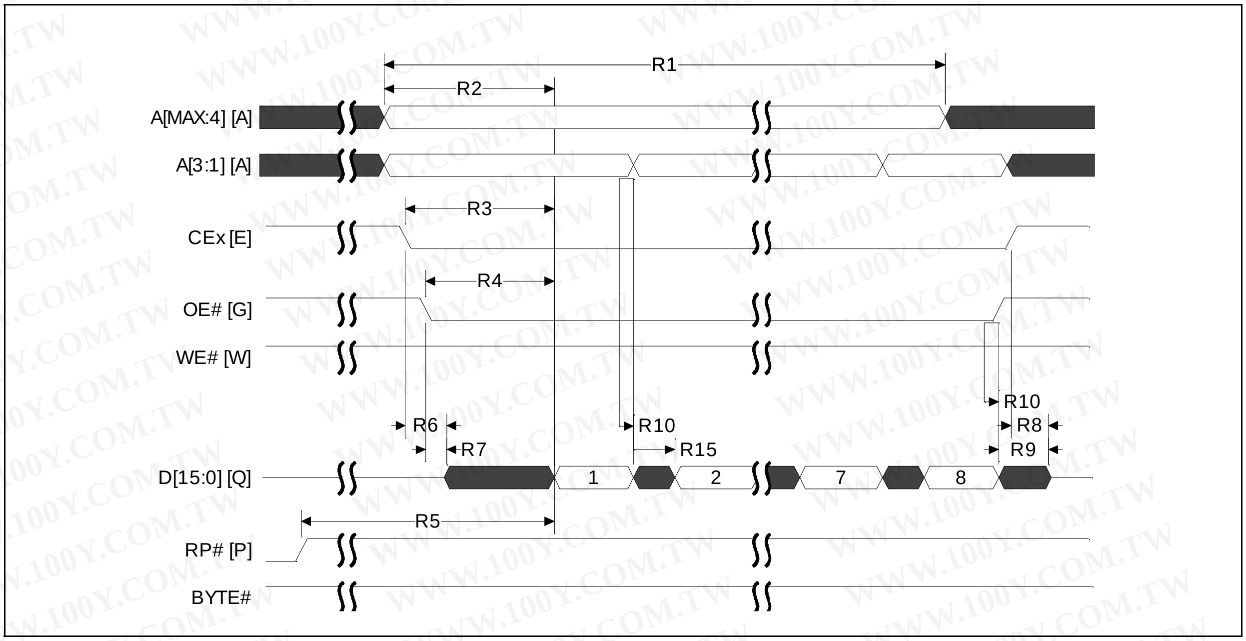
1. CE_X low is defined as the last edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 15, "Chip Enable Truth Table" on page 32).
2. When reading the flash array a faster t_{GLQV} (R16) applies. For non-array reads, R4 applies (i.e., Status Register reads, query reads, or device identifier reads).

Figure 12. 4-Word Asynchronous Page Mode Read Waveform



Note: CE_X low is defined as the last edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 15, "Chip Enable Truth Table" on page 32).

Figure 13. 8-Word Asynchronous Page Mode Read



Notes:

1. CE_X low is defined as the last edge of CE0, CE1, or CE2 that enables the device. CE_X high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 15, “Chip Enable Truth Table” on page 32).
2. In this diagram, BYTE# is asserted high

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7.2 Write Specifications

Table 11. Write Operations

#	Symbol	Parameter	Density	Valid for All Speeds Min	Valid for All Speeds Max	Unit	Notes
W1	t_{PHWL} (t_{PHEL})	RP# High Recovery to WE# (CE$_X$) Going Low	32 Mbit	150			1,2,3
			64 Mbit	180			
			128 Mbit	210			
W2	t_{ELWL} (t_{WLEL})	CE$_X$ (WE#) Low to WE# (CE$_X$) Going Low		0			1,2,4
W3	t_{WP}	Write Pulse Width		60			1,2,4
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE$_X$) Going High		50			1,2,5
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE$_X$) Going High		55			1,2,5
W6	t_{WHEH} (t_{EHWH})	CE$_X$ (WE#) Hold from WE# (CE$_X$) High		0		ns	1,2,
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE$_X$) High		0			1,2,
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE$_X$) High	All	0			1,2,
W9	t_{WPH}	Write Pulse Width High		30			1,2,6
W11	t_{VPWH} (t_{VPEH})	V_{PEN} Setup to WE# (CE$_X$) Going High		0			1,2,3
W12	t_{WHGL} (t_{EHGL})	Write Recovery before Read		35			1,2,7
W13	t_{WHRL} (t_{EHRL})	WE# (CE$_X$) High to STS Going Low			500		1,2,8
W15	t_{QVVL}	V_{PEN} Hold from Valid SRD, STS Going High		0			1,2,3,8,9

Notes:

CE$_X$ low is defined as the first edge of CE0, CE1, or CE2 that enables the device. CE$_X$ high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 15, "Chip Enable Truth Table" on page 32).

1. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to *AC Characteristics–Read-Only Operations*.
2. A write operation can be initiated and terminated with either CE$_X$ or WE#.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from CE$_X$ or WE# going low (whichever goes low last) to CE$_X$ or WE# going high (whichever goes high first). Hence, t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}.
5. Refer to Table 16, "Enhanced Configuration Register" on page 34 for valid A_{IN} and D_{IN} for block erase, program, or lock-bit configuration.
6. Write pulse width high (t_{WPH}) is defined from CE$_X$ or WE# going high (whichever goes high first) to CE$_X$ or WE# going low (whichever goes low first). Hence, t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}.
7. For array access, t_{AVQV} is required in addition to t_{WHGL} for any accesses after a write.
8. STS timings are based on STS configured in its RY/BY# default mode.
9. V_{PEN} should be held at V_{PENH} until determination of block erase, program, or lock-bit configuration success (SR[1,3,4,5] = 0).

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Figure 14. Asynchronous Write Waveform

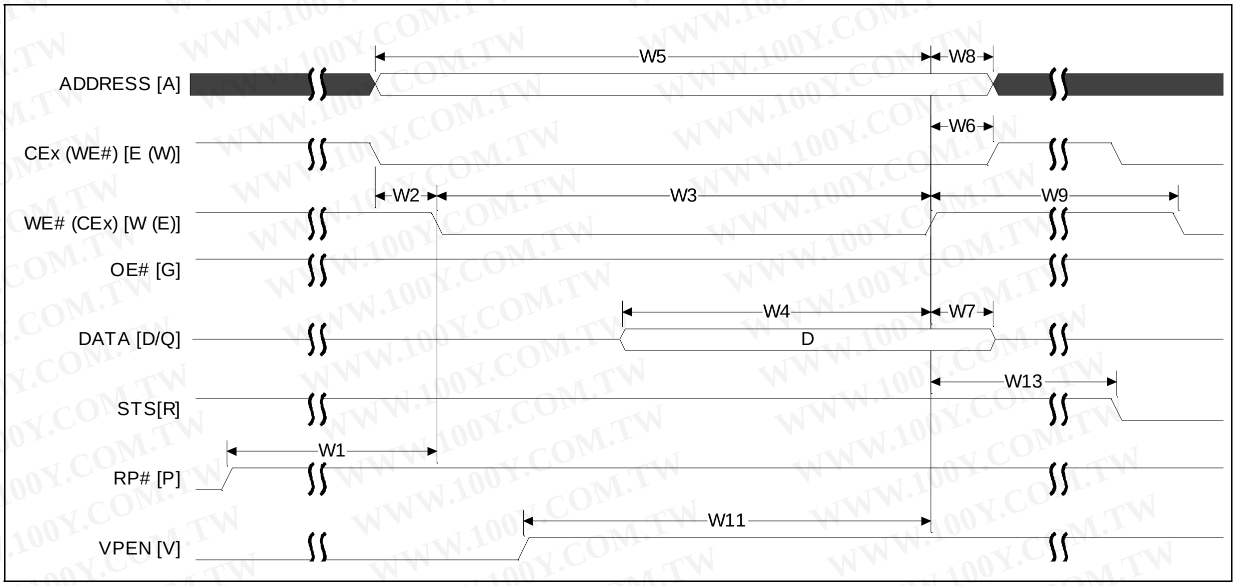
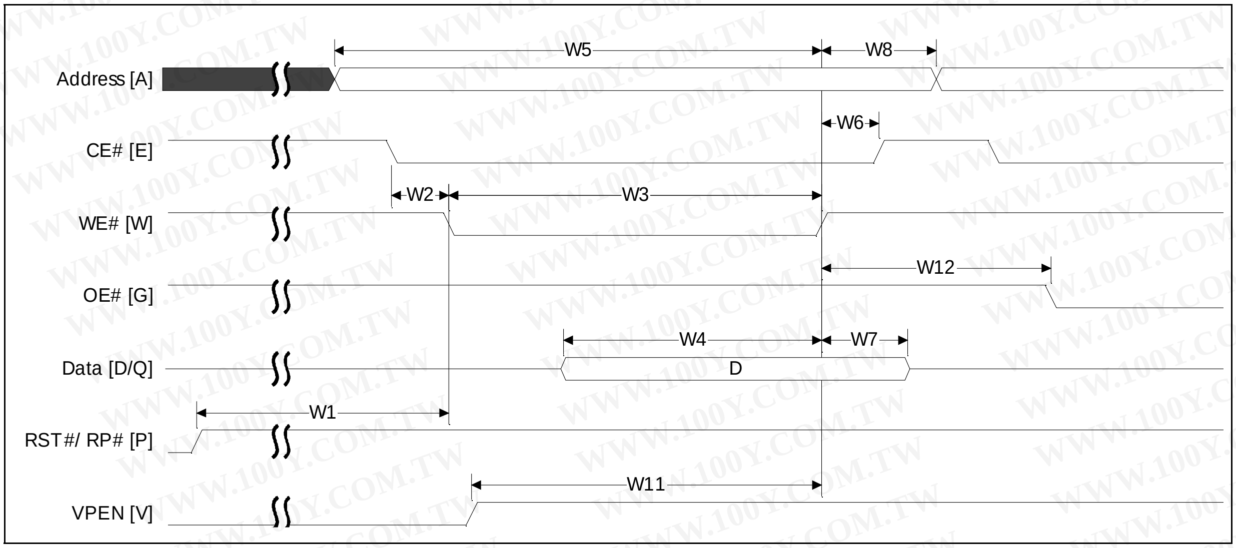


Figure 15. Asynchronous Write to Read Waveform



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7.3 Program, Erase, Block-Lock Specifications

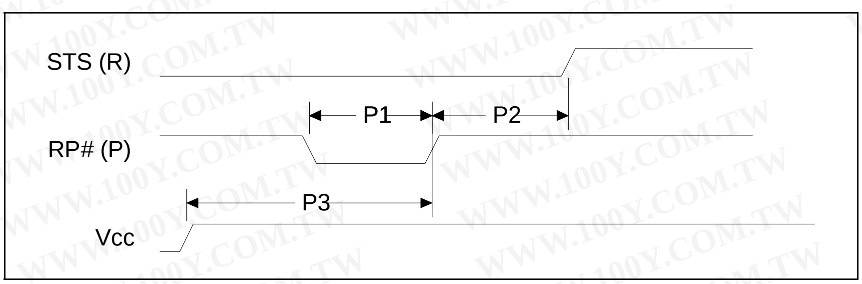
Table 12. Configuration Performance

#	Symbol	Parameter	Typ	Max[8]	Unit	Notes
W16		Write Buffer Byte Program Time (Time to Program 32 bytes/16 words)	128	654	µs	1,2,3,4,5,6,7
W16	t_{WHQV3} t_{EHQV3}	Byte Program Time (Using Word/Byte Program Command)	40	175	µs	1,2,3,4
		Block Program Time (Using Write to Buffer Command)	0.53	2.4	sec	1,2,3,4
W16	t_{WHQV4} t_{EHQV4}	Block Erase Time	1.0	4.0	sec	1,2,3,4
W16	t_{WHQV5} t_{EHQV5}	Set Lock-Bit Time	50	60	µs	1,2,3,4,9
W16	t_{WHQV6} t_{EHQV6}	Clear Block Lock-Bits Time	0.5	0.70	sec	1,2,3,4,9
W16	t_{WHRH1} t_{EHRH1}	Program Suspend Latency Time to Read	15	20	µs	1,2,3,9
W16	t_{WHRH} t_{EHRH}	Erase Suspend Latency Time to Read	15	20	µs	1,2,3,9
WY	t_{STS}	STS Pulse Width Low Time	500		ns	1

Notes:
1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. These performance numbers are valid for all speed versions.
3. Sampled but not 100% tested.
4. Excludes system-level overhead.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. Effective per-byte program time (t_{WHQV1}, t_{EHQV1}) is 4µs/byte (typical).
7. Effective per-word program time (t_{WHQV2}, t_{EHQV2}) is 8µs/word (typical).
8. Max values are measured at worst case temperature, data pattern and V_{CC} corner after 100k cycles (except as noted).
9. Max values are expressed at 25 °C/-40 °C.

7.4 Reset Specifications

Figure 16. AC Waveform for Reset Operation



Note: STS is shown in its default mode (RY/BY#)

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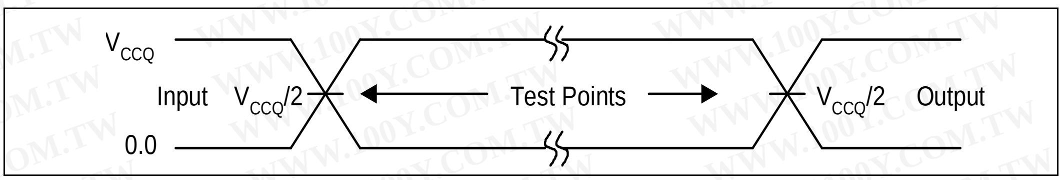
Table 13. Reset Specifications

#	Symbol	Parameter	Min	Max	Unit	Notes
P1	t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)	25		µs	1,2
P2	t_{PHRH}	RP# High to Reset during Block Erase, Program, or Lock-Bit Configuration		100	ns	1,3
P3	t_{VCCPH}	Vcc Power Valid to RP# de-assertion (high)	60		µs	

Notes:
1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, program, or lock-bit configuration operation is not executing then the minimum required RP# Pulse Low Time is 100 ns.
3. A reset time, t_{PHQV}, is required from the latter of STS (in RY/BY# mode) or RP# going high until outputs are valid.

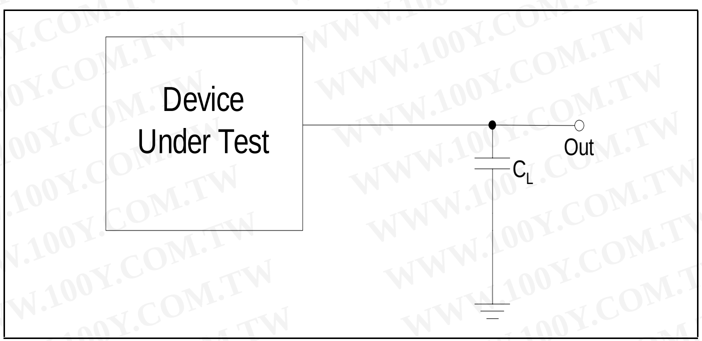
7.5 AC Test Conditions

Figure 17. AC Input/Output Reference Waveform



Note: AC test inputs are driven at V_{CCQ} for a Logic "1" and 0.0 V for a Logic "0." Input timing begins, and output timing ends, at $V_{CCQ}/2$ V (50% of V_{CCQ}). Input rise and fall times (10% to 90%) < 5 ns.

Figure 18. Transient Equivalent Testing Load Circuit



Note: C_L Includes Jig Capacitance

Figure 19. Test Configuration

Test Configuration	C_L (pF)
$V_{CCQ} = V_{CCQMIN}$	30

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8.0 Bus Interface

This section provides an overview of Bus operations. Basically, there are three operations you can do with flash memory: Read, Program (Write), and Erase. The on-chip Write State Machine (WSM) manages all erase and program algorithms. The system CPU provides control of all in-system read, write, and erase operations through the system bus. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. Table 14 summarizes the necessary states of each control signal for different modes of operations.

Table 14. Bus Operations

Mode	RP#	CE_x (1)	OE# (2)	WE# (2)	V_{PEN}	$DQ_{15:0}$ (3)	STS (Default Mode)	Notes
Async., Status, Query and Identifier Reads	V_{IH}	Enabled	V_{IL}	V_{IH}	X	D_{OUT}	High Z	4,6
Output Disable	V_{IH}	Enabled	V_{IH}	V_{IH}	X	High Z	High Z	
Standby	V_{IH}	Disabled	X	X	X	High Z	High Z	
Reset/Power-down	V_{IL}	X	X	X	X	High Z	High Z	
Command Writes	V_{IH}	Enabled	V_{IH}	V_{IL}	X	D_{IN}	High Z	6,7
Array Writes(8)	V_{IH}	Enabled	V_{IH}	V_{IL}	V_{PENH}	X	V_{IL}	8,5

Notes:
1. See Table 15 for valid CE_X Configurations.
2. OE# and WE# should never be asserted simultaneously. If done so, OE# overrides WE#.
3. DQ refers to DQ[7:0} when BYTE# is low and DQ[15:0] if BYTE# is high.
4. Refer to DC characteristics. When $V_{PEN} \leq V_{PENLK}$, memory contents can be read but not altered.
5. X should be V_{IL} or V_{IH} for the control pins and V_{PENLK} or V_{PENH} for V_{PEN}. For outputs, X should be V_{OL} or V_{OH}.
6. In default mode, STS is V_{OL} when the WSM is executing internal block erase, program, or a lock-bit configuration algorithm. It is V_{OH} (pulled up by an external pull up resistance ~= 10k) when the WSM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or reset power-down mode.
7. See Table 18, "Command Bus Operations" on page 36 for valid DIN (user commands) during a Write operation
8. Array writes are either program or erase operations. /

Table 15. Chip Enable Truth Table

CE2	CE1	CE0	DEVICE
V_{IL}	V_{IL}	V_{IL}	Enabled
V_{IL}	V_{IL}	V_{IH}	Disabled
V_{IL}	V_{IH}	V_{IL}	Disabled
V_{IL}	V_{IH}	V_{IH}	Disabled
V_{IH}	V_{IL}	V_{IL}	Enabled
V_{IH}	V_{IL}	V_{IH}	Enabled
V_{IH}	V_{IH}	V_{IL}	Enabled
V_{IH}	V_{IH}	V_{IH}	Disabled

Note: For single-chip applications, CE2 and CE1 can be connected to $_{GND}$.

The next few sections detail each of the basic flash operations and some of the advanced features available on flash memory.

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8.1 Bus Reads

Reading from flash memory outputs stored information to the processor or chipset, and does not change any contents. Reading can be performed an unlimited number of times. Besides array data, other types of data such as device information and device status is available from the flash.

To perform a bus read operation, CEx (refer to Table 15 on page 32) and OE# must be asserted. CEx is the device-select control; when active, it enables the flash memory device. OE# is the data-output control; when active, the addressed flash memory data is driven onto the I/O bus. For all read states, WE# and RP# must be de-asserted. See Section 9.2, "Read Operations" on page 38.

8.1.1 Asynchronous Page Mode Read

There are two Asynchronous Page mode configurations available on Intel® Embedded Flash Memory (J3 v. D), depending on the system design requirements:

- Four-Word Page mode: This is the default mode on power-up or reset. Array data can be sensed up to four words (8 Bytes) at a time.
- Eight-Word Page mode: Array data can be sensed up to eight words (16 Bytes) at a time. This mode must be enabled on power-up or reset by using the command sequence described in Table 18 on page 36. Address bits A[3:1] determine which word is output during a read operation, and A[3:0] determine which byte is output for a x8 bus width.

After the initial access delay, the first word out of the page buffer corresponds to the initial address. In Four-Word Page mode, address bits A[2:1] determine which word is output from the page buffer for a x16 bus width, and A[2:0] determine which byte is output from the page buffer for a x8 bus width. Subsequent reads from the device come from the page buffer. These reads are output on D[15:0] for a x16 bus width and D[7:0] for a x8 bus width after a minimum delay as long as A[2:0] (Four-Word Page mode) or A[3:0] (Eight-Word Page mode).

Data can be read from the page buffer multiple times, and in any order. In Four-Word Page mode, if address bits A[MAX:3] (A[MAX:4] for Eight-Word Page Mode) change at any time, or if CE# is toggled, the device will sense and load new data into the page buffer. Asynchronous Page mode is the default read mode on power-up or reset.

To perform a Page mode read after any other operation, the Read Array command must be issued to read from the flash array. Asynchronous Page mode reads are permitted in all blocks and are used to access register information. During register access, only one word is loaded into the page buffer.

8.1.1.1 Enhanced Configuration Register (ECR)

The Enhanced Configuration Register (ECR) is a volatile storage register that when addressed by the Set Enhanced Configuration Register command can select between Four-Word Page mode and Eight-Word Page mode. The ECR is volatile; all bits will be reset to default values when RP# is deasserted or power is removed from the device. To modify ECR settings, use the Set Enhanced Configuration Register command. The Set Enhanced Configuration Register command is written along with the configuration register value, which is placed on the lower 16 bits of the address bus A[15:0]. This is followed by a second write that confirms the operation and again presents the Enhanced Configuration Register data on the address bus. After executing this command, the device returns to Read Array mode.

The ECR is shown in Table 16. 8-word page mode Command Bus-Cycle is captured in Table 17.

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Note: For forward compatibility reasons, if the 8-word Asynchronous Page mode is used on Intel® Embedded Flash Memory (J3 v. D), a Clear Status Register command must be executed after issuing the Set Enhanced Configuration Register command. See Table 17 for further details.

Table 16. Enhanced Configuration Register

Reserved		Page Length	Reserved												
ECR 15	ECR 14	ECR 13	ECR 12	ECR 11	ECR 10	ECR 9	ECR 8	ECR 7	ECR 6	ECR 5	ECR 4	ECR 3	ECR 2	ECR 1	ECR 0

BITS	DESCRIPTION	NOTES
ECR[15:14]	RFU	All bits should be set to 0.
ECR[13]	• "1" = 8 Word Page mode • "0" = 4 Word Page mode	
ECR[12:0]	RFU	All bits should be set to 0.

Table 17. Asynchronous 8-Word Page Mode Command Bus-Cycle Definition

Command	Bus Cycles Required	First Bus Cycle			Second Bus Cycle		
		Oper	Addr(1)	Data	Oper	Addr(1)	Data
Set Enhanced Configuration Register (Set ECR)	2	Write	ECD	0060h	Write	ECD	0004h

1. X = Any valid address within the device. ECD = Enhanced Configuration Register Data

8.1.2 Output Disable

With CEx asserted, and OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output signals D[15:0] are placed in a high-impedance state.

8.2 Bus Writes

Writing or Programming to the device, is where the host writes information or data into the flash device for non-volatile storage. When the flash device is programmed, 'ones' are changed to 'zeros'. 'Zeros' cannot be programed back to 'ones'. To do so, an erase operation must be performed. Writing commands to the Command User Interface (CUI) enables various modes of operation, including the following:

- Reading of array data
- Common Flash Interface (CFI) data
- Identifier codes, inspection, and clearing of the Status Register
- Block Erasure, Program, and Lock-bit Configuration (when V_{PEN} = V_{PENH})

Erasing is performed on a block basis – all flash cells within a block are erased together. Any information or data previously stored in the block will be lost. Erasing is typically done prior to programming. The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte/Word Program command requires the command and address of the location to be written. Set Block Lock-Bit commands require the command and block within the device to be locked. The Clear Block Lock-Bits command requires the command and address within the device to be cleared.

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The CUI does not occupy an addressable memory location. It is written when the device is enabled and WE# is active. The address and data needed to execute a command are latched on the rising edge of WE# or the first edge of CE0, CE1, or CE2 that disables the device (see Table 15 on page 32). Standard microprocessor write timings are used.

8.3 Standby

CE0, CE1, and CE2 can disable the device (see Table 15 on page 32) and place it in standby mode. This manipulation of CEx substantially reduces device power consumption. D[15:0] outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, program, or lock-bit configuration, the WSM continues functioning, and consuming active power until the operation completes.

8.3.1 Reset/Power-Down

RP# at V_{IL} initiates the reset/power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state, and turns off numerous internal circuits. RP# must be held low for a minimum of t_{PLPH}. Time t_{PHQV} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and Status Register is set to 0080h.

During Block Erase, Program, or Lock-Bit Configuration modes, RP#-low will abort the operation. In default mode, STS transitions low and remains low for a maximum time of t_{PLPH} + t_{PHRH} until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially corrupted after a program or partially altered after an erase or lock-bit configuration. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during Block Erase, Program, or Lock-Bit Configuration modes. If a CPU reset occurs with no flash memory reset, proper initialization may not occur because the flash memory may be providing status information instead of array data. Intel® Flash memories allow proper initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

8.4 Device Commands

When the V_{PEN} voltage ≤ V_{PENLK}, only read operations from the Status Register, CFI, identifier codes, or blocks are enabled. Placing V_{PENH} on V_{PEN} additionally enables block erase, program, and lock-bit configuration operations. Device operations are selected by writing specific commands to the Command User Interface (CUI). The CUI does not occupy an addressable memory location. It is the mechanism through which the flash device is controlled.

A command sequence is issued in two consecutive write cycles - a Setup command followed by a Confirm command. However, some commands are single-cycle commands consisting of a setup command only. Generally, commands that alter the contents of the flash device, such as Program or Erase, require at least two write cycles to guard against inadvertent changes to the flash device. Flash commands fall into two categories: Basic Commands and Extended Commands. Basic commands are recognized by all Intel® Flash devices, and are used to perform common flash operations such as selecting the read mode, programming the array, or erasing blocks. Extended commands are product-dependant; they are used to perform additional features such as software block locking. Table 18 describes all applicable commands on Intel® Embedded Flash Memory (J3 v. D).

Table 18. Command Bus Operations

	Command	Setup Write Cycle		Confirm Write Cycle	
		Address Bus	Data Bus	Address Bus[3]	Data Bus
Registers	Program Enhanced Configuration Register	Register Data [1,2]	0060h	Register Data	0004h
Registers	Program OTP Register	Device Address [1]	00C0h	Register Offset	Register Data
Registers	Clear Status Register	Device Address[2]	0050h	---	---
Registers	Program STS Configuration Register	Device Address[2]	00B8h	Device Address	Register Data
Read Modes	Read Array	Device Address [2]	00FFh	---	---
Read Modes	Read Status Register	Device Address[2]	0070h	---	---
Read Modes	Read Identifier Codes (Read Device Information)	Device Address[2]	0090h	---	---
Read Modes	CFI Query	Device Address[2]	0098h	---	---
Program and Erase	Word/Byte Program	Device Address[1]	0040h/ 0010h	Device Address[4]	Array Data
Program and Erase	Buffered Program	Word Address[1]	00E8h	Device Address	00D0h
Program and Erase	Block Erase	Block Address[1]	0020h	Block Address	00D0h
Program and Erase	Program/Erase Suspend	Device Address[1]	00B0h	---	---
Program and Erase	Program/Erase Resume	Device Address[1]	00D0h	---	---
Security	Lock Block	Block Address[1]	0060h	Block Address	0001h
Security	Unlock Block	Device Address[2]	0060h	Device Address	00D0h

Notes:
1. In case of 256 Mb device (2x128), the command should be issued to the base address of the die
2. In case of 256 Mb device (2x128), the command sequence must be repeated for each die at its base address
3. In case of 256 Mb device (2x128), keep the second cycle to the same address. (i.e. Do not toggle A24 for the second cycle)
4. In case of 256 Mb device (2x128), the second cycle must be writtne to the Block Address and Offset address to be programmed

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9.0 Flash Operations

This section describes the operational features of flash memory. Operations are command-based, wherein command codes are first issued to the device, then the device performs the desired operation. All command codes are issued to the device using bus-write cycles (see Chapter 8.0, “Bus Interface”). A complete list of available command codes can be found in Appendix A, “Device Command Codes”.

9.1 Status Register

The Status Register (SR) is an 8-bit, read-only register that indicates device status and operation errors. To read the Status Register, issue the Read Status Register command. Subsequent reads output Status Register information on DQ[7:0], and 00h on DQ[15:8].

SR *status bits* are set and cleared by the device. SR *error bits* are set by the device, but must be cleared using the Clear Status Register command. Upon power-up or exit from reset, the Status Register defaults to 80h. Page-mode reads are not supported in this read mode. Status Register contents are latched on the falling edge of OE# or the first edge of CEx that enables the device. OE# must toggle to V_{IH} or the device must be disabled before further reads to update the Status Register latch. The Read Status Register command functions independently of V_{PEN} voltage.
Table 19 shows Status Register bit definitions.

Table 19. Status Register Bit Definitions

<table>
<tr><th colspan="4">Status Register (SR)</th><th colspan="4">Default Value = 80h</th></tr>
<tr><td>Ready Status</td><td>Erase Suspend Status</td><td>Erase Error</td><td>Program Error</td><td>Program /Erase Voltage Error</td><td>Program Suspend Status</td><td>Block-Locked Error</td><td>Reserved</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>

<table>
<tr><th>Bit</th><th colspan="2">Name</th><th>Description</th></tr>
<tr><td>7</td><td colspan="2">Ready Status</td><td>0 = Device is busy; SR[6:0] are invalid (Not driven);
1 = Device is ready; SR[6:0] are valid.</td></tr>
<tr><td>6</td><td colspan="2">Erase Suspend Status</td><td>0 = Erase suspend not in effect.
1 = Erase suspend in effect.</td></tr>
<tr><td>5</td><td>Erase Error</td><td rowspan="2">Command Sequence Error</td><td rowspan="2">SR5 SR4
0 0 = Program or erase operation successful.
0 1 = Program error - operation aborted.
1 0 = Erase error - operation aborted.
1 1 = Command sequence error - command aborted.</td></tr>
<tr><td>4</td><td>Program Error</td></tr>
<tr><td>3</td><td colspan="2">V_{PEN} Error</td><td>0 = V_{PEN} within acceptable limits during program or erase operation.
1 = V_{PEN} not within acceptable limits during program or erase operation. Operation aborted.</td></tr>
<tr><td>2</td><td colspan="2">Program Suspend Status</td><td>0 = Program suspend not in effect.
1 = Program suspend in effect.</td></tr>
<tr><td>1</td><td colspan="2">Block-Locked Error</td><td>0 = Block NOT locked during program or erase - operation successful.
1 = Block locked during program or erase - operation aborted.</td></tr>
<tr><td>0</td><td colspan="2">Reserved</td><td>Not used - Reserved for future use.</td></tr>
</table>

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9.1.1 Clearing the Status Register

The Status Register (SR) contain status and error bits which are set by the device. SR *status bits* are cleared by the device, however SR *error bits* are cleared by issuing the Clear Status Register command (see Table 20). Resetting the device also clears the Status Register.

Table 20. Clear Status Register Command Bus-Cycle

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Clear Status Register	Device Address	0050h	---	---

In case of 256 Mb device (2x128), the command sequence must be repeated for each die at its base address.

Issuing the Clear Status Register command places the device in Read Status Register mode.

Note: Care should be taken to avoid Status Register ambiguity. If a command sequence error occurs while in an Erase Suspend condition, the Status Register will indicate a Command Sequence error by setting SR4 and SR5. When the erase operation is resumed (and finishes), any errors that may have occurred during the erase operation will be masked by the Command Sequence error. To avoid this situation, clear the Status Register prior to resuming a suspended erase operation. The Clear Status Register command functions independent of the voltage level on VPEN.

9.2 Read Operations

Four types of data can be read from the device: array data, device information, CFI data, and device status. Upon power-up or return from reset, the device defaults to Read Array mode. To change the device's read mode, the appropriate command must be issued to the device. Table 21 shows the command codes used to configure the device for the desired read mode. The following sections describe each read mode.

Table 21. Read Mode Command Bus-Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Read Array	Device Address	00FFh	---	---
Read Status Register	Device Address	0070h	---	---
Read Device Information	Device Address	0090h	---	---
CFI Query	Device Address	0098h	---	---

In case of 256 Mb device (2x128), the command sequence must be repeated for each die at its base address.

9.2.1 Read Array

Upon power-up or return from reset, the device defaults to Read Array mode. Issuing the Read Array command places the device in Read Array mode. Subsequent reads output array data on DQ[15:0]. The device remains in Read Array mode until a different read command is issued, or a program or erase operation is performed, in which case, the read mode is automatically changed to Read Status.

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To change the device to Read Array mode while it is programming or erasing, first issue the Suspend command. After the operation has been suspended, issue the Read Array command. When the program or erase operation is subsequently resumed, the device will automatically revert back to Read Status mode.

Note: Issuing the Read Array command to the device while it is actively programming or erasing causes subsequent reads from the device to output invalid data. Valid array data is output only after the program or erase operation has finished.

The Read Array command functions independent of the voltage level on VPEN.

9.2.2 Read Status Register

Issuing the Read Status Register command places the device in Read Status Register mode. Subsequent reads output Status Register information on DQ[7:0], and 00h on DQ[15:8]. The device remains in Read Status Register mode until a different read-mode command is issued. Performing a program, erase, or block-lock operation also changes the device's read mode to Read Status Register mode.

The Status Register is updated on the falling edge of CE#, or OE# when CE# is low. Status Register contents are valid only when SR7 = 1. When WSM is active, SR7 indicates the WSM's state and SR[6:0] are in high-Z state.

The Read Status Register command functions independent of the voltage level on VPEN.

9.2.3 Read Device Information

Issuing the Read Device Information command places the device in Read Device Information mode. Subsequent reads output device information on DQ[15:0] (see Table 22). In the case of the 256 Mbit device (2 x 128), the command should be issued to the base address of the die.

Table 22. Device Information Summary

Device Information	Word Address	DQ[15:0]
Device Manufacturer Code (Intel)	Device Base Address + 00h	0089h
Device ID Code	Device Base Address + 01h	(See Appendix B, "ID Codes")
Block Lock Status[1]	Block Base Address + 02h	DQ0 = 0 Unlocked DQ0 = 1 Locked DQ[15:1] = RFU
OTP Lock Register[1]	Device Base Address + 80h	Lock Register 0 Data
OTP Register - Factory Segment[1]	Device Base Address + 81h to 84h	Factory-Programmed Data
OTP Register - User-Programmable Segment[1]	Device Base Address + 85h to 88h	User Data

The device remains in Read Device Information mode until a different read command is issued. Also, performing a program, erase, or block-lock operation changes the device to Read Status Register mode.

The Read Device Information command functions independent of the voltage level on VPEN.

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9.2.4 CFI Query

The query table contains an assortment of flash product information such as block size, density, allowable command sets, electrical specifications, and other product information. The data contained in this table conforms to the Common Flash Interface (CFI) protocol.

Issuing the CFI Query command places the device in CFI Query mode. Subsequent reads output CFI information on DQ[15:0] (see Appendix D, "Common Flash Interface").

The device remains in CFI Query mode until a different read command is issued, or a program or erase operation is performed, which changes the read mode to Read Status Register mode.

The CFI Query command functions independent of the voltage level on VPEN.

9.3 Programming Operations

Programming the flash array changes 'ones' to 'zeros'. To change zeros to ones, an erase operation must be performed (see Section 9.4, "Block Erase Operations"). Only one programming operation can occur at a time. Programming is permitted during an erase suspend.

Information is programmed into the flash array by issuing the appropriate command. Intel® Embedded Flash Memory (J3 v. D) supports two different programming methods: Byte/Word and Write-to-Buffer. Table 23 shows the two-cycle command sequences used for each method. In the case of the 256 Mbit device (2 x 128), the command should be issued to the base address of the die.

Table 23. Program Command Bus-Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Single-Word/Byte Program	Device Address	0040h/0010h	Device Address	Array Data
Buffered Program	Device Address	00E8h	Device Address	00D0h

Note: All programming operations require the addressed block to be unlocked, and a valid VPEN voltage applied throughout the programming operation. Otherwise, the programming operation will abort, setting the appropriate Status Register error bit(s).

The following sections describe each programming method.

9.3.1 Single-Word/Byte Programming

Array programming is performed by first issuing the Single-Word/Byte Program command. This is followed by writing the desired data at the desired array address. The read mode of the device is automatically changed to Read Status Register mode, which remains in effect until another read-mode command is issued.

During programming, STS and the Status Register indicate a busy status (SR7 = 0). Upon completion, STS and the Status Register indicate a ready status (SR7 = 1). The Status Register should be checked for any errors (SR4), then cleared.

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Note: Issuing the Read Array command to the device while it is actively programming causes subsequent reads from the device to output invalid data. Valid array data is output only after the program operation has finished.

Standby power levels are not be realized until the programming operation has finished. Also, asserting RP# aborts the programming operation, and array contents at the addressed location are indeterminate. The addressed block should be erased, and the data re-programmed. If a Single-Word/Byte program is attempted when the corresponding block lock-bit is set, SR1 and SR4 will be set.

9.3.2 Buffered Programming

Buffered programming operations simultaneous program multiple words into the flash memory array, significantly reducing effective word-write times. User-data is first written to a write buffer, then programmed into the flash memory array in buffer-size increments. Appendix C, "Flow Charts" contains a flow chart of the buffered-programming operation.

Note: Optimal performance and power consumption is realized only by aligning the start address on 32-word boundaries (i.e., A[4:0] = 0b00000). Crossing a 32-word boundary during a buffered programming operation can cause programming time to double.

To perform a buffered programming operation, first issue the Buffered Program setup command at the desired starting address. The read mode of the device/addressed partition is automatically changed to Read Status Register mode.

Polling SR7 determines write-buffer availability (0 = not available, 1 = available). If the write buffer is not available, re-issue the setup command and check SR7; repeat until SR7 = 1.

Next, issue the word count at the desired starting address. The word count represents the total number of words to be written into the write buffer, minus one. This value can range from 00h (one word) to a maximum of 1Fh (32 words). Exceeding the allowable range causes an abort.

Following the word count, the write buffer is filled with user-data. Subsequent bus-write cycles provide addresses and data, up to the word count. All user-data addresses must lie between <starting address> and <starting address + word count>, otherwise the WSM continues to run as normal but, user may advertently change the content in unexpected address locations.

Note: User-data is programmed into the flash array at the address issued when filling the write buffer.

After all user-data is written into the write buffer, issue the confirm command. If a command other than the confirm command is issued to the device, a command sequence error occurs and the operation aborts.

After issuing the confirm command, write-buffer contents are programmed into the flash memory array. The Status Register indicates a busy status (SR7 = 0) during array programming.

Note: Issuing the Read Array command to the device while it is actively programming or erasing causes subsequent reads from the device to output invalid data. Valid array data is output only after the program or erase operation has finished.

Upon completion of array programming, the Status Register indicates ready (SR7 = 1). A full Status Register check should be performed to check for any programming errors, then cleared by using the Clear Status Register command.

Additional buffered programming operations can be initiated by issuing another setup command, and repeating the buffered programming bus-cycle sequence. However, any errors in the Status Register must first be cleared before another buffered programming operation can be initiated.

9.4 Block Erase Operations

Erasing a block changes 'zeros' to 'ones'. To change ones to zeros, a program operation must be performed (see Section 9.3, "Programming Operations"). Erasing is performed on a block basis - an entire block is erased each time an erase command sequence is issued. Once a block is fully erased, all addressable locations within that block read as logical ones (FFFFh). Only one block-erase operation can occur at a time, and *is not* permitted during a program suspend.

To perform a block-erase operation, issue the Block Erase command sequence at the desired block address. Table 24, "Block-Erase Command Bus-Cycle" on page 42 shows the two-cycle Block Erase command sequence.

Table 24. Block-Erase Command Bus-Cycle

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Block Erase	Device Address	0020h	Block Address	00D0h

In case of 256 Mb device (2x128), the command should be issued to the base address of the die

Note: A block-erase operation requires the addressed block to be unlocked, and a valid voltage applied to VPEN throughout the block-erase operation. Otherwise, the operation will abort, setting the appropriate Status Register error bit(s).

The Erase Confirm command latches the address of the block to be erased. The addressed block is preconditioned (programmed to all zeros), erased, and then verified. The read mode of the device is automatically changed to Read Status Register mode, and remains in effect until another read-mode command is issued.

During a block-erase operation, STS and the Status Register indicates a busy status (SR7 = 0). Upon completion, STS and the Status Register indicates a ready status (SR7 = 1). The Status Register should be checked for any errors, then cleared. If any errors did occur, subsequent erase commands to the device are ignored unless the Status Register is cleared.

The only valid commands during a block erase operation are Read Array, Read Device Information, CFI Query, and Erase Suspend. After the block-erase operation has completed, any valid command can be issued.

Note: Issuing the Read Array command to the device while it is actively erasing causes subsequent reads from the device to output invalid data. Valid array data is output only after the block-erase operation has finished.

Standby power levels are not be realized until the block-erase operation has finished. Also, asserting RP# aborts the block-erase operation, and array contents at the addressed location are indeterminate. The addressed block should be erased before programming within the block is attempted.

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9.5 Suspend and Resume

An erase or programming operation can be suspended to perform other operations, and then subsequently resumed. Table 25 shows the Suspend and Resume command bus-cycles.

Note: All erase and programming operations require the addressed block to remain unlocked with a valid voltage applied to VPEN throughout the suspend operation. Otherwise, the block-erase or programming operation will abort, setting the appropriate Status Register error bit(s). Also, asserting RP# aborts suspended block-erase and programming operations, rendering array contents at the addressed location(s) indeterminate.

Table 25. Suspend and Resume Command Bus-Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Suspend	Device Address	00B0h	---	---
Resume	Device Address	00D0h	---	---

In case of 256 Mb device (2x128), the command should be issued to the base address of the die

To suspend an on-going erase or program operation, issue the Suspend command to any device address. The program or erase operation suspends at pre-determined points during the operation after a delay of t_{SUSP}. Suspend is achieved when STS (in RY/BY# mode) goes high, SR[7,6] = 1 (erase-suspend) or SR[7,2] = 1 (program-suspend).

Note: Issuing the Suspend command does not change the read mode of the device. The device will be in Read Status Register mode from when the erase or program command was first issued, unless the read mode was changed prior to issuing the Suspend command.

Not all commands are allowed when the device is suspended. Table 26 shows which device commands are allowed during Program Suspend or Erase Suspend.

Table 26. Valid Commands During Suspend (Sheet 1 of 2)

Device Command	Program Suspend	Erase Suspend
STS Configuration	Allowed	Allowed
Read Array	Allowed	Allowed
Read Status Register	Allowed	Allowed
Clear Status Register	Allowed	Allowed
Read Device Information	Allowed	Allowed
CFI Query	Allowed	Allowed
Word Program	Not Allowed	Allowed
Buffered Program	Not Allowed	Allowed
Block Erase	Not Allowed	Not Allowed
Program Suspend	Not Allowed	Allowed
Erase Suspend	Not Allowed	Not Allowed
Program/Erase Resume	Allowed	Allowed

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Table 26. Valid Commands During Suspend (Sheet 2 of 2)

Device Command	Program Suspend	Erase Suspend
Lock Block	Not Allowed	Not Allowed
Unlock Block	Not Allowed	Not Allowed
Program OTP Register	Not Allowed	Not Allowed

During Suspend, array-read operations are not allowed in blocks being erased or programmed.

A block-erase under program-suspend is not allowed. However, word-program under erase-suspend is allowed, and can be suspended. This results in a simultaneous erase-suspend/ program-suspend condition, indicated by SR[7,6,2] = 1.

To resume a suspended program or erase operation, issue the Resume command to any device address. The read mode of the device is automatically changed to Read Status Register. The operation continues where it left off, STS (in RY/BY# mode) goes low, and the respective Status Register bits are cleared.

When the Resume command is issued during a simultaneous erase-suspend/ program-suspend condition, the programming operation is resumed first. Upon completion of the programming operation, the Status Register should be checked for any errors, and cleared. The resume command must be issued again to complete the erase operation. Upon completion of the erase operation, the Status Register should be checked for any errors, and cleared.

9.6 Status Signal (STS)

The STATUS (STS) signal can be configured to different states using the STS Configuration command (Table 27). Once the STS signal has been configured, it remains in that configuration until another Configuration command is issued or RP# is asserted low. Initially, the STS signal defaults to RY/BY# operation where RY/BY# low indicates that the WSM is busy. RY/BY# high indicates that the state machine is ready for a new operation or suspended. Table 28 displays possible STS configurations.

Table 27. STS Configuration Register

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
STS Configuration	Device Address[1]	00B8h	Device Address[2]	Register Data

Notes:
1. In case of 256 Mb device (2x128), the command sequence must be repeated for each die at its base address
2. In case of 256 Mb device (2x128), keep the second cycle to the same address. (ie. Do not toggle A24 for the second cycle)

To reconfigure the STATUS (STS) signal to other modes, the Configuration command is given followed by the desired configuration code. The three alternate configurations are all pulse mode for use as a system interrupt as described in the following paragraphs. For these configurations, bit 0 controls Erase Complete interrupt pulse, and bit 1 controls Program Complete interrupt pulse. Supplying the 0x00 configuration code with the Configuration command resets the STS signal to the default RY/BY# level mode. The Configuration command may only be given when the device is not busy or suspended. Check SR.7 for device status. An invalid configuration code will result in SR.4 and SR.5 being set.

Note: STS Pulse mode is not supported in the Clear Lock Bits and Set Lock Bit commands

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Table 28. STS Configuration Coding Definitions

D7	D6	D5	D4	D3	D2	D1	D0
Reserved						Pulse on Program Complete (1)	Pulse on Erase Complete (1)

D[1:0] = STS Configuration Codes	Notes
00 = default, level mode; device ready indication	Controls HOLD to a memory controller to prevent accessing a flash memory subsystem while any flash device's WSM is busy.
01 = pulse on Erase Complete	Generates a system interrupt pulse when any flash device in an array has completed a block erase. Helpful for reformatting blocks after file system free space reclamation or "cleanup."
10 = pulse on Program Complete	Not supported on this device.
11 = pulse on Erase or Program Complete	Generates system interrupts to trigger servicing of flash arrays when either erase or program operations are completed, when a common interrupt service routine is desired.

Notes:
1. When configured in one of the pulse modes, STS pulses low with a typical pulse width of 500 ns.
2. An invalid configuration code will result in both SR4 and SR5 being set.
3. Reserved bits are invalid should be ignored.

9.7 Security and Protection

Intel® Embedded Flash Memory (J3 v. D) device offer both hardware and software security features. Block lock operations, PRs and VPEN allow users to implement various levels of data protection.

9.7.1 Normal Block Locking

Intel® Embedded Flash Memory (J3 v. D) has the unique capability of Flexible Block Locking (locked blocks remain locked upon reset or power cycle): All blocks are unlocked at the factory. Blocks can be locked individually by issuing the Set Block Lock Bit command sequence to any address within a block. Once locked, blocks remain locked when power is removed, or when the device is reset.

All locked blocks are unlocked simultaneously by issuing the Clear Block Lock Bits command sequence to any device address. Locked blocks cannot be erased or programmed. Table 29 summarizes the command bus-cycles.

Table 29. Block Locking Command Bus-Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Set Block Lock Bit	Block Address[1]	0060h	Block Address	0001h
Clear Block Lock Bits	Device Address[2]	0060h	Device Address	00D0h

Notes:
1. In case of 256 Mb device (2x128), the command should be issued to the base address of the die
2. In case of 256 Mb device (2x128), the command sequence must be repeated for each die at its base address

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After issuing the Set Block Lock Bit setup command or Clear Block Lock Bits setup command, the device's read mode is automatically changed to Read Status Register mode. After issuing the confirm command, completion of the operation is indicated by STS (in RY/BY# mode) going high and SR7 = 1.

Blocks cannot be locked or unlocked while programming or erasing, or while the device is suspended. Reliable block lock and unlock operations occur only when V_{CC} and V_{PEN} are valid. When $V_{PEN} \leq V_{PENLK}$, block lock-bits cannot be changed.

When the set lock-bit operation is complete, SR4 should be checked for any error. When the clear lock-bit operation is complete, SR5 should be checked for any error. Errors bits must be cleared using the Clear Status Register command.

Block lock-bit status can be determined by first issuing the Read Device Information command, and then reading from <block base address> + 02h. DQ0 indicates the lock status of the addressed block (0 = unlocked, 1 = locked).

9.7.2 Configurable Block Locking

One of the unique new features on the Intel® Embedded Flash Memory (J3 v. D), non-existent on the previous generations of this product family, is the ability to protect and/or secure the user's system by offering multiple level of securities: Non-Volatile Temporary; Non-Volatile Semi-Permanently or Non-Volatile Permanently. For additional information and collateral request, please contact your filed representative.

9.7.3 OTP Protection Registers

Intel® Embedded Flash Memory (J3 v. D) includes a 128-bit Protection Register (PR) that can be used to increase the security of a system design. For example, the number contained in the PR can be used to "match" the flash component with other system components such as the CPU or ASIC, hence preventing device substitution.

The 128-bits of the PR are divided into two 64-bit segments:

- One segment is programmed at the Intel factory with a unique unalterable 64-bit number.
- The other segment is left blank for customer designers to program as desired. Once the customer segment is programmed, it can be locked to prevent further programming.

9.7.4 Reading the OTP Protection Register

The Protection Register is read in Identification Read mode. The device is switched to this mode by issuing the Read Identifier command (0090h). Once in this mode, read cycles from addresses shown in Table 30 or Table 31 retrieve the specified information. To return to Read Array mode, write the Read Array command (00FFh).

9.7.5 Programming the OTP Protection Register

Protection Register bits are programmed using the two-cycle Protection Program command. The 64-bit number is programmed 16 bits at a time for word-wide configuration and eight bits at a time for byte-wide configuration. First write the Protection Program Setup command, 00C0h. The next write to the device will latch in address and data and program the specified location. The allowable addresses are shown in Table 30, "Word-Wide Protection Register Addressing" on page 47 or Table 31, "Byte-Wide Protection Register Addressing" on page 48. See Figure 29, "Protection Register Programming Flowchart" on page 59. Any attempt to address Protection

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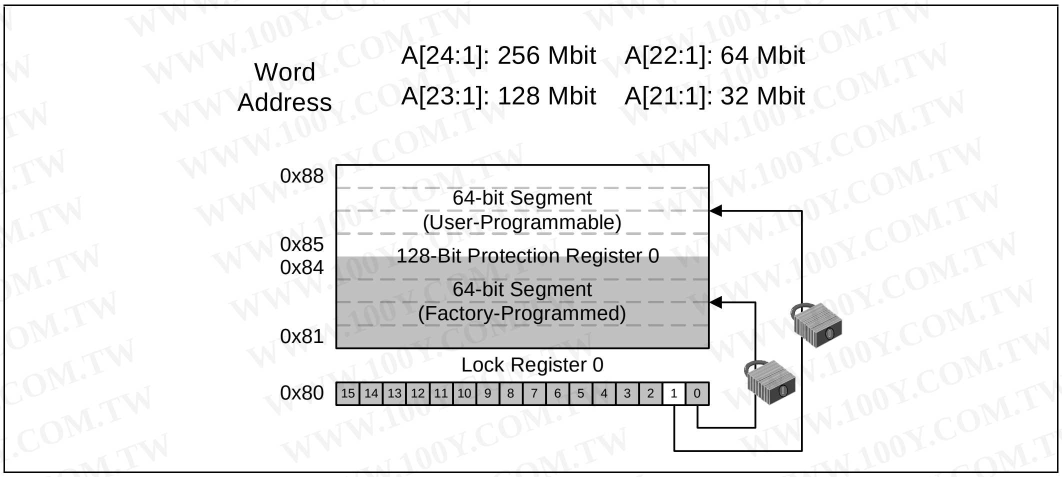
Program commands outside the defined PR address space will result in a Status Register error (SR.4 will be set). Attempting to program a locked PR segment will result in a Status Register error (SR.4 and SR.1 will be set).

9.7.6 Locking the OTP Protection Register

The user-programmable segment of the Protection Register is lockable by programming Bit 1 of the Protection Lock Register (PLR) to 0. Bit 0 of this location is programmed to 0 at the Intel factory to protect the unique device number. Bit 1 is set using the Protection Program command to program “0xFFFD” to the PLR. After these bits have been programmed, no further changes can be made to the values stored in the Protection Register. Protection Program commands to a locked section will result in a Status Register error (SR.4 and SR.1 will be set). PR lockout state is not reversible.

Figure 20. Protection Register Memory Map



Note: A0 is not used in x16 mode when accessing the protection register map. See Table 30 for x16 addressing. If x8 mode A0 is used, see Table 31 for x8 addressing.

Table 30. Word-Wide Protection Register Addressing

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
LOCK	Both	1	0	0	0	0	0	0	0
0	Factory	1	0	0	0	0	0	0	1
1	Factory	1	0	0	0	0	0	1	0
2	Factory	1	0	0	0	0	0	1	1
3	Factory	1	0	0	0	0	1	0	0
4	User	1	0	0	0	0	1	0	1
5	User	1	0	0	0	0	1	1	0
6	User	1	0	0	0	0	1	1	1
7	User	1	0	0	0	1	0	0	0

Note: All address lines not specified in the above table must be 0 when accessing the Protection Register (i.e., A[MAX:9] = 0.)

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Table 31. Byte-Wide Protection Register Addressing

Byte	Use	A8	A7	A6	A5	A4	A3	A2	A1	A0
LOCK	Both	1	0	0	0	0	0	0	0	0
LOCK	Both	1	0	0	0	0	0	0	0	1
0	Factory	1	0	0	0	0	0	0	1	0
1	Factory	1	0	0	0	0	0	0	1	1
2	Factory	1	0	0	0	0	0	1	0	0
3	Factory	1	0	0	0	0	0	1	0	1
4	Factory	1	0	0	0	0	0	1	1	0
5	Factory	1	0	0	0	0	0	1	1	1
6	Factory	1	0	0	0	0	1	0	0	0
7	Factory	1	0	0	0	0	1	0	0	1
8	User	1	0	0	0	0	1	0	1	0
9	User	1	0	0	0	0	1	0	1	1
A	User	1	0	0	0	0	1	1	0	0
B	User	1	0	0	0	0	1	1	0	1
C	User	1	0	0	0	0	1	1	1	0
D	User	1	0	0	0	0	1	1	1	1
E	User	1	0	0	0	1	0	0	0	0
F	User	1	0	0	0	1	0	0	0	1

Note: All address lines not specified in the above table must be 0 when accessing the Protection Register, i.e., A[MAX:9] = 0.

9.7.7 VPP / VPEN Protection

When it's necessary to protect the entire array, global protection can be achieved using a hardware mechanism. using VPP or VPEN. Whenever a valid voltage is present on VPP or VPEN, blocks within the main flash array can be erased or programmed. By grounding VPP or VPEN, blocks within the main array cannot be altered – attempts to program or erase blocks will fail resulting in the setting of the appropriate error bit in the Status Register. By holding VPP or VPEN low, absolute write protection of all blocks in the array can be achieved.

Appendix A Device Command Codes

For a complete definition on device operations refer to Section 8.4, "Device Commands" on page 35. The list of all applicable commands are included here one more time for the convenience.

Table 32. Command Bus Operations for Intel® Embedded Flash Memory (J3 v. D)

	Command	Setup Write Cycle		Confirm Write Cycle	
		Address Bus	Data Bus	Address Bus[3]	Data Bus
Registers	Program Enhanced Configuration Register	Register Data [1,2]	0060h	Register Data	0004h
	Program OTP Register	Device Address [1]	00C0h	Register Offset	Register Data
	Clear Status Register	Device Address[2]	0050h	---	---
	Program STS Configuration Register	Device Address[2]	00B8h	Device Address	Register Data
Read Modes	Read Array	Device Address [2]	00FFh	---	---
	Read Status Register	Device Address[2]	0070h	---	---
	Read Identifier Codes (Read Device Information)	Device Address[2]	0090h	---	---
	CFI Query	Device Address[2]	0098h	---	---
Program and Erase	Word/Byte Program	Device Address[1]	0040h/ 0010h	Device Address[4]	Array Data
	Buffered Program	Word Address[1]	00E8h	Device Address	00D0h
	Block Erase	Block Address[1]	0020h	Block Address	00D0h
	Program/Erase Suspend	Device Address[1]	00B0h	---	---
	Program/Erase Resume	Device Address[1]	00D0h	---	---
Security	Lock Block	Block Address[1]	0060h	Block Address	0001h
	Unlock Block	Device Address[2]	0060h	Device Address	00D0h

Notes:
1. In case of 256 Mb device (2x128), the command should be issued to the base address of the die
2. In case of 256 Mb device (2x128), the command sequence must be repeated for each die at its base address
3. In case of 256 Mb device (2x128), keep the second cycle to the same address. (i.e. Do not toggle A24 for the second cycle)
4. In case of 256 Mb device (2x128), the second cycle must be writtne to the Block Address and Offset address to be programmed

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Appendix B ID Codes

Table 33. Read Identifier Codes

Code		Address	Data
Device Code	32-Mbit	00001	0016
Device Code	64-Mbit	00001	0017
Device Code	128-Mbit	00001	0018
Device Code	256- Mbit	00001	001D

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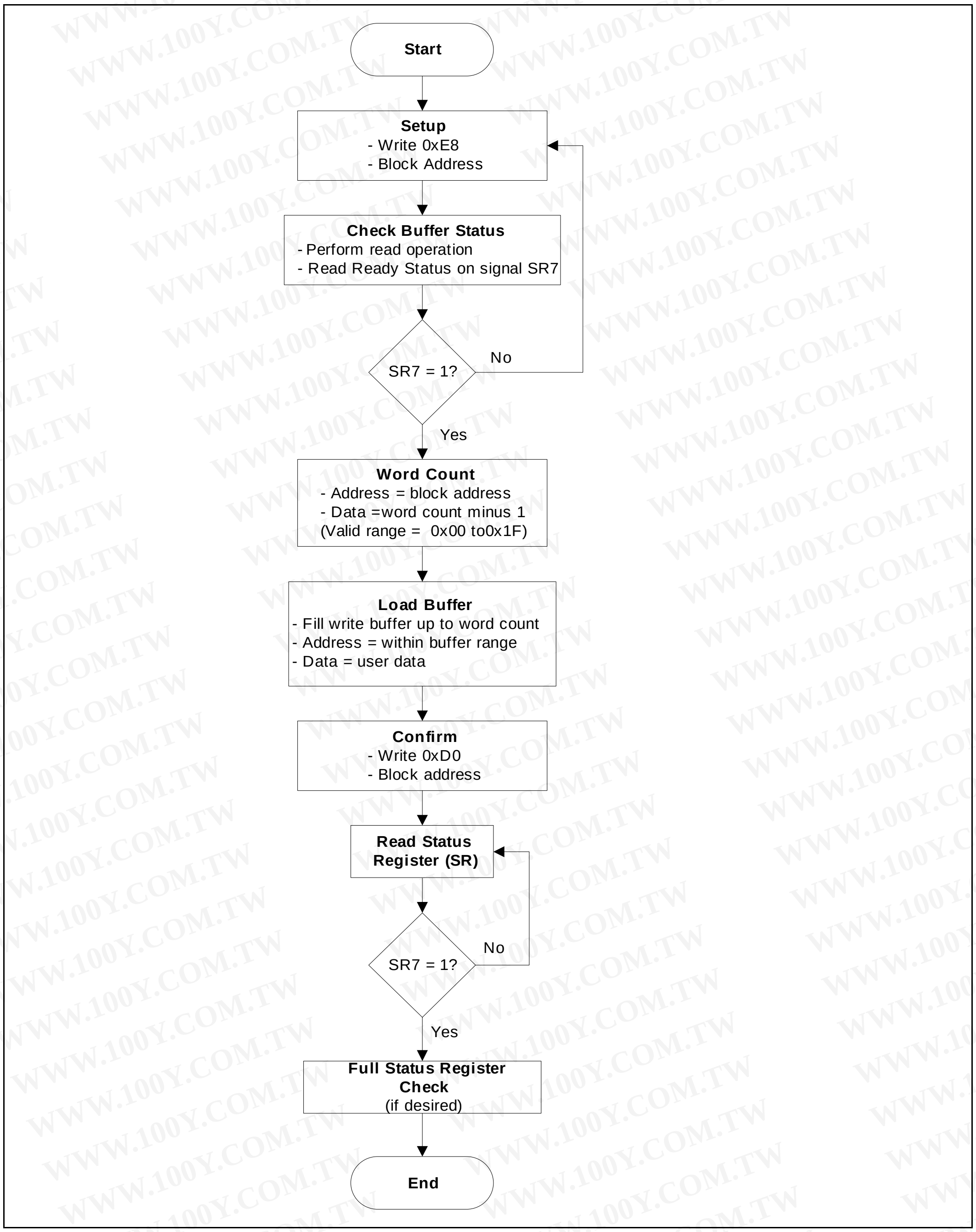
Appendix C Flow Charts

C.1 Write to Buffer

Figure 21. Write to Buffer Flowchart



C.2 Status Register

Figure 22. Status Register Flowchart

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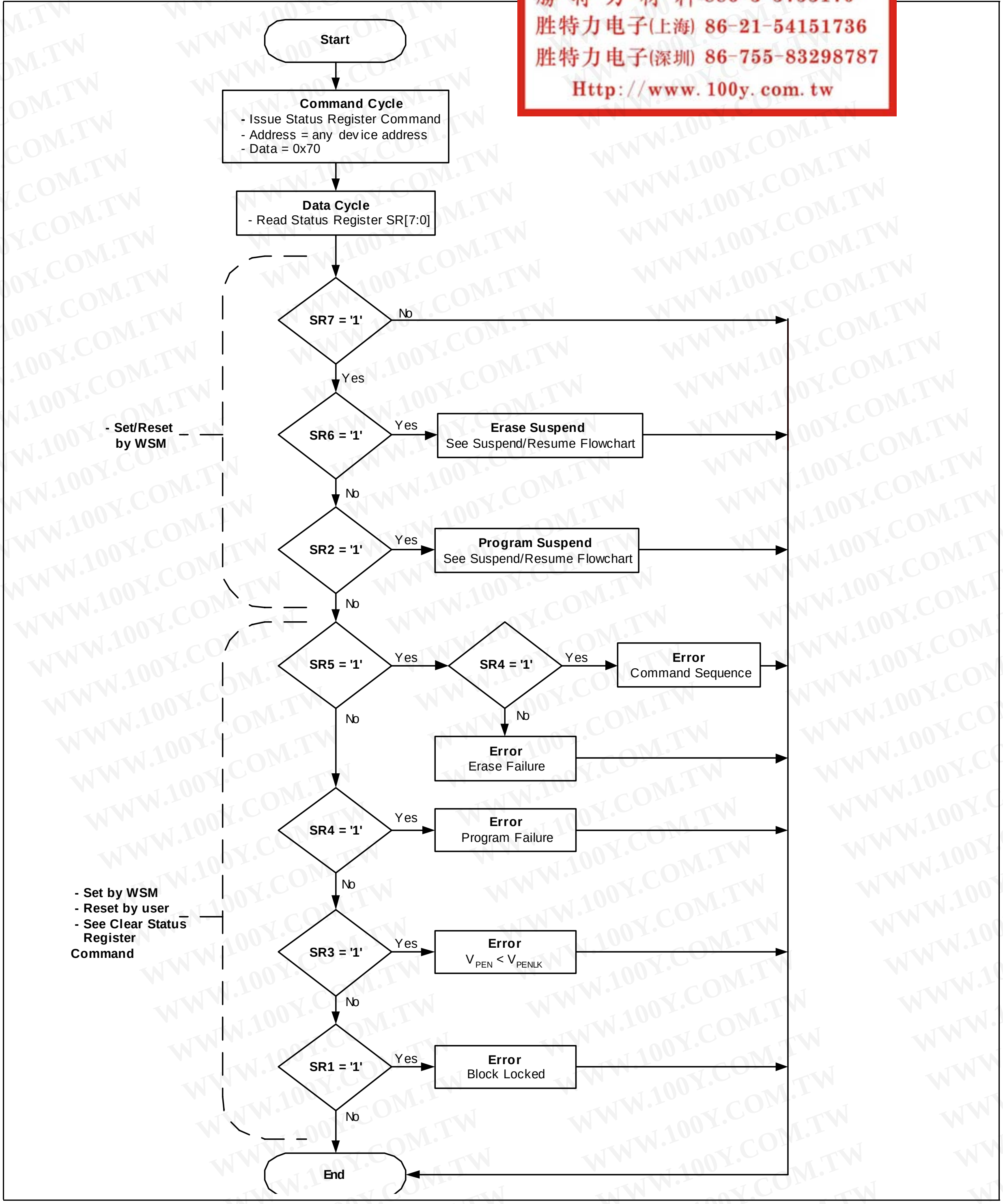
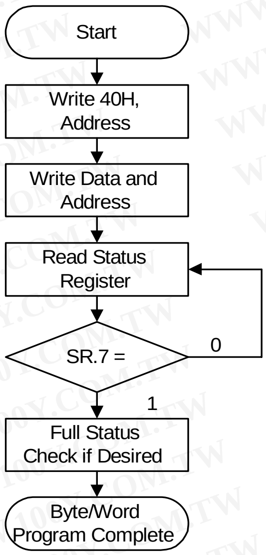


C.3 Byte/Word Programming

Figure 23. Byte/Word Program Flowchart



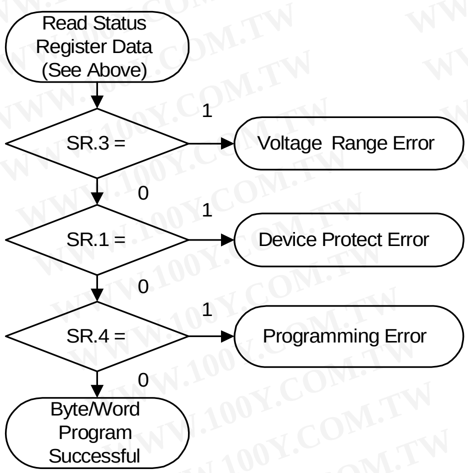
Bus Operation	Command	Comments
Write	Setup Byte/ Word Program	Data = 40H Addr = Location to Be Programmed
Write	Byte/Word Program	Data = Data to Be Programmed Addr = Location to Be Programmed
Read (Note 1)		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

1. Toggling OE# (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.

SR full status check can be done after each program operation, or after a sequence of programming operations.

Write FFH after the last program operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = Programming to Voltage Error Detect
Standby		Check SR.1 1 = Device Protect Detect RP# = V_{IH}, Block Lock-Bit Is Set Only required for systems implemeting lock-bit configuration.
Standby		Check SR.4 1 = Programming Error

Toggling OE# (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are programmed before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

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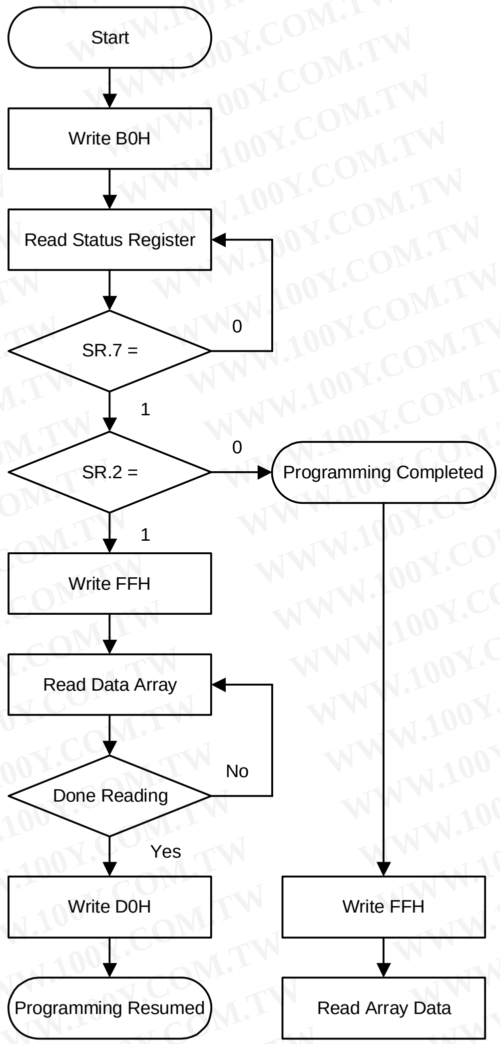
C.4 Program Suspend/Resume

Figure 24. Program Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 - WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Programming Suspended 0 = Programming Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array locations other than that being programmed.
Write	Program Resume	Data = D0H Addr = X

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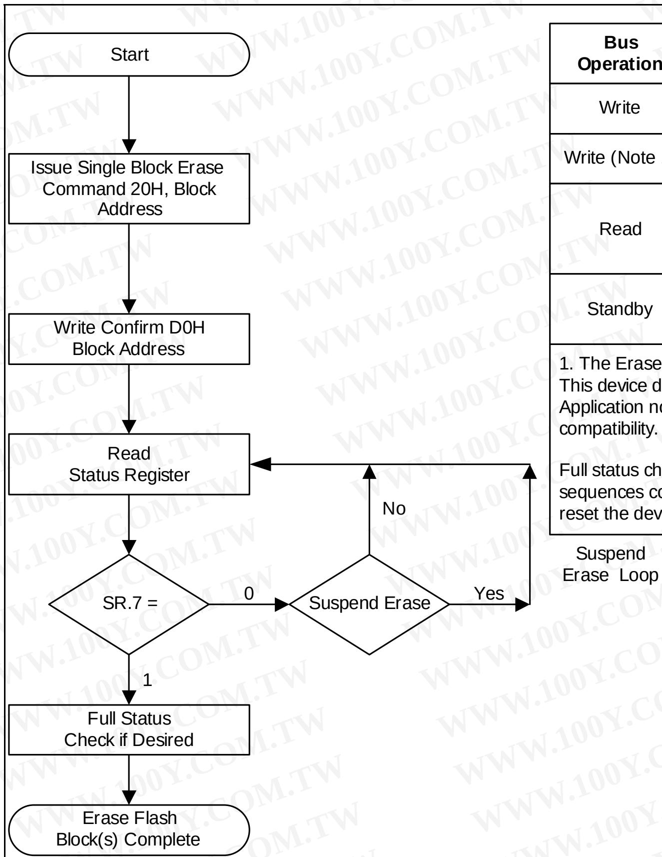
C.5 Block Erase

Figure 25. Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Block	Data = 20H Addr = Block Address
Write (Note 1)	Erase Confirm	Data = D0H Addr = Block Address
Read		Status register data With the device enabled, OE# low updates SR Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

1. The Erase Confirm byte must follow Erase Setup. This device does not support erase queuing. Please see Application note AP-646 For software erase queuing compatibility.

Full status check can be done after all erase and write sequences complete. Write FFH after the last operation to reset the device to read array mode.

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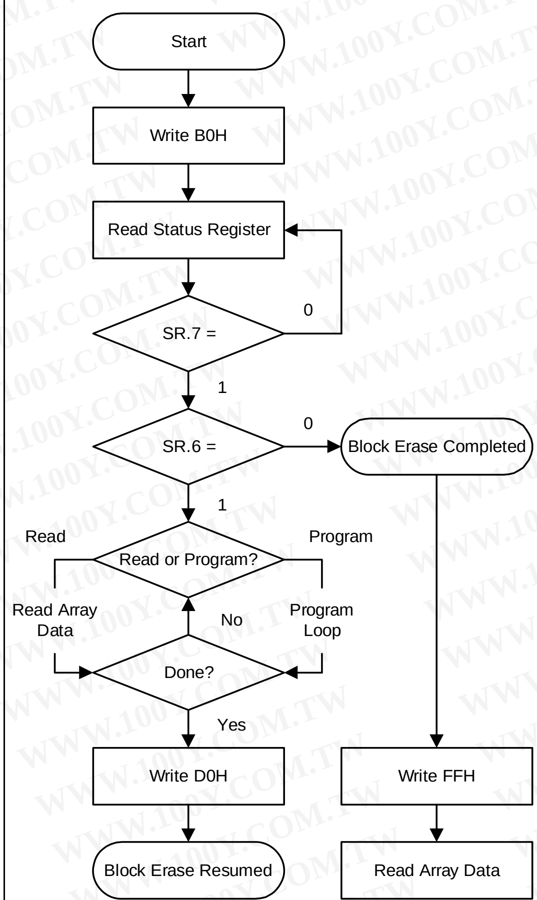
C.6 Block Erase Suspend/Resume

Figure 26. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 - WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

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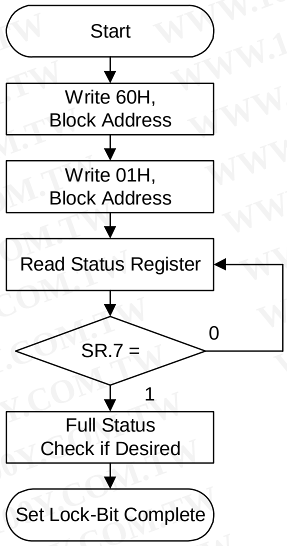
C.7 Block Locking

Figure 27. Set Block Lock-Bit Flowchart



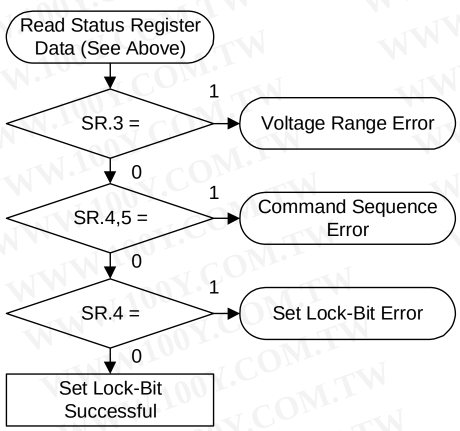
Bus Operation	Command	Comments
Write	Set Block Lock-Bit Setup	Data = 60H Addr =Block Address
Write	Set Block Lock-Bit Confirm	Data = 01H Addr = Block Address
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent lock-bit operations.

Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations.

Write FFH after the last lock-bit set operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = Programming Voltage Error Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Lock-Bit Error

SR.5, SR.4 and SR.3 are only cleared by the Clear Status Register command, in cases where multiple lock-bits are set before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

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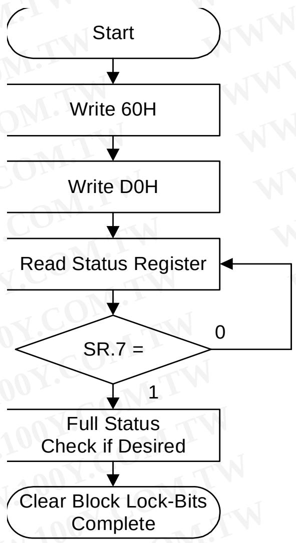
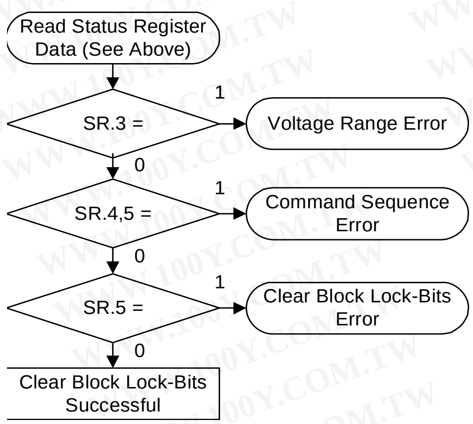
C.8 Unlock Block

Figure 28. Clear Lock-Bit Flowchart



Bus Operation	Command	Comments
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block or Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the clear lock-bits operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = Programming Voltage Error Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error
SR.5, SR.4, and SR.3 are only cleared by the Clear Status Register command. If an error is detected, clear the status register before attempting retry or other error recovery.		

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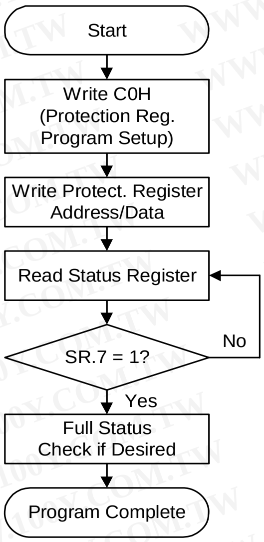
C.9 OTP Protection Register Programming

Figure 29. Protection Register Programming Flowchart



Bus Operation	Command	Comments
Write	Protection Program Setup	Data = C0H
Write	Protection Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

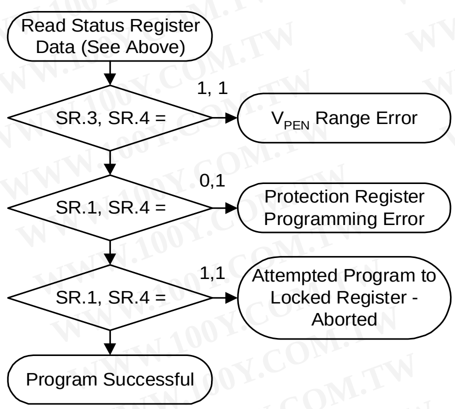
Protection Program operations can only be addressed within the protection register address space. Addresses outside the defined space will return an error.

Repeat for subsequent programming operations.

SR Full Status Check can be done after each program or after a sequence of program operations.

Write FFH after the last program operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		SR.1 SR.3 SR.4 0 1 1 V_{PEN} Low
Standby		0 0 1 Prot. Reg. Prog. Error
Standby		1 0 1 Register Locked: Aborted

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.1, SR.3 and SR.4 are only cleared by the Clear Staus Register Command, in cases of multiple protection register program operations before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

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Appendix D Common Flash Interface

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. It allows flash vendors to standardize their existing interfaces for long-term compatibility.

This appendix defines the data structure or "database" returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component. The Query is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI.

D.1 Query Structure Output

The Query "database" allows system software to gain information for controlling the flash component. This section describes the device's CFI-compliant interface that allows the host system to access Query data.

Query data are always presented on the lowest-order data outputs (D[7:0]) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two bytes of the Query structure, "Q" and "R" in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00H data on upper bytes. Thus, the device outputs ASCII "Q" in the low byte (D[7:0]) and 00h in the high byte (D[15:8]).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the "h" suffix has been dropped. In addition, since the upper byte of word-wide devices is always "00h," the leading "00" has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

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Table 34. Summary of Query Structure Output as a Function of Device and Mode

Device Type/ Mode	Query start location in maximum device bus width addresses	Query data with maximum device bus width addressing			Query data with byte addressing		
		Hex Offset	Hex Code	ASCII Value	Hex Offset	Hex Code	ASCII Value
x16 device	10h	10:	0051	"Q"	20:	51	"Q"
x16 mode		11:	0052	"R"	21:	00	"Null"
		12:	0059	"Y"	22:	52	"R"
x16 device					20:	51	"Q"
x8 mode	N/A(1)	N/A(1)			21:	51	"Q"
					22:	52	"R"

Note:
1. The system must drive the lowest order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing, where these lower addresses are not toggled by the system, is "Not Applicable" for x8-configured devices.

Table 35. Example of Query Structure Output of a x16- and x8-Capable Device

Word Addressing			Byte Addressing		
Offset	Hex Code	Value	Offset	Hex Code	Value
A_{15}–A_0	$D15$–D_0		A_7–A_0	D_7–D_0	
0010h	0051	"Q"	20h	51	"Q"
0011h	0052	"R"	21h	51	"Q"
0012h	0059	"Y"	22h	52	"R"
0013h	P_ID_{LO}	PrVendor	23h	52	"R"
0014h	P_ID_{HI}	ID #	24h	59	"Y"
0015h	P_{LO}	PrVendor	25h	59	"Y"
0016h	P_{HI}	TblAdr	26h	P_ID_{LO}	PrVendor
0017h	A_ID_{LO}	AltVendor	27h	P_ID_{LO}	ID #
0018h	A_ID_{HI}	ID #	28h	P_ID_{HI}	ID #
...	...	...	...	...	...

D.2 Query Structure Overview

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or "database." The structure sub-sections and address locations are summarized below. See *AP-646 Common Flash Interface (CFI) and Command Sets* (order number 292204) for a full description of CFI.

The following sections describe the Query structure sub-sections in detail.

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Table 36. Query Structure

Offset	Sub-Section Name	Description	Notes
00h		Manufacturer Code	1
01h		Device Code	1
(BA+2)h(2)	Block Status Register	Block-Specific Information	1,2
04-0Fh	Reserved	Reserved for Vendor-Specific Information	1
10h	CFI Query Identification String	Reserved for Vendor-Specific Information	1
1Bh	System Interface Information	Command Set ID and Vendor Data Offset	1
27h	Device Geometry Definition	Flash Device Layout	1
P(3)	Primary Intel-Specific Extended Query Table	Vendor-Defined Additional Information Specific to the Primary Vendor Algorithm	1,3

Notes:
1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BA = Block Address beginning location (i.e., 02000h is block 2's beginning location when the block size is 128 Kbyte).
3. Offset 15 defines "P" which points to the *Primary Intel-Specific Extended Query* Table.

D.3 Block Status Register

The Block Status Register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Table 37. Block Status Register

Offset	Length	Description	Address	Value
(BA+2)h(1)	1	Block Lock Status Register	BA+2:	--00 or --01
		BSR.0 Block Lock Status 0 = Unlocked 1 = Locked	BA+2:	(bit 0): 0 or 1
		BSR 1–15: *Reserved for Future Use*	BA+2:	(bit 1–15): 0

Note:
1. BA = The beginning location of a Block Address (i.e., 008000h is block 1's (64-KB block) beginning location in word mode).

D.4 CFI Query Identification String

The CFI Query Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table 38. CFI Identification (Sheet 1 of 2)

Offset	Length	Description	Add.	Hex Code	Value
10h	3	Query-unique ASCII string "QRY"	10 11: 12:	--51 --52 --59	"Q" "R" "Y"
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13: 14:	--01 --00	

Table 38. CFI Identification (Sheet 2 of 2)

Offset	Length	Description	Add.	Hex Code	Value
15h	2	Extended Query Table primary algorithm address	15: 16:	--31 --00	
17h	2	Alternate vendor command set and control interface ID code.	17:	--00	
		0000h means no second vendor-specified algorithm exists	18:	--00	
19h	2	Secondary algorithm Extended Query Table address. 0000h means none exists	19: 1A:	--00 --00	

D.5 System Interface Information

The following device information can optimize system interface software.

Table 39. System Interface Information

Offset	Length	Description	Add.	Hex Code	Value
1Bh	1	V_{CC} logic supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1B:	--27	2.7 V
1Ch	1	V_{CC} logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1C:	--36	3.6 V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1D:	--00	0.0 V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1E:	--00	0.0 V
1Fh	1	“n” such that typical single word program time-out = 2^n µs	1F:	--06	64 µs
20h	1	“n” such that typical max. buffer write time-out = 2^n µs	20:	--07	128 µs
21h	1	“n” such that typical block erase time-out = 2^n ms	21:	--0A	1 s
22h	1	“n” such that typical full chip erase time-out = 2^n ms	22:	--00	NA
23h	1	“n” such that maximum word program time-out = 2^n times typical	23:	--02	256 µs
24h	1	“n” such that maximum buffer write time-out = 2^n times typical	24:	--03	1024 µs
25h	1	“n” such that maximum block erase time-out = 2^n times typical	25:	--02	4 s
26h	1	“n” such that maximum chip erase time-out = 2^n times typical	26:	--00	NA

D.6 Device Geometry Definition

This field provides critical details of the flash device geometry.

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Table 40. Device Geometry Definition

Offset	Length	Description	Code See Table Below		
27h	1	"n" such that device size = 2^n in number of bytes	27:		
28h	2	Flash device interface: x8 async x16 async x8/x16 async 28:00,29:00 28:01,29:00 28:02,29:00	28: 29:	--02 --00	x8/ x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2^n	2A: 2B:	--05 --00	32
2Ch	1	Number of erase block regions within device: 1. x = 0 means no erase blocking; the device erases in "bulk" 2. x specifies the number of device or partition regions with one or more contiguous same-size erase blocks 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) x (individual block size)	2C:	--01	1
2Dh	4	Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	2D: 2E: 2F: 30:		

Table 41. Device Geometry: Address Codes

Address	32 Mbit	64 Mbit	128 Mbit
27:	--16	--17	--18
28:	--02	--02	--02
29:	--00	--00	--00
2A:	--05	--05	--05
2B:	--00	--00	--00
2C:	--01	--01	--01
2D:	--1F	--3F	--7F
2E:	--00	--00	--00
2F:	--00	--00	--00
30:	--02	--02	--02

D.7 Primary-Vendor Specific Extended Query Table

Certain flash features and commands are optional. The *Primary Vendor-Specific Extended Query* table specifies this and other similar information.

Table 42. Primary Vendor-Specific Extended Query (Sheet 1 of 2)

Offset(1) P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+0)h	3	Primary extended query table	31:	--50	"P"
(P+1)h		Unique ASCII string "PRI"	32:	--52	"R"
(P+2)h			33:	--49	"I"
(P+3)h	1	Major version number, ASCII	34:	--31	"1"

Table 42. Primary Vendor-Specific Extended Query (Sheet 2 of 2)

Offset[(1)] P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+4)h	1	Minor version number, ASCII	35:	--31	"1"
(P+5)h (P+6)h (P+7)h (P+8)h	4	Optional feature and command support (1=yes, 0=no) Undefined bits are "0." If bit 31 is "1" then another 31 bit field of optional features follows at the end of the bit-30 field.	36: 37: 38: 39:	--CE --00 --00 --00	
		bit 0 Chip erase supported	bit 0 = 0		No
		bit 1 Suspend erase supported	bit 1 = 1		Yes
		bit 2 Suspend program supported	bit 2 = 1		Yes
		bit 3 Legacy lock/unlock supported	bit 3 = 1[(1)]		Yes[(1)]
		bit 4 Queued erase supported	bit 4 = 0		No
		bit 5 Instant Individual block locking supported	bit 5 = 0		No
		bit 6 Protection bits supported	bit 6 = 1		Yes
		bit 7 Page-mode read supported	bit 7 = 1		Yes
		bit 8 Synchronous read supported	bit 8 = 0		No
		bit9 Simultaneous Operation Supported	bit 9 = 0		No
		bit 30 CFI Link(s) to follow (32, 64, 128- Mb)	bit 30 = 0		No
		bit 30 CFI Link(s) to follow (256 Mb)	bit 30 = 0 bit 30 = 1		No Yes
		bit 31 Another "Optional Feature" field to follow	bit 31 = 0		No
(P+9)h	1	Supported functions after suspend: read Array, Status, Query Other supported operations are: Upper Die *bits 1–7 reserved; undefined bits are "0"* Lower Die	3A:	--01	
		bit 0 Program supported after erase suspend	bit 0 = 1		Yes
(P+A)h (P+B)h	2	Block Status Register mask	3B:	--01	
		bits 2–15 are Reserved; undefined bits are "0"	3C:	--00	
		bit 0 Block Lock-Bit Status register active	bit 0 = 1		Yes
		bit 1 Block Lock-Down Bit Status active	bit 1 = 0		No
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage bits 0–3 BCD value in 100 mV bits 4–7 BCD value in volts	3D:	--33	3.3 V
(P+D)h	1	V_{PP} optimum program/erase supply voltage bits 0–3 BCD value in 100 mV bits 4–7 HEX value in volts	3E:	--00	0.0 V

Note:
1. Future devices may not support the described "Legacy Lock/Unlock" function. Thus bit 3 would have a value of "0."
2. Setting this bit, will lead to the extension of the CFI table. Please refer to Table 45.

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Table 43. Protection Register Information

Offset[1] P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+E)h	1	Number of Protection register fields in JEDEC ID space. "00h," indicates that 256 protection bytes are available	3F:	--01	01
(P+F)h (P+10)h (P+11)h (P+12)h	4	Protection Field 1: Protection Description This field describes user-available One Time Programmable (OTP) protection register bytes. Some are pre-programmed with device-unique serial numbers. Others are user-programmable. Bits 0-15 point to the protection register lock byte, the section's first byte. The following bytes are factory pre-programmed and user-programmable. bits 0-7 = Lock/bytes JEDEC-plane physical low address bits 8-15 = Lock/bytes JEDEC-plane physical high address bits 16-23 = "n" such that 2^n = factory pre-programmed bytes bits 24-31 = "n" such that 2^n = user-programmable bytes	40: 41: 42: 43:	--80 --00 --03 --03	80h 00h 8bytes 8bytes

Note:
1. The variable P is a pointer which is defined at CFI offset 15h.

Table 44. Burst Read Information

Offset[1] P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+13)h	1	Page Mode Read capability bits 0–7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	44:	--03	8 byte
(P+14)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	45:	--00	0
(P+15)h		Reserved for future use	46:		

Note:
1. The variable P is a pointer which is defined at CFI offset 15h.

The following table is the extended CFI used for the lower die of 256 Mb (2x128) device.

Table 45. Additional CFI link for the lower die of the stacked device (256 Mb only)

Offset[1] P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+15)h (P+16)h (P+17)h (P+18)h	4	Link Field Bit Information	46:	--10	
			47:	--10	
			48:	--00	
			49:	--00	
		Bits[9:0] = Address offset (within 32 Mbit segment) of reference CFI table	bit [9:0] = 10h		10
		Bits [27:10] = n^{th} 32 Mbit segment of referenced CFI table	bits[27:10] = 04h		4
		Bits [30:28] = Memory type: • 000b = CSD Flash • 100b = LD Flash	bits[30:28] = 0h		0
		bit 31 = Another CFI link field immediately follows	Bit 31 = 0h		No

Table 45. Additional CFI link for the lower die of the stacked device (256 Mb only)

Offset[1] P = 31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+19)h	1	CFI Link Quantity Subfield Definition	04A	--10	
		Bits [3:0] = Quantity field (n such that n+1 equals quantity Bit 4 = Table & die relative location • 0b = Table & die on different CE# • 1b = Table & die on same CE# Bit 5 = Link field & table relative location • 0b = Table & die on different CE# • 1b = Table & die on same CE# Bits [7:6] = RFU (Set to 00b)			

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Appendix E Additional Information

Order Number	Document/Tool
298130	Intel® StrataFlash™ Memory (J3); 28F128J3, 28F640J3, 28F320J3 Specification Update
298136	Intel® Persistent Storage Manager (IPSM) User's Guide Software Manual
297833	Intel® Flash Data Integrator (FDI) User's Guide Software Manual
290606	*5 Volt Intel® StrataFlash™ MemoryI28F320J5 and 28F640J5* datasheet
292204	AP-646 Common Flash Interface (CFI) and Command Sets
253418	Intel® Wireless Communications and Computing Package User's Guide

1. Call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit the Intel home page http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel® Embedded Flash Memory (J3 v. D), visit http://developer.intel.com/design/flash/isf.

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Appendix F Ordering Information

Figure 30. Decoder for Discrete Family (32, 64 and 128 Mbit)

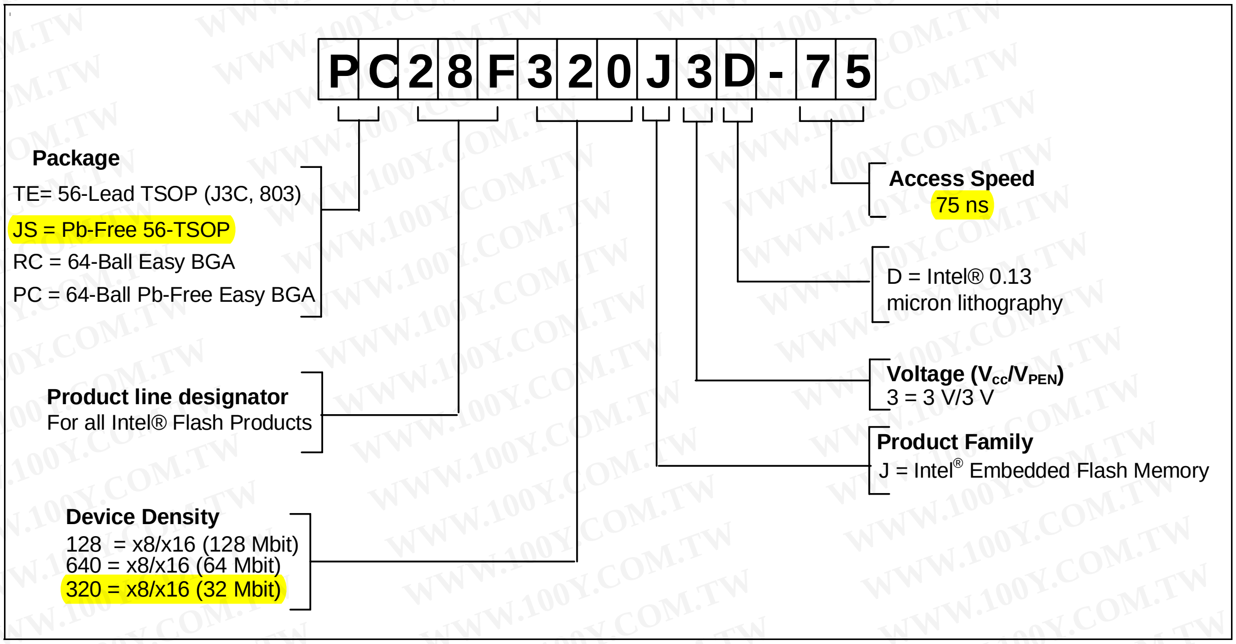

Table 46. Valid Combinations for Discrete Family

32-Mbit	64-Mbit	128-Mbit
TE28F320J3D-75	TE28F640J3D-75	TE28F128J3D-75
JS28F320J3D-75	JS28F640J3D-75	JS28F128J3D-75
RC28F320J3D-75	RC28F640J3D-75	RC28F128J3D-75
PC28F320J3D-75	PC28F640J3D-75	PC28F128J3D-75

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Figure 31. Decoder for SCSP Family (256 Mbit Only)

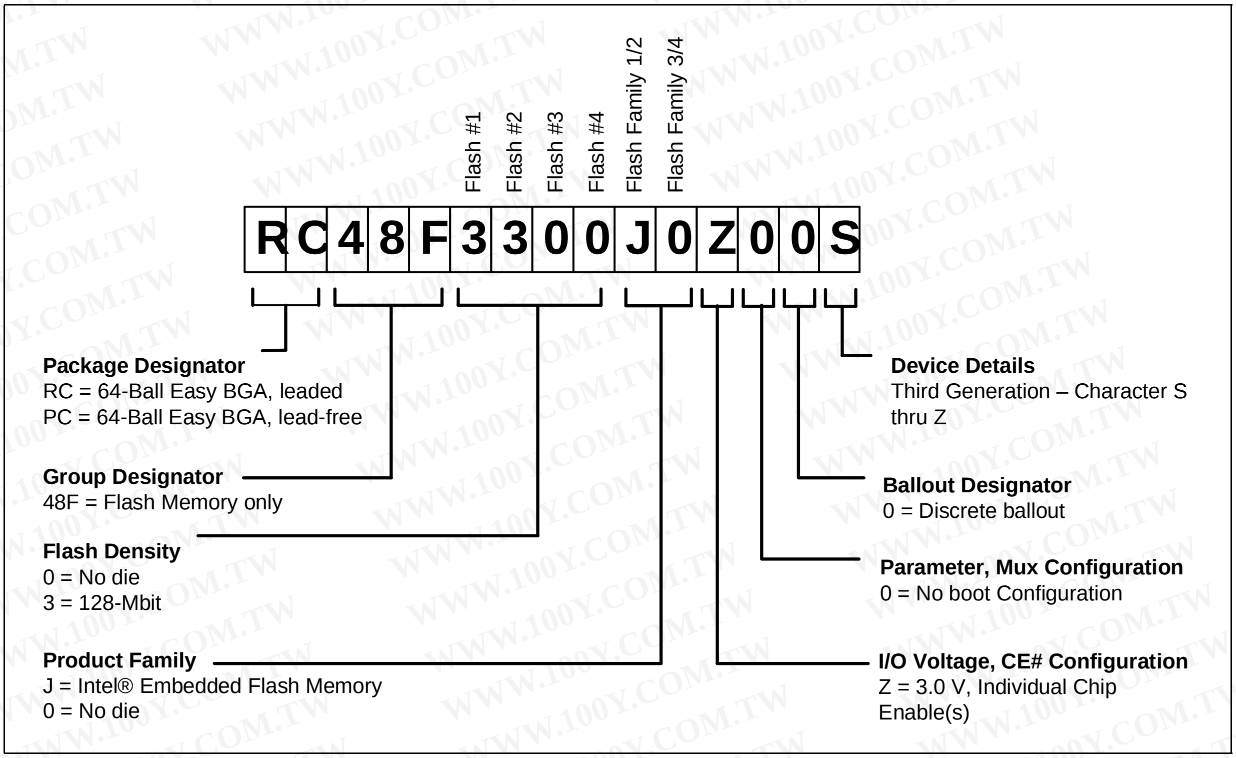

Table 47. Valid Line Item Combinations for SCSP Family

256-Mbit
RC48F3300J0Z00S
PC48F3300J0Z00S

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