Data Sheet No. PD94140

IRU3004

5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC WITH DUAL LDO CONTROLLER

FEATURES

- Meets latest VRM 8.4 specification for PentiumIII
- Provides single chip solution for Vcore, GTL+ and clock supply
- On-Board DAC programs the output voltage from 1.3V to 3.5V. The IRU3004 remains on for VID code of (11111)
- Dual linear regulator controller on-board for 1.5V GTL+ and 2.5V clock supplies
- Loss-less Short Circuit Protection
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Minimum Part Count, No External Compensation
- Soft-Start Function
- High current totem pole driver for direct driving of the external power MOSFET
- Power Good Function

APPLICATIONS

- Pentium III & next generation processor DC to DC converter application
- Low Cost Pentium with AGP

DESCRIPTION

The IRU3004 controller IC is specifically designed to meet Intel specifications for Pentium III™ microprocessor applications as well as the next generation P6 family processors. The IC provides a single chip controller IC for the Vcore, GTL+ and clock supplies required for the Pentium III applications. The IRU3004 features a patented topology, that in combination with a few external components as shown in the typical application circuit, will provide in excess of 20A of output current for an on-board DC-DC converter while automatically providing the right output voltage via the 5-bit internal DAC meeting the latest VRM specification. The IRU3004 also features loss-less current sensing by using the $R_{DS(on)}$ of the high side power MOSFET as the sensing resistor and a Power Good window comparator that switches its open collector output low when the output is outside of a ±10% window. Other features of the device are: under-voltage lockout for both 5V and 12V supplies, an external programmable soft-start function as well as programming the oscillator frequency by using an external capacitor.

TYPICAL APPLICATION

Note: Pentium III is trademark of Intel Corp.

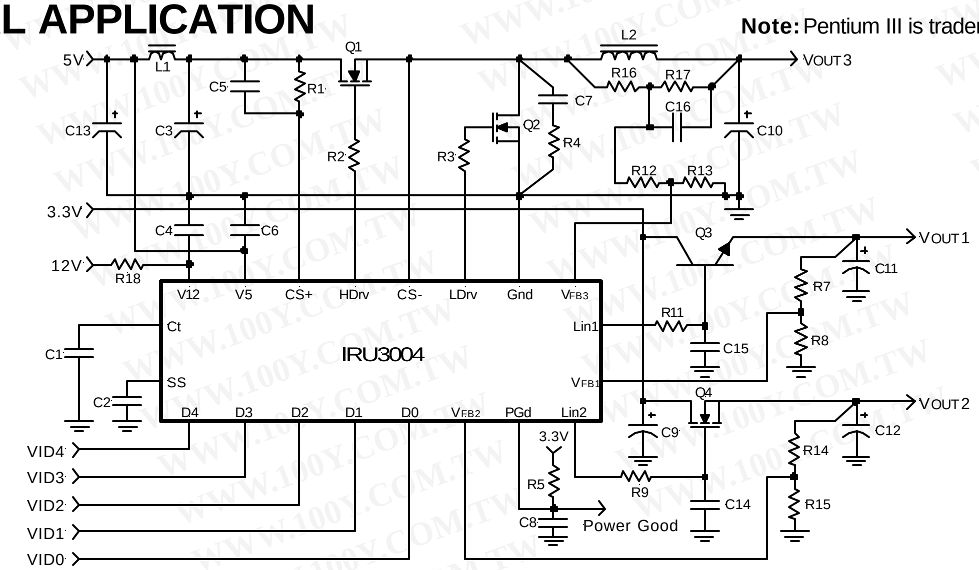


Figure 1 - Typical application of the IRU3004.

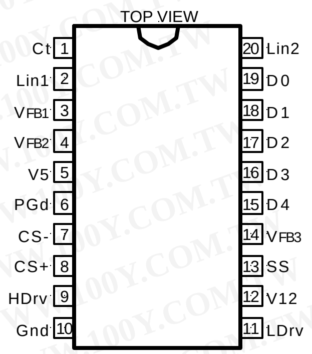
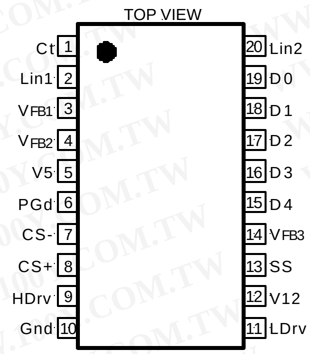
PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3004CW	20-Pin Plastic SOIC (W)
0 To 70	IRU3004CF	20-Pin Plastic TSSOP (F)

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 10V
V12 Supply Voltage 20V
Storage Temperature Range .... -65°C To 150°C
Operating Junction Temperature Range .... 0°C To 125°C

PACKAGE INFORMATION

20-PIN WIDE BODY PLASTIC SOIC (W)	20-PIN PLASTIC TSSOP (F)
	
θ_{JA}=85°C/W	θ_{JA}=90°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
VID Section						
DAC Output Voltage (Note 1)			0.98Vs	Vs	1.02Vs	V
DAC Output Line Regulation					0.1	%
DAC Output Temp Variation					0.5	%
VID Input LO					0.4	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5				27		KΩ
Power Good Section						
Under-Voltage lower trip point		V_{OUT} Ramping Down	0.89Vs	0.90Vs	0.91Vs	V
Under-Voltage upper trip point		V_{OUT} Ramping Up		0.92Vs		V
UV Hysteresis			0.015Vs	0.02Vs	0.025Vs	V
Over-Voltage upper trip point		V_{OUT} Ramping Up	1.09Vs	1.10Vs	1.11Vs	V
Over-Voltage lower trip point		V_{OUT} Ramping Down		1.08Vs		V
OV Hysteresis			0.015Vs	0.02Vs	0.025Vs	V
Power Good Output LO		R_L=3mA			0.4	V
Power Good Output HI		R_L=5K Pull-Up to 5V	4.8			V
Soft-Start Section						
Soft-Start Current		CS+=0V, CS-=5V		10		µA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
UVLO Section						
UVLO Threshold-12V		Supply Ramping Up	9.2	10	10.8	V
UVLO Hysteresis-12V			0.3	0.4	0.5	V
UVLO Threshold-5V		Supply Ramping Up	4.1	4.3	4.5	V
UVLO Hysteresis-5V			0.2	0.3	0.4	V
Error Comparator Section						
Input Bias Current					2	μA
Input Offset Voltage			-2		+2	mV
Delay to Output		V_{DIFF}=10mV			100	ns
Current Limit Section						
CS Threshold Set Current			160	200	240	μA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1μF			2	%
Supply Current						
Operating Supply Current		C_L=3000pF:				
		V5		20		mA
		V12		14		
Output Drivers Section						
Rise Time		C_L=3000pF		70	100	ns
Fall Time		C_L=3000pF		70	130	ns
Dead Band Time		C_L=3000pF	100	200	300	ns
Oscillator Section						
Osc Frequency		Ct=150pF	160	220	260	KHz
Osc Valley					0.2	V
Osc Peak				V5		V
LDO Controller Section						
V_{FB1} & V_{FB2}			1.455	1.500	1.545	V
Input Bias Current					2	μA
Lin1 or Lin2 Drive Current				50		mA

Note 1: Vs refers to the set point voltage given in Table 1.

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Ct	This pin programs the oscillator frequency in the range of 50KHz to 500KHz with an external capacitor connected from this pin to the ground.
2	Lin1	This pin controls the gate of an external transistor for either the GTL+ linear regulator or Clock supply.
3	V_{FB1}	This pin provides the feedback for the linear regulator that its output drive is Lin1 pin.
4	V_{FB2}	This pin provides the feedback for the linear regulator that its output drive is Lin2 pin.
5	V5	5V supply voltage.
6	PGd	This pin is an open collector output that switches LO when the output of the converter is not within ±10% (typical) of the nominal output voltage. When Power Good pin switches LO the sat voltage is less than 0.4V at 3mA.
7	CS-	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
8	CS+	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
9	HDrv	Output driver for the high-side power MOSFET.
10	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from V5 and V12 pins to this pin for noise free operation.
11	LDrv	Output driver for the synchronous power MOSFET.
12	V12	This pin is connected to the 12 V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (0.1 to 1μF) must be connected directly from this pin to ground pin in order to supply the peak current to the power MOSFET duringthe transitions.
13	SS	This pin provides the soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to the ground which ramps up the outputs of the switching regulator, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
14	V_{FB3}	This pin is connected directly to the output of the Core supply to provide feedback to the Error comparator.
15	D4	This pin selects a range of output voltages for the DAC. When in the LOW state the range is 1.3V to 2.05V. For VID codes of all "1" the IRU3004 keeps all the outputs on.
16	D3	MSB input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply.
17	D2	Input to the DAC that programs the output voltage. This pin can be pulled up externally by a 10K resistor to either 3.3V or 5V supply.
18	D1	Input to the DAC that programs the output voltage. This pin can be pulled up externally by a 10KΩ resistor to either 3.3V or 5V supply.
19	D0	LSB input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply.
20	Lin2	This pin controls the gate of an external transistor for either the GTL+ linear regulator or Clock supply.

BLOCK DIAGRAM

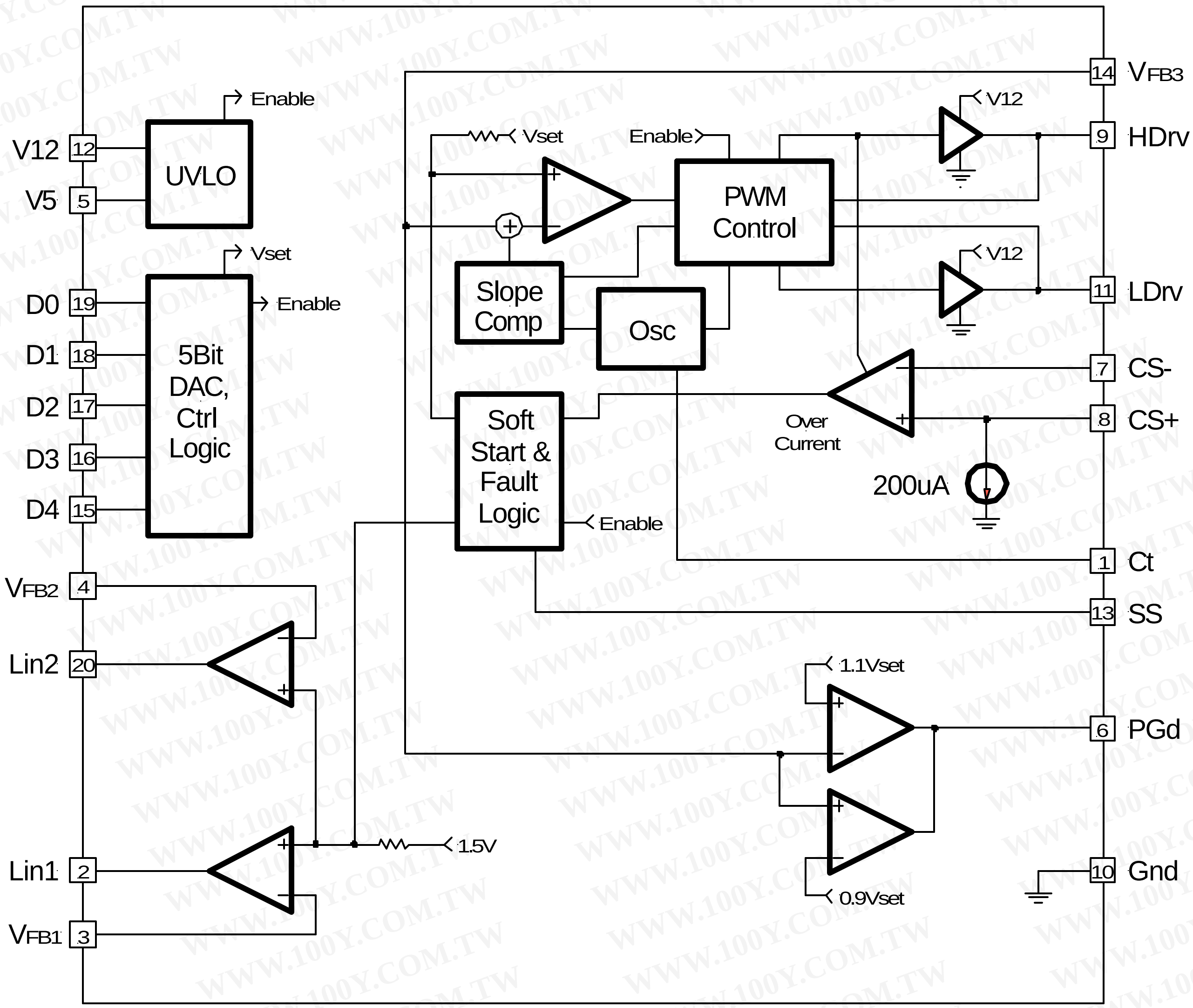


Figure 2 - Simplified block diagram of the IRU3004.

TYPICAL APPLICATION

Pentium III

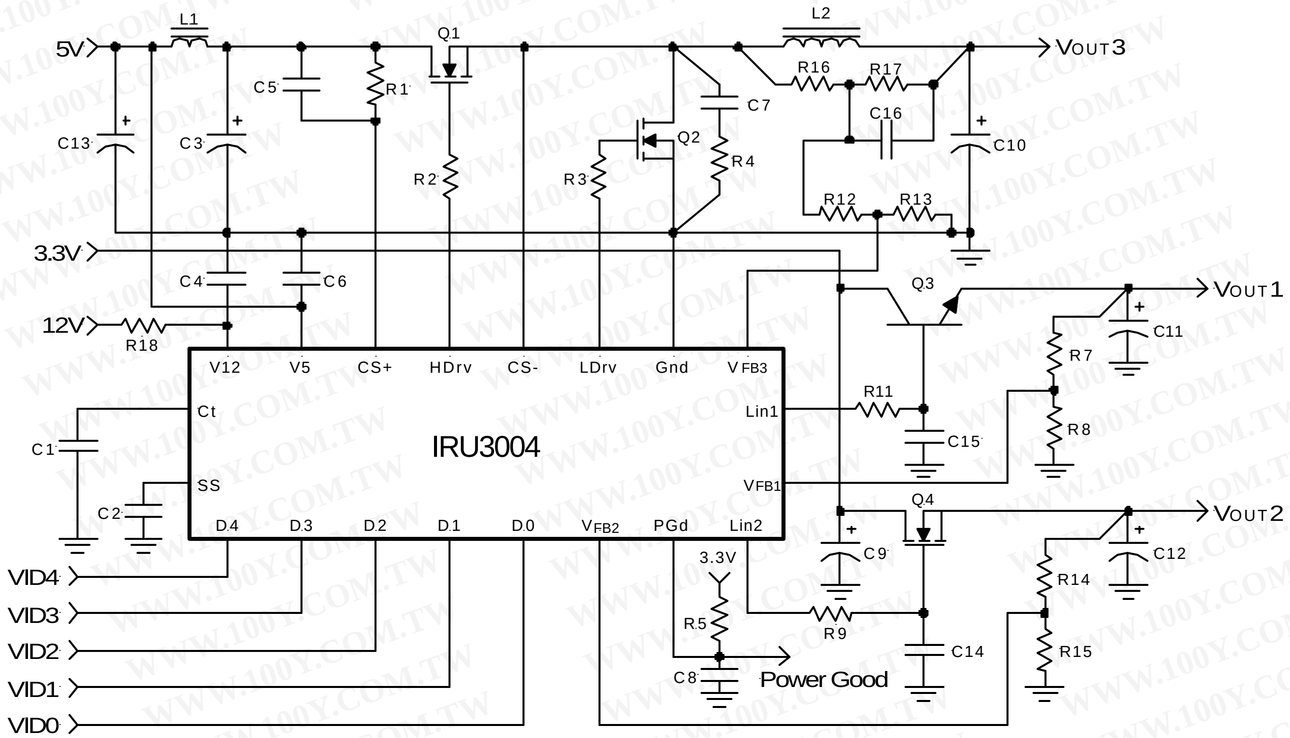


Figure 3 - Typical application of IRU3004 in an on-board DC-DC converter providing the Core, GTL+, and Clock supplies for the Pentium II microprocessor.

IRU3004 APPLICATION PARTS LIST

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103S, TO-263 package	IR
Q2	MOSFET	1	IRL3103D1S, TO-263 package	IR
Q3	Bipolar Trans, GP	1	MPS2222A, SOT-23 package	Motorola
Q4	MOSFET	1	IRLR024, TO-252 package	IR
L1	Inductor	1	L=1µH, 5052 core with 4 turns of 1.0mm wire	MicroMetal
L2	Inductor	1	L=2.7µH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Ceramic	1	150pF, 0603	
C2, 6	Capacitor, Ceramic	2	1µF, 0603	
C3	Capacitor, Electrolytic	2	10MV1200GX, 1200µF,10V	Sanyo
C4	Capacitor, Ceramic	1	1µF, 0805	
C5	Capacitor, Ceramic	1	220pF, 0603	
C7, 14, 15	Capacitor, Ceramic	3	1000pF, 0603	
C8	Capacitor, Ceramic	1	0.1µF, 0603	
C9	Capacitor, Electrolytic	1	6MV1000GX, 1000µF, 6.3V	Sanyo
C10	Capacitor, Electrolytic	6	6MV1500GX, 1500µF, 6.3V	Sanyo
C11	Capacitor, Electrolytic	1	6MV150GX, 150µF, 6.3V	Sanyo
C12	Capacitor, Electrolytic	1	6MV1000GX, 1000µF, 6.3V	Sanyo
C13	Capacitor, Electrolytic	1	10MV470GX, 470µF, 10V	Sanyo
C16	Capacitor, Ceramic	1	4.7µF, 1206	
R1	Resistor	1	3.3KΩ, 5%, 0603	
R2, 3, 4	Resistor	3	4.7Ω, 5%, 1206	
R5, 15	Resistor	2	10KΩ, 5%, 0603	
R7, 12	Resistor	2	100Ω, 1%, 0603	
R8	Resistor	1	150Ω, 1%, 0603	
R9, 11, 14	Resistor	3	100Ω, 5%, 0603	
R13	Resistor	1	22KΩ, 1%, 0603	
R16	Resistor	1	220Ω, 1%, 0603	
R17	Resistor	1	330Ω, 1%, 0603	
R18	Resistor	1	10Ω, 5%, 0603	

Note 1: R16, R17, C16, R12, and R13 set the Vcore 2% higher for level shift to reduce CPU transient voltage.

Note 2: R14 and R15 set the 1.5V approximately 1% higher to account for the trace resistance drop.

TYPICAL APPLICATION

Pentium with AGP

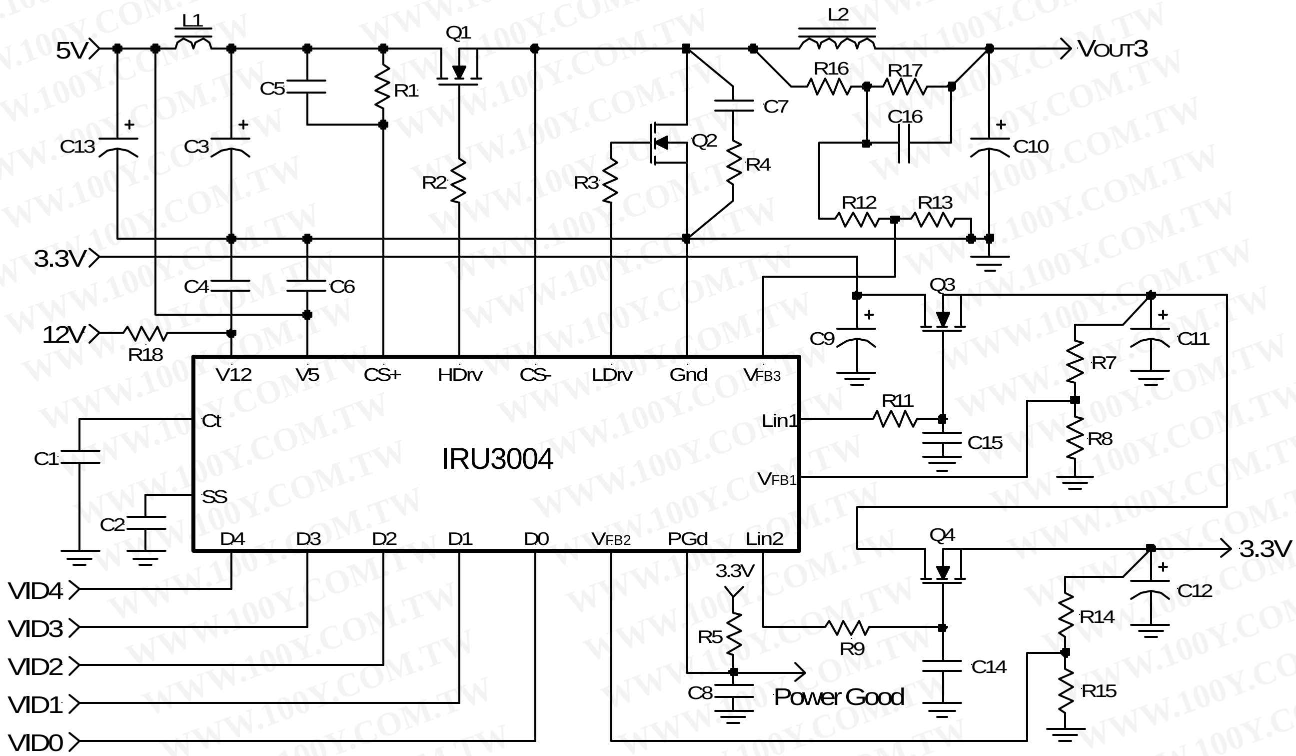


Figure 4 - Typical application of IRU3004 in a Pentium with AGP where the power dissipation of the 3.3V linear regulator is equally distributed between Q3 and Q4 pass transistors. This equal distribution is possible by accurately regulating the first regulator using the IRU3004 linear controller and its internal 1% reference voltage while the second controller regulates the output of the first regulator from 4.17V to 3.3V, thereby distributing the power dissipation equally.

IRU3004 APPLICATION PARTS LIST

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103s, TO-263 package	IR
Q2	MOSFET	1	IRL3103D1S, TO-263 package	IR
Q3, 4	MOSFET	2	IRL3303S, TO-263 package	IR
L1	Inductor	1	L=1µH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L2	Inductor	1	L=2.7µH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Ceramic	1	150pF, 0603	
C2, 6	Capacitor, Ceramic	2	1µF, 0603	
C3	Capacitor, Electrolytic	2	10MV1200GX, 1200µF, 10V	Sanyo
C4	Capacitor, Ceramic	1	1µF, 0805	
C5	Capacitor, Ceramic	1	220pF, 0603	
C7, 14, 15	Capacitor, Ceramic	3	1000pF, 0603	
C8	Capacitor, Ceramic	1	0.1µF, 0603	
C9	Capacitor, Electrolytic	1	6MV1000GX, 1000µF, 6.3V	Sanyo
C10	Capacitor, Electrolytic	6	6MV1500GX, 1500µF, 6.3V	Sanyo
C11	Capacitor, Electrolytic	1	6MV150GX, 150µF, 6.3V	Sanyo
C12	Capacitor, Electrolytic	1	6MV1000GX, 1000µF, 6.3V	Sanyo
C13	Capacitor, Electrolytic	1	10MV470GX, 470µF, 10V	Sanyo
C16	Capacitor, Ceramic	1	4.7µF, 1206	
R1	Resistor	1	3.3KΩ, 5%, 0603	
R2, 3, 4	Resistor	3	4.7Ω, 5%, 1206	
R5, 15	Resistor	2	10KΩ, 5%, 0603	
R7	Resistor	1	267Ω, 1%, 0603	
R8	Resistor	2	150Ω, 1%, 0603	
R9, 11, 14	Resistor	3	100Ω, 5%, 0603	
R12	Resistor	1	100Ω, 1%, 0603	
R13	Resistor	1	22KΩ, 1%, 0603	
R16	Resistor	1	220Ω, 1%, 0603	
R17	Resistor	1	330Ω, 1%, 0603	
R18	Resistor	1	10Ω, 5%, 0603	

Note 1: R16, R17, C16, R12, and R13 set the Vcore 2% higher for level shift to reduce CPU transient voltage.

APPLICATION INFORMATION

An example of how to calculate the components for the application circuit is given below.

Assuming, two sets of output conditions that this regulator must meet:

a) Vo=2.8V, Io=14.2A, ΔVo=185mV, ΔIo=14.2A

b) Vo=2V, Io=14.2A, ΔVo=140mV, ΔIo=14.2A

The regulator design will be done such that it meets the worst case requirement of each condition.

Output Capacitor Selection

The first step is to select the output capacitor. This is done primarily by selecting the maximum ESR value that meets the transient voltage budget of the total ΔVo specification. Assuming that the regulators DC initial accuracy plus the output ripple is 2% of the output voltage, then the maximum ESR of the output capacitor is calculated as:

$$ESR \le \frac{100}{14.2} = 7m\Omega$$

The Sanyo MVGX series is a good choice to achieve both the price and performance goals. The 6MV1500GX, 1500µF, 6.3V has an ESR of less than 36mΩ typical. Selecting 6 of these capacitors in parallel has an ESR of ≈ 6mΩ which achieves our low ESR goal.

Other type of Electrolytic capacitors from other manufacturers to consider are the Panasonic FA series or the Nichicon PL series.

Reducing the Output Capacitors Using Voltage Level Shifting Technique

The trace resistance or an external resistor from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transition from light load to full load and vice versa. To accomplish this, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the device is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. This intentional voltage level shifting during the load transient eases the requirement for the output capacitor ESR at the cost of load regulation. One can show that the new ESR requirement eases up by half the total trace resistance. For example, if the ESR requirement of the output capacitors without voltage level shifting must be 7mΩ, then after level shifting the new ESR will only need to be 9.5mΩ if the trace resistance is 5mΩ (7 + 5/2=9.5). However, one must be careful that the combined "voltage level shifting" and the transient response is still within the maximum tolerance of the Intel specification. To insure this, the maximum trace resistance must be less than:

$$Rs \le 2 \times \frac{(Vspec - 0.02 \times Vo - \Delta Vo)}{\Delta I}$$

Where:
Rs = Total maximum trace resistance allowed
Vspec = Intel total voltage specification
Vo = Output voltage
ΔVo = Output ripple voltage
ΔI = load current step

For example, assuming:
Vspec = ±140mV = ±0.1V for 2V output
Vo = 2V
ΔVo = assume 10mV = 0.01V
ΔI = 14.2A

Then the Rs is calculated to be:

$$Rs \le 2 \times \frac{(0.140 - 0.02 \times 2 - 0.01)}{14.2} = 12.6m\Omega$$

However, if a resistor of this value is used, the maximum power dissipated in the trace (or if an external resistor is being used) must also be considered. For example if Rs=12.6mΩ, the power dissipated is:

$$Io^2 \times Rs = 14.2^2 \times 12.6 = 2.54W$$

This is a lot of power to be dissipated in a system. So, if the Rs=5mΩ, then the power dissipated is about 1W which is much more acceptable. If level shifting is not implemented, then the maximum output capacitor ESR was shown previously to be 7mΩ which translated to ≈ 6 of the 1500µF, 6MV1500GX type Sanyo capacitors. With Rs=5mΩ, the maximum ESR becomes 9.5mΩ which is equivalent to ≈ 4 caps. Another important consideration is that if a trace is being used to implement the resistor, the power dissipated by the trace increases the case temperature of the output capacitors which could seriously effect the life time of the output capacitors.

Output Inductor Selection

The output inductance must be selected such that under low line and the maximum output voltage condition, the inductor current slope times the output capacitor ESR is ramping up faster than the capacitor voltage is drooping during a load current step. However, if the inductor is too small, the output ripple current and ripple voltage become too large. One solution to bring the ripple current down is to increase the switching frequency, however that will be at the cost of reduced efficiency and higher system cost. The following set of formulas are derived to achieve the optimum performance without many design iterations.

The maximum output inductance is calculated using the following equation:

$$L = ESR \times C \times \left(\frac{V_{IN(MIN)} - V_{O(MAX)}}{2 \times \Delta I}\right)$$

Where:

$V_{IN(MIN)}$ = Minimum input voltage

$Vo = 2.8V$, $\Delta I = 14.2A$

$$L = 0.006 \times 9000 \times \left(\frac{4.75 - 2.8}{2 \times 14.2}\right) = 3.7\mu H$$

Assuming that the programmed switching frequency is set at 200KHz, an inductor is designed using the Micrometals' powder iron core material. The summary of the design is outlined below:

The selected core material is Powder Iron, the selected core is T50-52D from Micro Metal wound with 8 turns of #16 AWG wire, resulting in 3μH inductance with ≈ 3mΩ of DC resistance.

Assuming L=3μH and Fsw=200KHz (switching frequency), the inductor ripple current and the output ripple voltage is calculated using the following set of equations:

$T \equiv$ Switching Period

$D \equiv$ Duty Cycle

$Vsw \equiv$ High side Mosfet ON Voltage

$R_{DS} \equiv$ Mosfet On Resistance

$Vsync \equiv$ Synchronous MOSFET ON Voltage

$\Delta Ir \equiv$ Inductor Ripple Current

$\Delta Vo \equiv$ Output Ripple Voltage

$$T = \frac{1}{Fsw}$$

$$Vsw = Vsync = Io \times R_{DS}$$

$$D \approx \frac{Vo + Vsync}{V_{IN} - Vsw + Vsync}$$

$$T_{ON} = D \times T$$

$$T_{OFF} = T - T_{ON}$$

$$\Delta Ir = (Vo + Vsync) \times \frac{T_{OFF}}{L}$$

$$\Delta Vo = \Delta Ir \times ESR$$

In our example for Vo=2.8V and 14.2A load, assuming IRL3103 MOSFET for both switches with maximum on-resistance of 19mΩ, we have:

$$T = \frac{1}{200000} = 5\mu s$$

$$Vsw = Vsync = 14.2 \times 0.019 = 0.27V$$

$$D \approx \frac{2.8 + 0.27}{5 - 0.27 + 0.27} = 0.61$$

$$T_{ON} = 0.61 \times 5 = 3.1\mu s$$

$$T_{OFF} = 5 - 3.1 = 1.9\mu s$$

$$\Delta Ir = (2.8 + 0.27) \times \frac{1.9}{3} = 1.94A$$

$$\Delta Vo = 1.94 \times 0.006 = 0.011V = 11mV$$

Power Component Selection

Assuming IRL3103 MOSFETs as power components, we will calculate the maximum power dissipation as follows:

For high-side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle.

$$D_{MAX} \approx \frac{(2.8 + 0.27)}{(4.75 - 0.27 + 0.27)} = 0.65$$

$$P_{DH} = D_{MAX} \times Io^2 \times R_{DS(MAX)}$$

$$P_{DH} = 0.65 \times 14.2^2 \times 0.029 = 3.8W$$

$R_{DS(MAX)}$ = Maximum $R_{DS(ON)}$ of the MOSFET (125°C)

For synchronous MOSFET, maximum power dissipation happens at minimum Vo and minimum duty cycle.

$$D_{MIN} \approx \frac{(2 + 0.27)}{(5.25 - 0.27 + 0.27)} = 0.43$$

$$P_{DS} = (1 - D_{MIN}) \times Io^2 \times R_{DS(MAX)}$$

$$P_{DS} = (1 - 0.43) \times 14.2^2 \times 0.029 = 3.33W$$

Heat Sink Selection

Selection of the heat sink is based on the maximum allowable junction temperature of the MOSFETS. Since we previously selected the maximum $R_{DS(on)}$ at 125°C, then we must keep the junction below this temperature. Selecting TO-220 package gives θ_{JC}=1.8°C/W (from the venders' data sheet) and assuming that the selected heat sink is black anodized, the heat-sink-to-case thermal resistance is θ_{CS}=0.05°C/W, the maximum heat sink temperature is then calculated as:

$$T_S = T_J - P_D \times (\theta_{JC} + \theta_{CS})$$

$$T_S = 125 - 3.82 \times (1.8 + 0.05) = 118°C$$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated as follows:

Assuming $T_A = 35°C$:

$\Delta T = Ts - T_A = 118 - 35 = 83°C$
Temperature Rise Above Ambient

$$\theta_{SA} = \frac{\Delta T}{P_D} = \frac{83}{3.82} = 22°C/W$$

Next, a heat sink with lower θ_{SA} than the one calculated in the previous step must be selected. One way is to simply look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" given in the heat sink manufacturers' catalog and select a heat sink that results in lower temperature rise than the one calculated in previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

Company	Part #
Thermalloy	6078B
AAVID	577002

Following the same procedure for the Schottky diode results in a heat sink with θ_{SA}=25°C/W. Although it is possible to select a slightly smaller heat sink, for simplicity, the same heat sink as the one for the high side MOSFET is also selected for the synchronous MOSFET.

Switcher Current Limit Protection

The PWM controller uses the MOSFET $R_{DS(ON)}$ as the sensing resistor to sense the MOSFET current and compares to a programmed voltage which is set externally via a resistor (Rcs) placed between the drain of the MOSFET and the "CS+" terminal of the IC as shown in the application circuit. For example, if the desired current limit point is set to be 22A and from our previous selection, the maximum MOSFET $R_{DS(ON)}$=19mΩ, then the current sense resistor, Rcs is calculated as:

Where:
I_B = 200μA is the internal current setting of the device

$$Vcs = I_{CL} \times R_{DS} = 22 \times 0.019 = 0.418V$$

$$Rcs = \frac{Vcs}{I_B} = \frac{0.418V}{200\mu A} = 2.1K\Omega$$

Switcher Timing Capacitor Selection

The switching frequency can be programmed using an external timing capacitor. The value of Ct can be approximated using the equation below:

$$Fsw \ y \ \frac{3.5 \times 10^{-5}}{Ct}$$

Where:
Ct = Timing Capacitor
Fsw = Switching Frequency

If Fsw = 200KHz:

$$Ct \ y \ \frac{3.5 \times 10^{-5}}{200 \times 10^{3}} = 175pF$$

LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the linear regulators is to select its maximum $R_{DS(ON)}$ based on the input to output Dropout voltage and the maximum load current.

For $V_O = 1.5V$, $V_{IN} = 3.3V$ and $I_L = 2A$:

$$R_{DS(max)} = \frac{(V_{IN} - V_O)}{I_L} = \frac{(3.3 - 1.5)}{2} = 0.9\Omega$$

Note that since the MOSFETs $R_{DS(ON)}$ increases with temperature, this number must be divided by ≈ 1.5, in order to find the $R_{DS(on)}$ max at room temperature. The Motorola MTP3055VL has a maximum of 0.18Ω $R_{DS(ON)}$ at room temperature, which meets our requirement.

To select the heat sink for the LDO MOSFET the first step is to calculate the maximum power dissipation of the device and then follow the same procedure as for the switcher.

$$P_D = (V_{IN} - V_O) \times I_L$$

Where:
P_D = Power Dissipation of the Linear Regulator
I_L = Linear Regulator Load Current

For the 1.5V and 2A load:

$$P_D = (3.3 - 1.5) \times 2 = 3.6W$$

Assuming $T_{J(max)}$ = 125°C then:

$$Ts = T_J - P_D \times (\theta_{JC} + \theta_{CS})$$
$$Ts = 125 - 3.6 \times (1.8 + 0.05) = 118°C$$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated as follows:

Assuming $T_A = 35°C$:

$\Delta T = T_S - T_A = 118 - 35 = 83°C$
Temperature Rise Above Ambient

$$\theta_{SA} = \frac{\Delta T}{P_D} = \frac{83}{3.6} = 23°C/W$$

The same heat sink as the one selected for the switcher MOSFETs is also suitable for the 1.5V regulator. It is also possible to use TO-263 package or even the MTD3055VL in D-Pak if the load current is less than 1.5A. For the 2.5V regulator, since the dropout voltage is only 0.8V and the load current is less than 0.5A, for most applications, the same MOSFET without heat sink or for low cost applications, one can use PN2222A in TO-92 or SOT-23 package.

LDO Regulator Component Selection

Since the internal voltage reference for the linear regulators is set at 1.5V for all devices, there is no need to divide the output voltage for the 1.5V, GTL+ regulator.

For the 2.5V Clock supply, the resistor dividers are selected per following:

$$V_O = \left(1 + \frac{R_t}{R_B}\right) \times V_{REF}$$

Where:
Rt = Top resistor divider
R_B = Bottom resistor divider
Vref = 1.5V typical

Assuming Rt = 100Ω, for Vo = 2.5V:

$$R_B = \frac{R_t}{\left(\frac{V_O}{V_{REF}}\right) - 1} = \frac{100}{\left(\frac{2.5}{1.5}\right) - 1} = 150\Omega$$

For 1.5V output, Rt can be shorted and R_B left open. However, it is recommended to leave the resistor dividers as shown in the typical application circuit so that the output voltage can be adjusted higher to account for the trace resistance in the final board layout.

It is also recommended that an external filter be added on the linear regulators to reduce the amount of the high frequency ripple at the output of the regulators. This can simply be done by the resistor capacitor combination as shown in the application circuit.

Disabling the LDO Regulators

The LDO controllers can easily be disabled by connecting the feedback pins (V_{FB1} and V_{FB2}) to a voltage higher than 1.5V such as 5V for all devices.

Switcher Output Voltage Adjust

As was discussed earlier, the trace resistance from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To account for the DC drop, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the part is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. To do this, the top resistor of the resistor divider (R12 in the application circuit) is set at 100Ω, and the R13 is calculated.

For example, if DAC voltage setting is for 2.8V and the desired output under light load is 2.835V, then R13 is calculated using the following formula:

$$R13 = 100 \times \left(\frac{V_{DAC}}{(V_O - 1.004 \times V_{DAC})}\right) \quad (\Omega)$$

$$R13 = 100 \times \left(\frac{2.8}{(2.835 - 1.004 \times 2.800)}\right) = 11.76K\Omega$$

Select 11.8KΩ, 1%

Note: The value of the top resistor must not exceed 100Ω. The bottom resistor can then be adjusted to raise the output voltage.

Soft-Start Capacitor Selection

The soft-start capacitor must be selected such that during the start up, when the output capacitors are charging up, the peak inductor current does not reach the current limit threshold. A minimum of 1µF capacitor insures this for most applications. An internal 10µA current source charges the soft-start capacitor which slowly ramps up the inverting input of the PWM comparator V_{FB3}. This insures the output voltage to ramp at the same rate as the soft-start cap thereby limiting the input current. For example, with 1µF and the 10µA internal current source the ramp up rate is $(\Delta V/\Delta t)=(I/C)=1V/100ms$. Assuming that the output capacitance is 9000µF, the maximum start up current will be:

$$I = 9000\mu F \times (1V / 100ms) = 0.09A$$

Input Filter

It is recommended to place an inductor between the system 5V supply and the input capacitors of the switching regulator to isolate the 5V supply from the switching noise that occurs during the turn on and off of the switching components. Typically an inductor in the range of 1 to 3μH will be sufficient in this type of application.

Switcher External Shutdown

The best way to shutdown the switcher is to pull down on the soft-start pin using an external small signal transistor such as 2N3904 or 2N7002 small signal MOSFET. This allows slow ramp up of the output, the same as the power up.

Layout Considerations

Switching regulators require careful attention to the layout of the components, specifically power components since they switch large currents. These switching components can create large amount of voltage spikes and high frequency harmonics if some of the critical components are far away from each other and are connected with inductive traces. The following is a guideline of how to place the critical components and the connections between them in order to minimize the above issues.

<u>Start the layout by first placing the power components:</u>

1) Place the input capacitors C3 and the high side MOSFET, Q1 as close to each other as possible.

2) Place the synchronous MOSFET, Q2 and the Q1 as close to each other as possible with the intention that the source of Q1 and drain of the Q2 has the shortest length.

3) Place the snubber R4 & C7 between Q1 & Q2.

4) Place the output inductor, L2 and the output capacitors, C10 between the MOSFET and the load with output capacitors distributed along the slot 1 and close to it.

5) Place the bypass capacitors, C4 and C6 right next to 12V and 5V pins. C4 next to the 12V, pin 12 and C6 next to the 5V, pin 5.

6) Place the controller IC such that the PWM output drives, pins 9 and 11 are relatively short distance from gates of Q1 and Q2.

7) Place resistor dividers, R7 & R8 close to pin 3, R12 & R13 (see note) close to pin 14 and R14 and R15 (see note) close to pin 20.

Note: Although, the PWM controller does not require R12-15 resistors, and the feedback pins 3 and 14 can be directly connected to their respective outputs, they can be used to set the outputs slightly higher to account for any output drop at the load due to the trace resistance.

8) Place R11, C15, Q3 and C11 close to each other and do the same with R9, C14, Q4 and C12.

Note: It is better to place the linear regulator components close to the IC and then run a trace from the output of each regulator to its respective load such as 2.5V to the clock and 1.5V for GTL + termination. However, if this is not possible then the trace from the linear drive output pins, pins 2 and 20 must be routed away from any high frequency data signals. It is critical, to place high frequency ceramic capacitors close to the clock chip and termination resistors to provide local bypassing.

9) Place timing capacitor C1 close to pin 1 and soft start capacitor C2 close to pin 13.

<u>Component connections:</u>

Note: It is extremely important that no data bus should be passing through the switching regulator section specifically close to the fast transition nodes such as PWM drives or the inductor voltage.

Using the 4 layer board, dedicate on layer to ground, another layer as the power layer for the 5V, 3.3V, Vcore, 1.5V and if it is possible for the 2.5V. Connect all grounds to the ground plane using direct vias to the ground plane. Use large low inductance/low impedance plane to connect the following connections either using component side or the solder side:

a) C3 to Q1 Drain
b) Q1 Source to Q2 Drain
c) Q2 drain to L2
d) L2 to the output capacitors, C10
e) C10 to the slot 1
f) Input filter L1 to the C3
g) C9 to Q4 drain
h) C12 to the Q4 source

Connect the rest of the components using the shortest connection possible.

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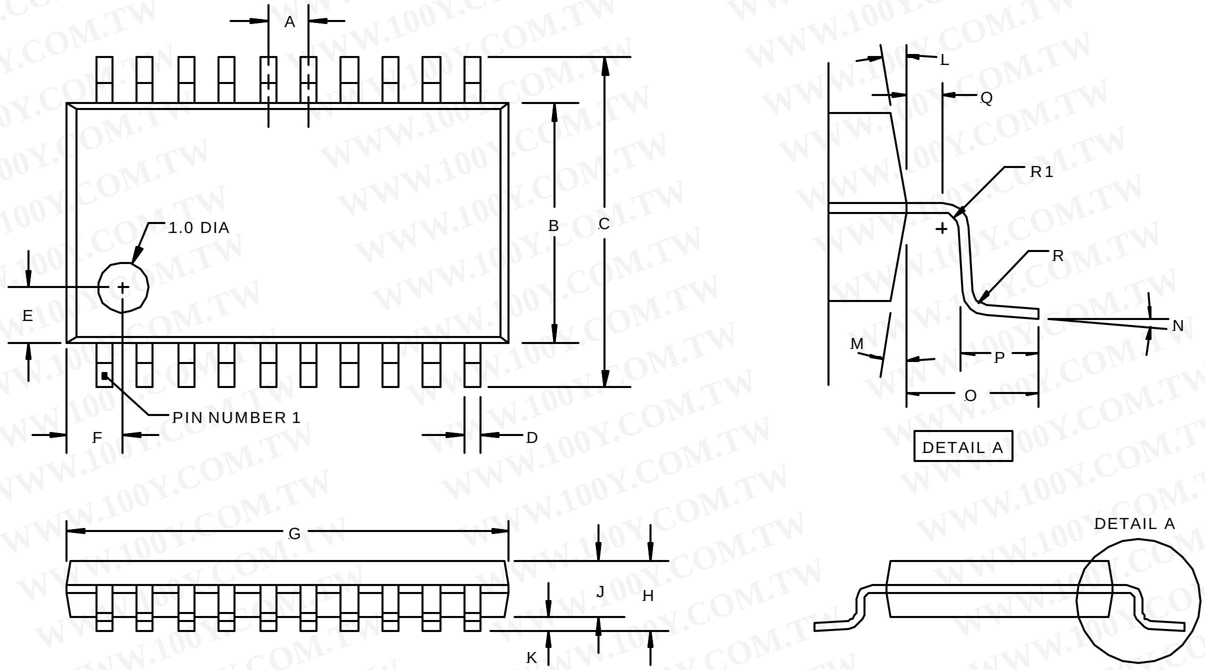
(F) TSSOP Package
20-Pin

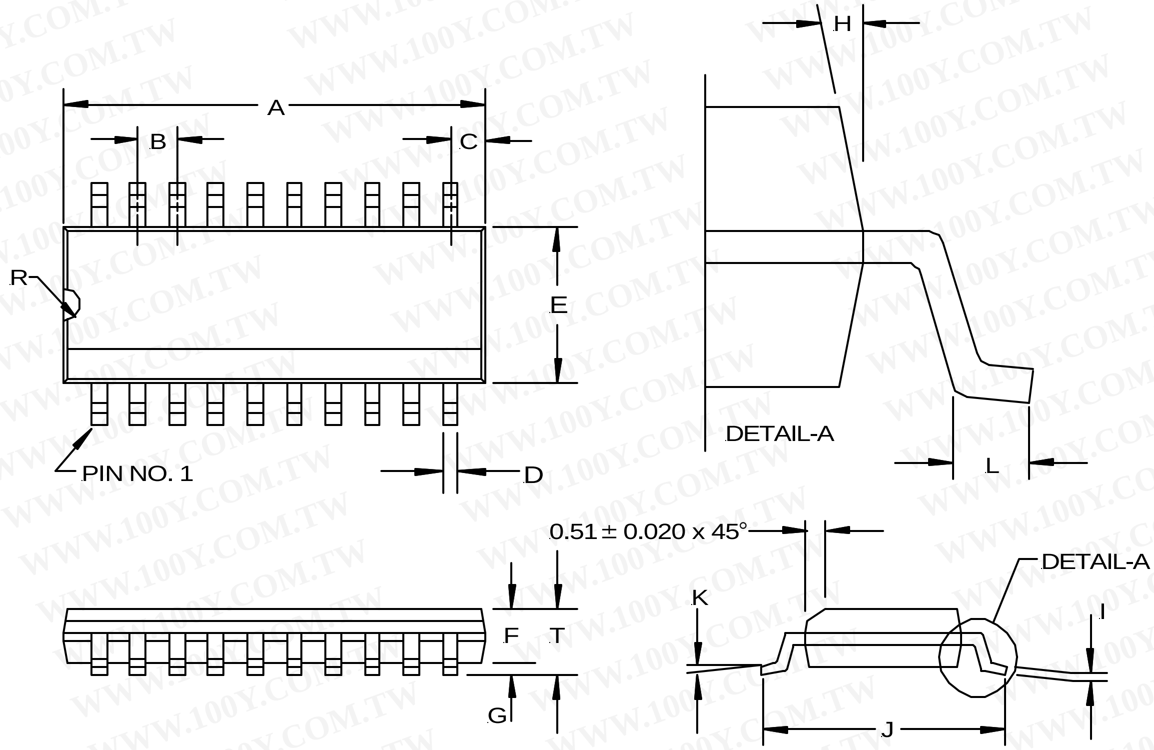


SYMBOL DESIG	20-PIN		
	MIN	NOM	MAX
A	0.65 BSC		
B	4.30	4.40	4.50
C	6.40 BSC		
D	0.19	---	0.30
E	1.00		
F	1.00		
G	6.40	6.50	6.60
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L	12° REF		
M	12° REF		
N	0°	---	8°
O	1.00 REF		
P	0.50	0.60	0.75
Q	0.20		
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

International
IOR Rectifier

(W) SOIC Package
20-Pin Surface Mount, Wide Body



SYMBOL	20-PIN	
	MIN	MAX
A	12.598	12.979
B	1.018	1.524
C	0.66 REF	
D	0.33	0.508
E	7.40	7.60
F	2.032	2.64
G	0.10	0.30
I	0.229	0.32
J	10.008	10.654
K	0°	8°
L	0.406	1.270
R	0.63	0.89
T	2.337	2.642

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
F	TSSOP Plastic	20	74	2500	Fig A
W	SOIC, Wide Body	20	38	1000	Fig B

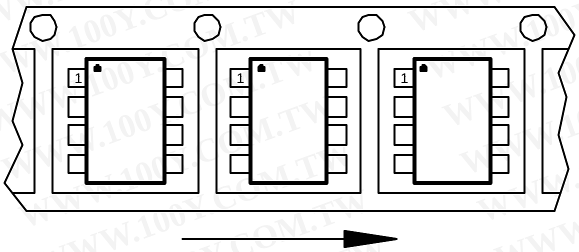


Figure A

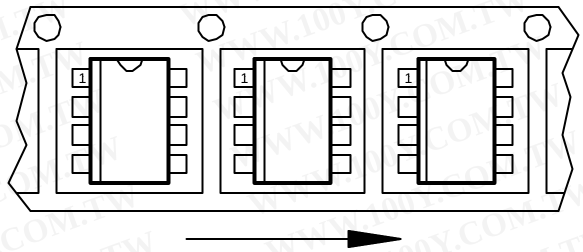


Figure B

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