

International
IR Rectifier

SMPS MOSFET

PD - 91846B
IRFR1N60A
IRFU1N60A

HEXFET® Power MOSFET

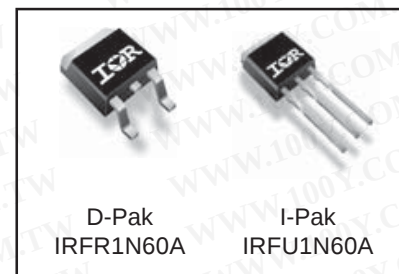
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- Power Factor Correction

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current

V _{DSS}	R _{ds(on)} max	I _D
600V	7.0Ω	1.4A



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	1.4	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	0.89	
I _{DM}	Pulsed Drain Current ①	5.6	
P _D @ T _C = 25°C	Power Dissipation	36	W
	Linear Derating Factor	0.28	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ②	3.8	V/ns
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Applicable Off Line SMPS Topologies:

- Low Power Single Transistor Flyback

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	7.0	Ω	$V_{GS} = 10V, I_D = 0.84A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 480V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	0.88	—	—	S	$V_{DS} = 50V, I_D = 0.84A$
Q_g	Total Gate Charge	—	—	14	nC	$I_D = 1.4A$
Q_{gs}	Gate-to-Source Charge	—	—	2.7		$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	8.1		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.8	—	ns	$V_{DD} = 250V$
t_r	Rise Time	—	14	—		$I_D = 1.4A$
$t_{d(off)}$	Turn-Off Delay Time	—	18	—		$R_G = 2.15\Omega$
t_f	Fall Time	—	20	—		$R_D = 178\Omega$, See Fig. 10 ④
C_{iss}	Input Capacitance	—	229	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	32.6	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	2.4	—		$f = 1.0MHz$, See Fig. 5
C_{oss}	Output Capacitance	—	320	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	11.5	—		$V_{GS} = 0V, V_{DS} = 480V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	130	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V$ ⑤

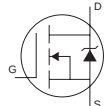
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	93	mJ
I_{AR}	Avalanche Current①	—	1.4	A
E_{AR}	Repetitive Avalanche Energy①	—	3.6	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)③	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.4	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	5.6		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_J = 25^\circ\text{C}, I_S = 1.4A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	290	440	ns	$T_J = 25^\circ\text{C}, I_F = 1.4A$
Q_{rr}	Reverse Recovery Charge	—	510	760	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

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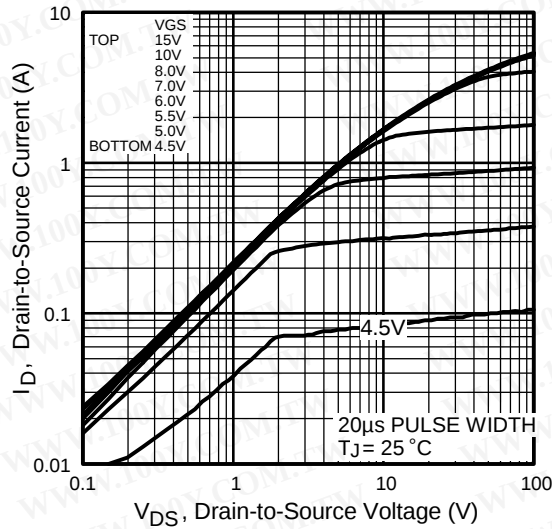


Fig 1. Typical Output Characteristics

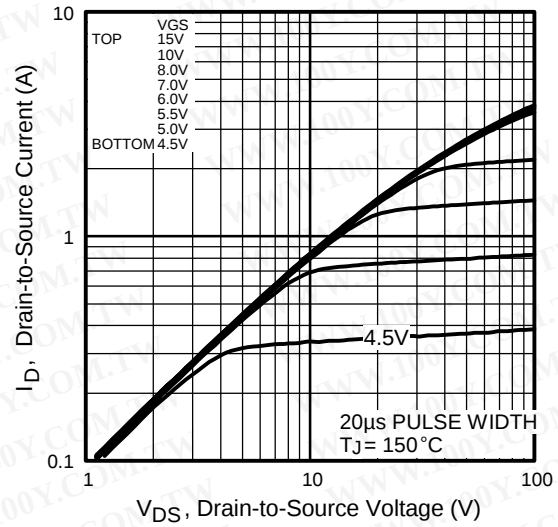


Fig 2. Typical Output Characteristics

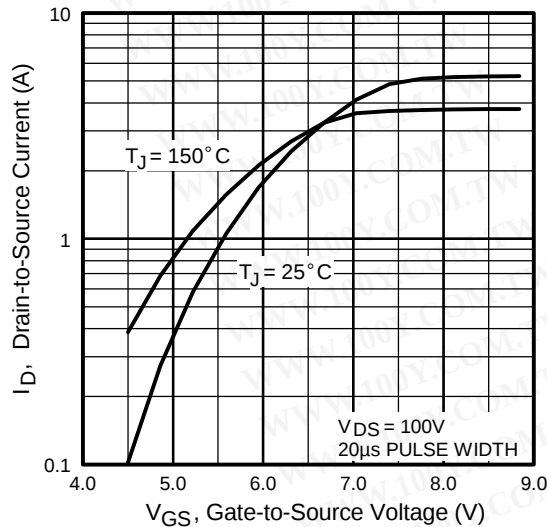


Fig 3. Typical Transfer Characteristics

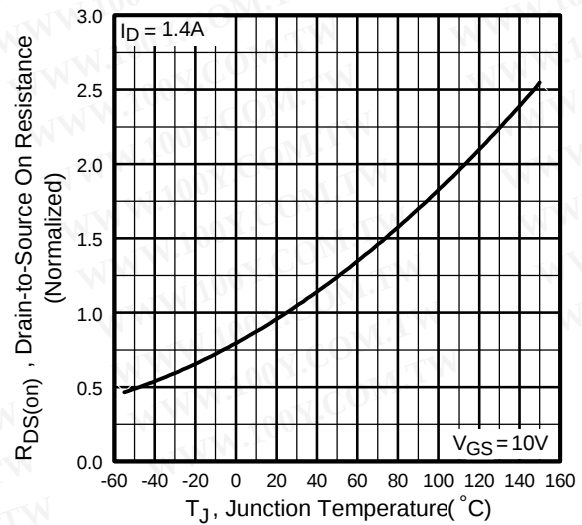


Fig 4. Normalized On-Resistance Vs. Temperature

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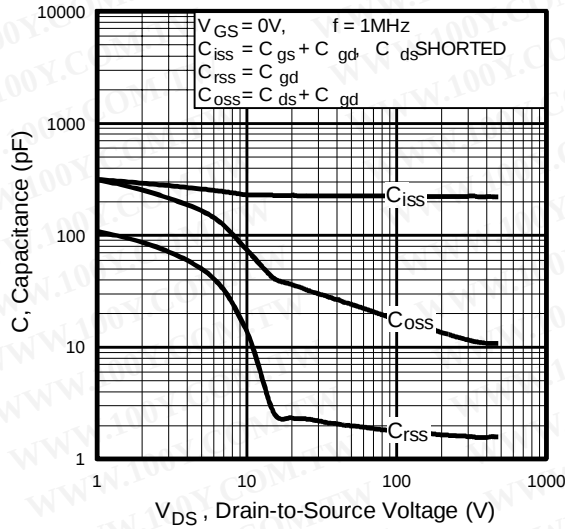


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

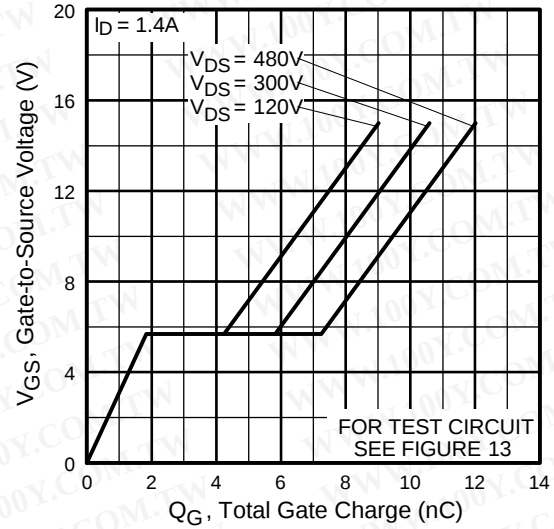


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

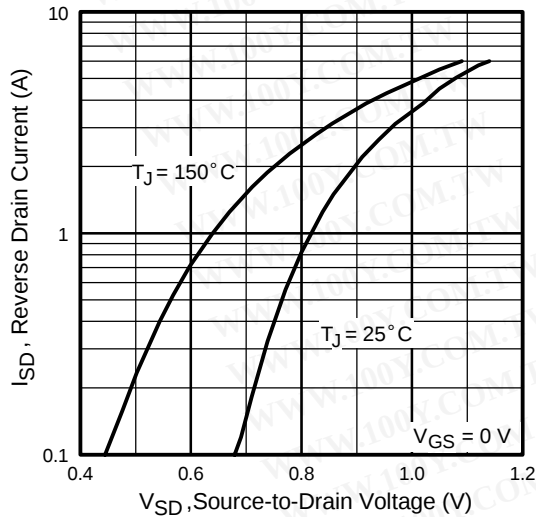


Fig 7. Typical Source-Drain Diode Forward Voltage

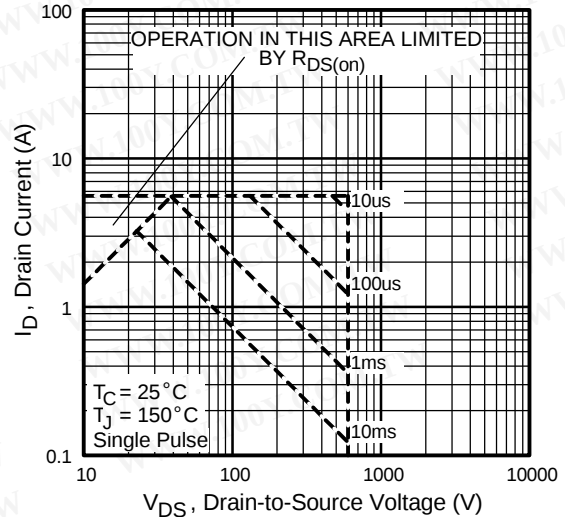


Fig 8. Maximum Safe Operating Area

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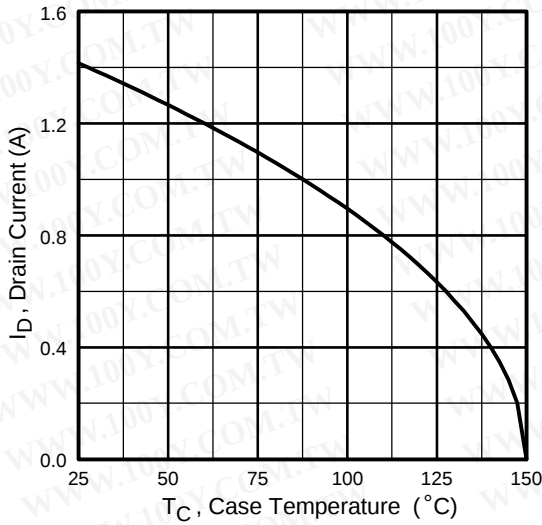


Fig 9. Maximum Drain Current Vs. Case Temperature

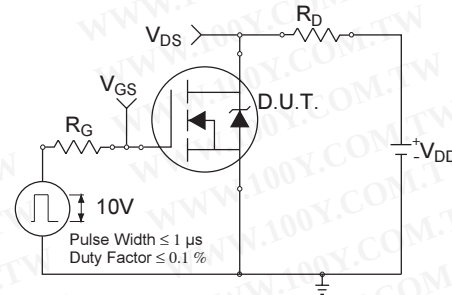


Fig 10a. Switching Time Test Circuit

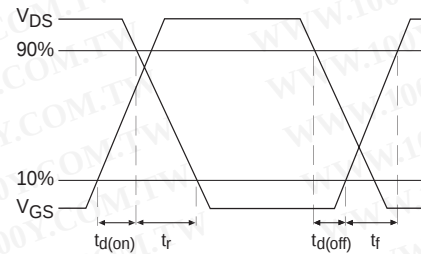


Fig 10b. Switching Time Waveforms

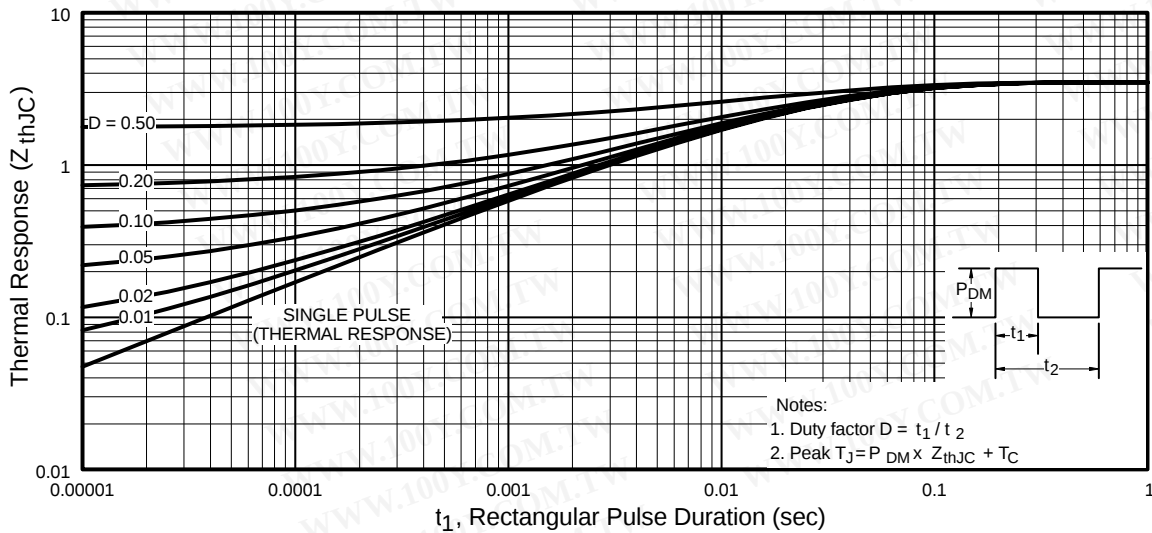


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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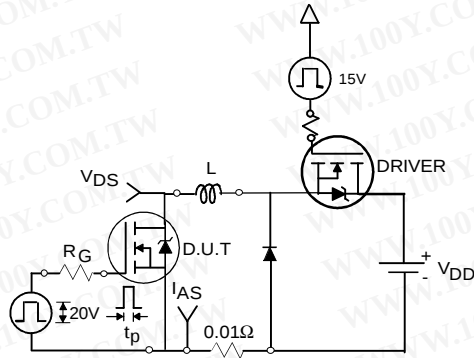


Fig 12a. Unclamped Inductive Test Circuit

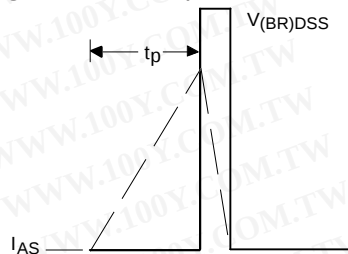


Fig 12b. Unclamped Inductive Waveforms

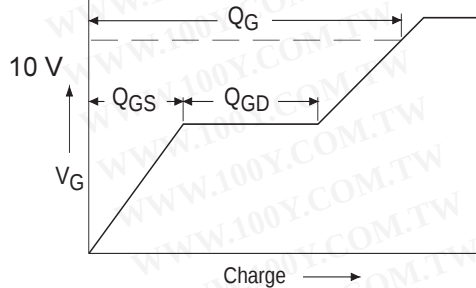


Fig 13a. Basic Gate Charge Waveform

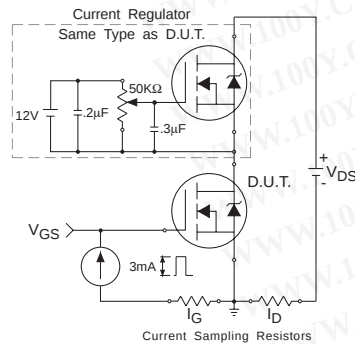


Fig 13b. Gate Charge Test Circuit

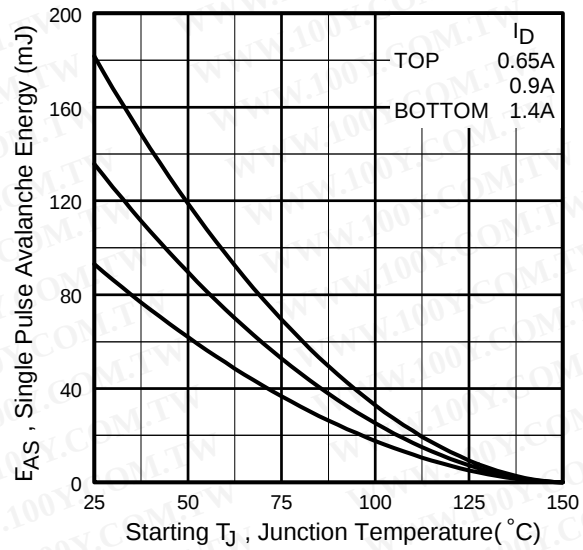


Fig 12c. Maximum Avalanche Energy
 Vs. Drain Current

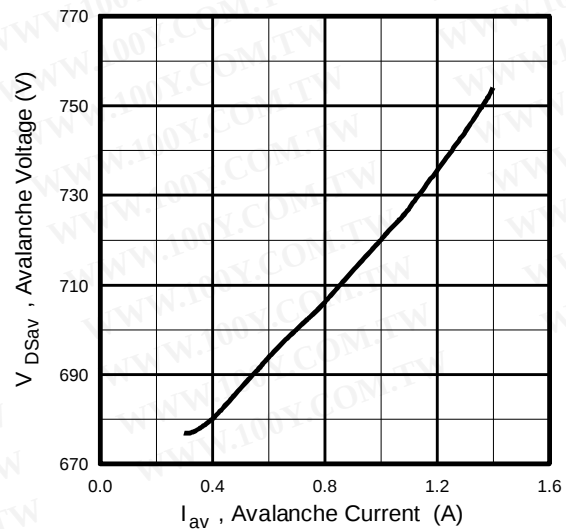
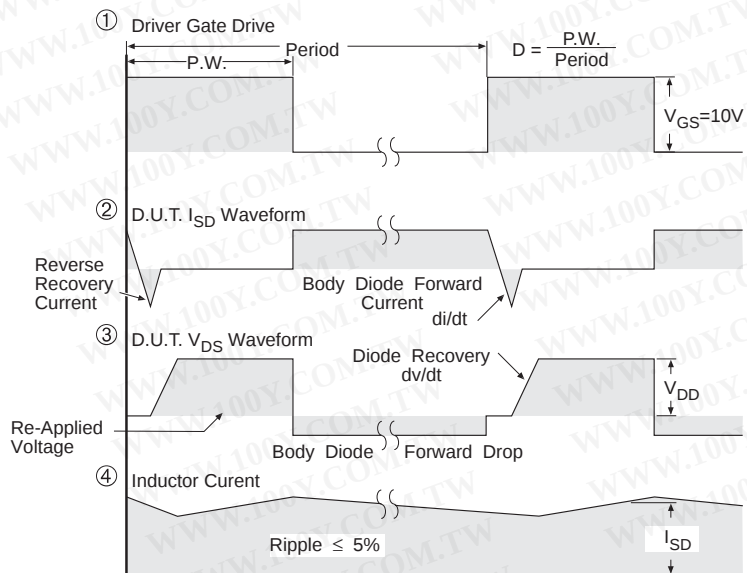
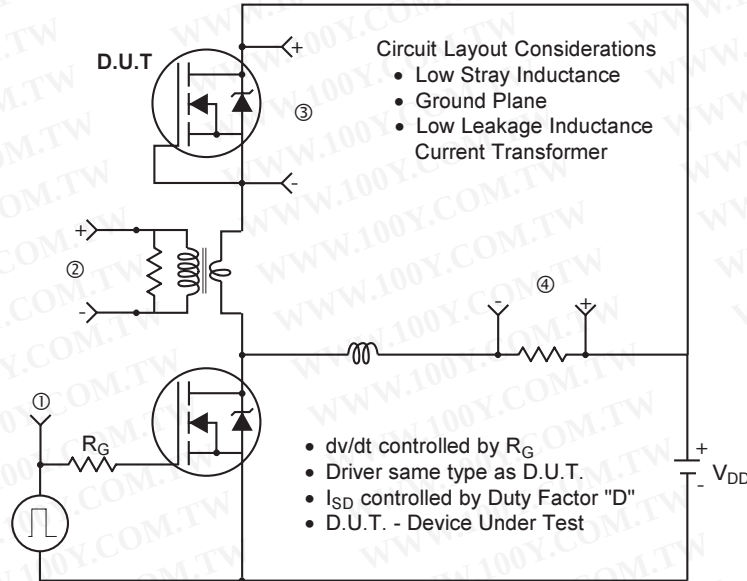


Fig 12d. Typical Drain-to-Source Voltage
 Vs. Avalanche Current

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Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

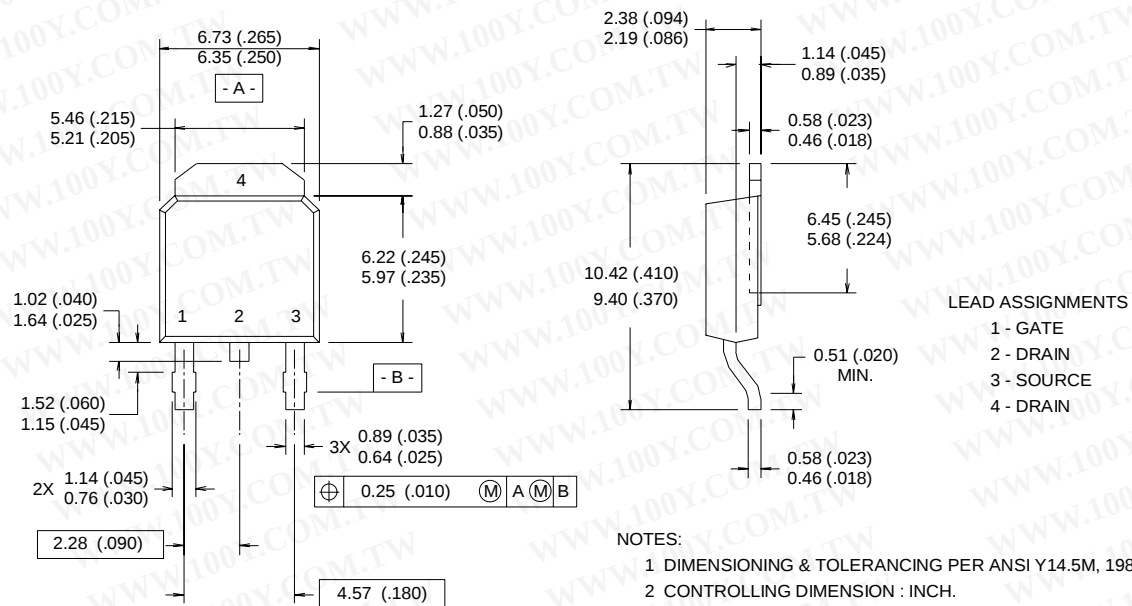
Fig 14. For N-Channel HEXFETS

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D-Pak (TO-252AA) Package Outline

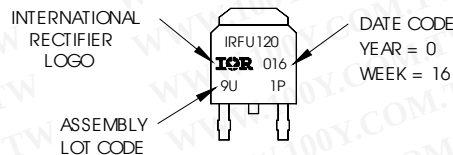
Dimensions are shown in millimeters (inches)



D-Pak (TO-252AA) Part Marking Information

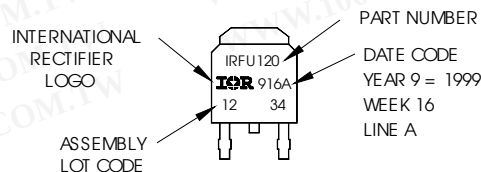
Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
 WITH ASSEMBLY
 LOT CODE 9U1P



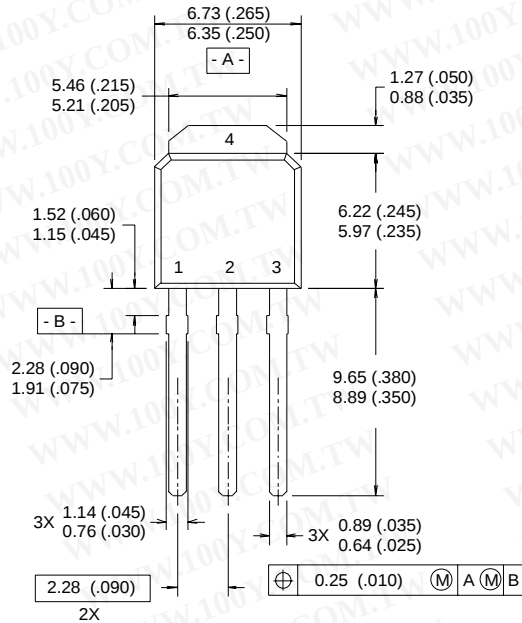
Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
 WITH ASSEMBLY
 LOT CODE 1234
 ASSEMBLED ON WW 16, 1999
 IN THE ASSEMBLY LINE "A"



International **IR** Rectifier I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



IRFR/U1N60A

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

NOTES:

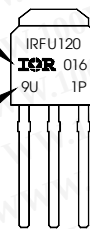
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-252AA.
- 4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

I-Pak (TO-251AA) Part Marking Information

Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P

INTERNATIONAL
RECTIFIER
LOGO

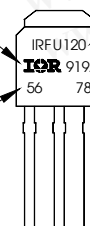


DATE CODE
YEAR = 0
WEEK = 16

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

INTERNATIONAL
RECTIFIER
LOGO



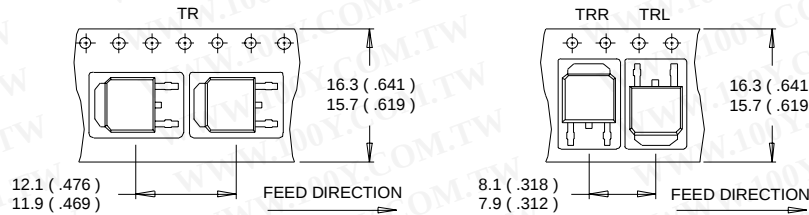
PART NUMBER
DATE CODE
YEAR 9 = 1999
WEEK 19
LINE A

IRFR/U1N60A

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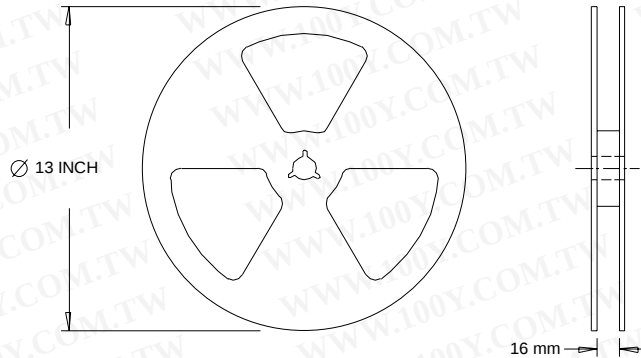
Tape & Reel Information

TO-252AA



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 95\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 1.4\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 1.4\text{A}$, $di/dt \leq 180\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ When mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

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