

4A, 100V, 0.60 Ohm, P-Channel Power MOSFET

This P-Channel enhancement mode silicon gate power field effect transistor is designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17501.

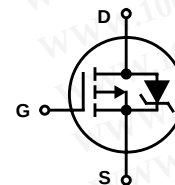
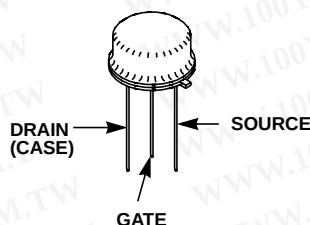
Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFF9120	TO-205AF	IRFF9120

NOTE: When ordering, use the entire part number.

Features

- 4A, 100V
- $r_{DS(ON)} = 0.60\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Symbol**Packaging****JEDEC TO-205AF**

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

IRFF9120

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

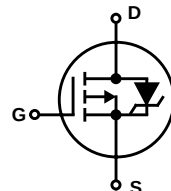
	IRFF9120	UNITS
Drain to Source Voltage (Note 1)	V_{DS} -100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR} -100	V
Continuous Drain Current, $T_C = 25^{\circ}\text{C}$	I_D -4	A
Pulsed Drain Current (Note 3)	I_{DM} -16	A
Gate to Source Voltage	V_{GS} ± 20	V
Maximum Power Dissipation, (Figure 14)	P_D 20	W
Linear Derating Factor (Figure 14)	0.16	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS} 370	mJ
Operating and Storage Temperature	T_J, T_{STG} -55 to 150	$^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	T_L 300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg} 260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA		-100	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Max Rating, V _{GS} = 0V		-	-	-250	μA
		V _{DS} = Max Rating x 0.8, V _{GS} = 0V, T _J = 125°C		-	-	-1000	μA
On-State Drain Current (Note 2)	I _{D(ON)}	V _{DS} > I _{D(ON)} × r _{DS(ON)MAX} , V _{GS} = -10V		-4	-	-	A
Gate to Source Leakage Forward	I _{GSS}	V _{GS} = -20V		-	-	-100	nA
Gate to Source Leakage Reverse	I _{GSS}	V _{GS} = 20V		-	-	100	nA
Drain to Source On-State Resistance (Note 2)	r _{DS(ON)}	V _{GS} = 10V, I _D = -2A		-	0.5	0.6	Ω
Forward Transconductance (Note 2)	g _{fs}	V _{DS} > I _{D(ON)} × r _{DS(ON)} Max, I _D = 2A		1.25	2	-	S
Turn-On Delay Time	t _{D(ON)}	V _{DD} ≅ 0.5BV _{DSS} , I _D = 4A, R _G = 9.1Ω (Figure 18) MOSFET Switching Times are Essentially Independent of Operating Temperature		-	25	50	ns
Rise Time	t _r			-	50	100	ns
Turn-Off Delay Time	t _{D(OFF)}			-	50	100	ns
Fall Time	t _f			-	50	100	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q _{G(TOT)}	V _{GS} = 10V, I _D = 4A, V _{DS} = 0.8 Max BV _{DSS} (See Figure 18 for Test Circuit) Gate Charge is Essentially Independent of Operating Temperature		-	16	22	nC
Gate to Source Charge	Q _{GS}			-	9	-	nC
Gate to Drain “Miller” Charge	Q _{GD}			-	7	-	nC
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz, See Figure 10		-	300	-	pF
Output Capacitance	C _{OSS}			-	200	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	50	-	pF
Internal Drain Inductance	L _D	Measured from the Drain Lead, 5.0mm (0.2in) From Header to Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances 	-	5.0	-	nH
Internal Source Inductance	L _S	Measured from the Source Lead, 5.0mm (0.2in) from Header to Source Bonding Pad		-	15	-	nH
Junction to Case	R _{θJC}			-	-	6.25	°C/W
Junction to Ambient	R _{θJA}	Typical Socket Mount		-	-	175	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier	-	-	-4	A
Pulse Source Current (Note 3)	I_{SM}		-	-	-16	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = -4\text{A}$, $V_{GS} = 0\text{V}$	-	-	-1.5	V
Diode Reverse Recovery Time	t_{rr}	$T_J = 150^{\circ}\text{C}$, $I_{SD} = 4\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	230	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^{\circ}\text{C}$, $I_{SD} = -4\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	1.3	-	μC

NOTES:

- Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle 2%.
- Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 3).
- $V_{DD} = 25\text{V}$, starting $T_J = 250^{\circ}\text{C}$, $L = 34.7\text{mH}$, $R_G = 25\Omega$, peak $I_{AS} = 4.0\text{A}$. See Figures 15 and 16)

Typical Performance Curves

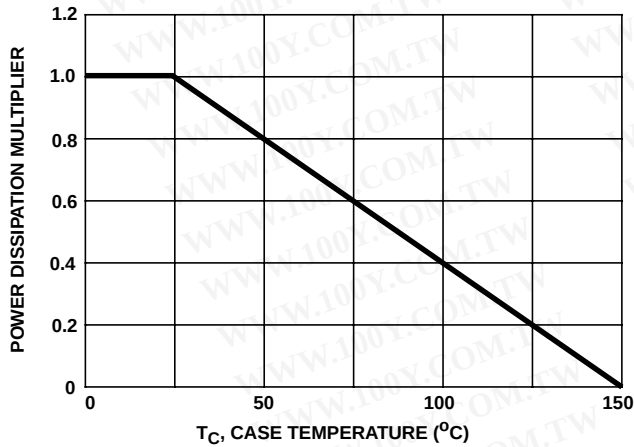


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

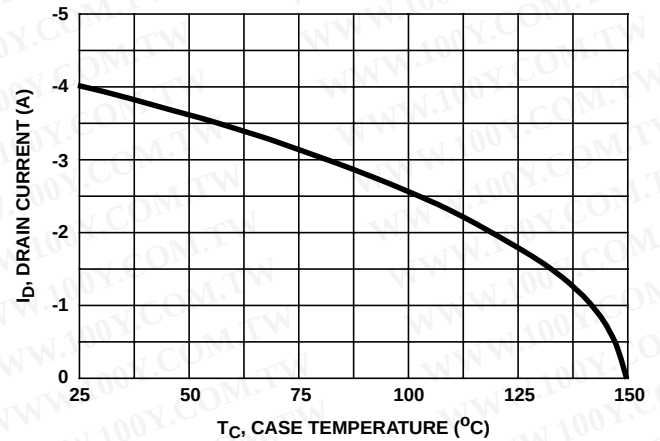


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

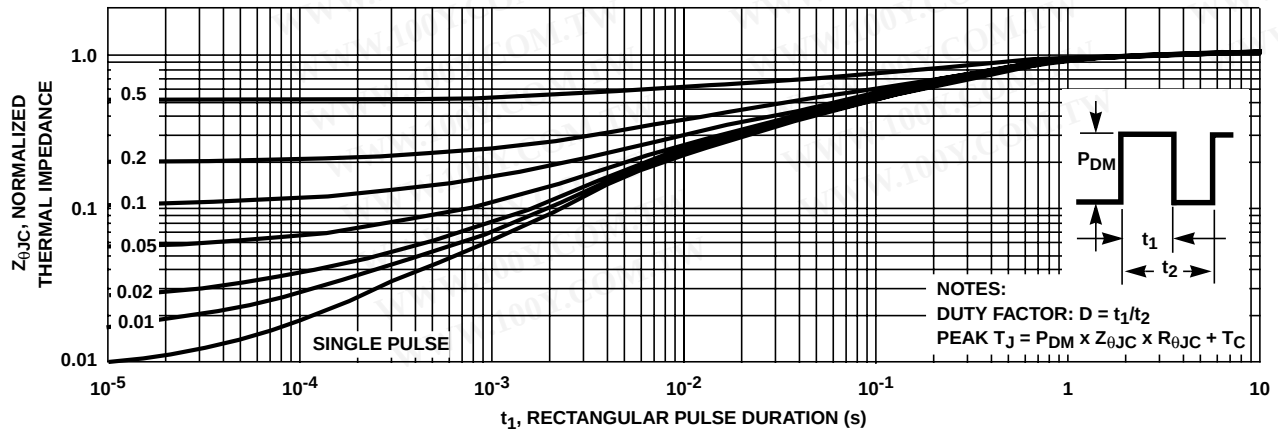


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

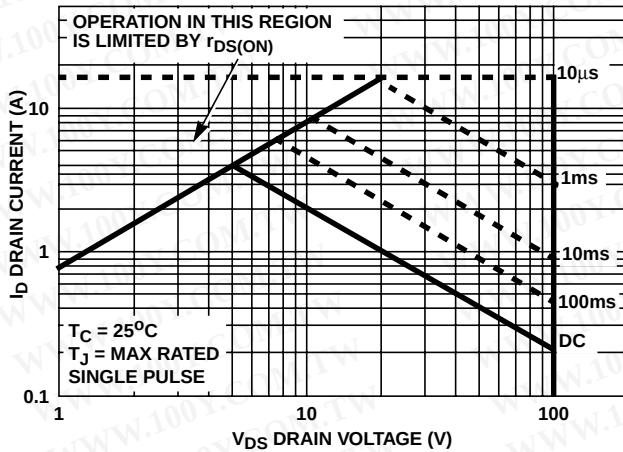


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

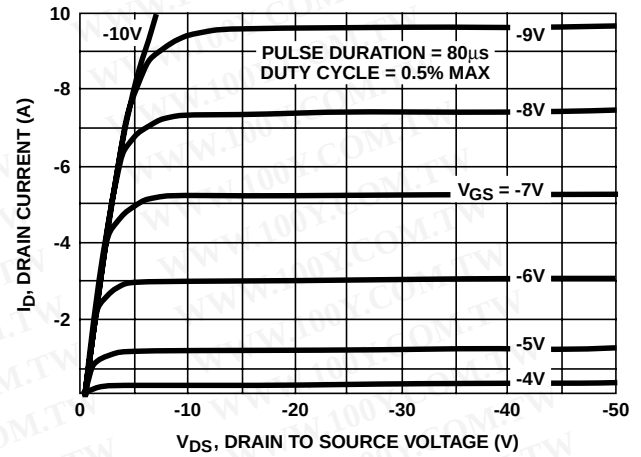


FIGURE 5. OUTPUT CHARACTERISTICS

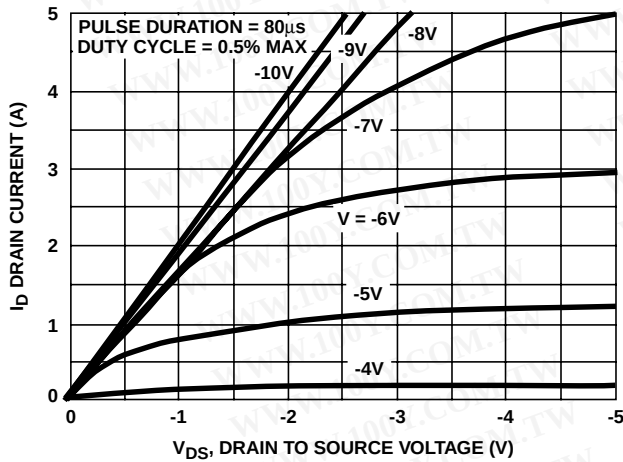


FIGURE 6. SATURATION CHARACTERISTICS

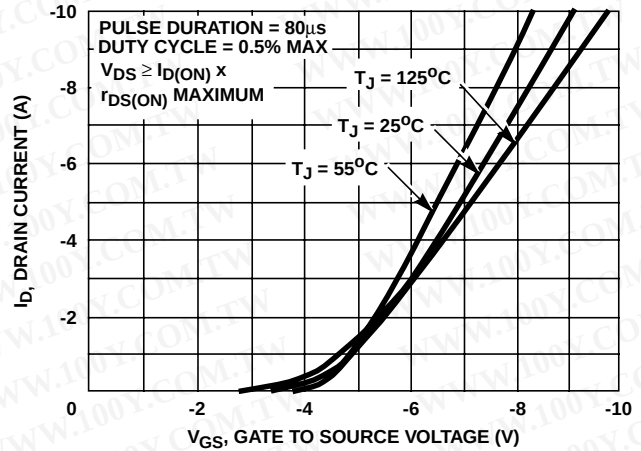


FIGURE 7. TRANSFER CHARACTERISTICS

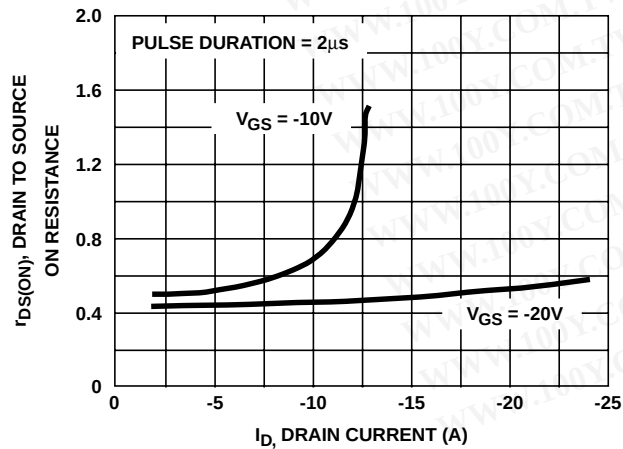


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

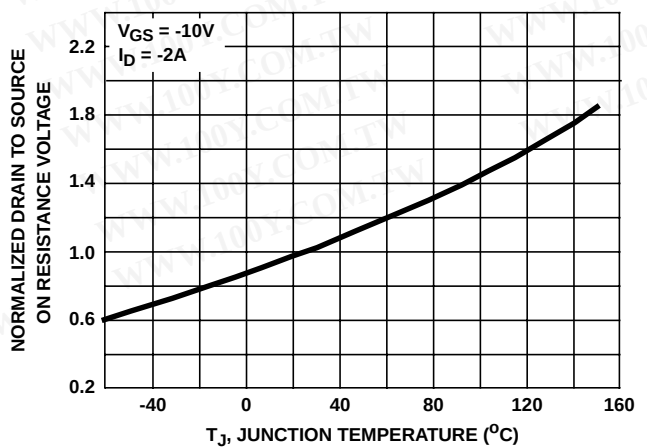


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

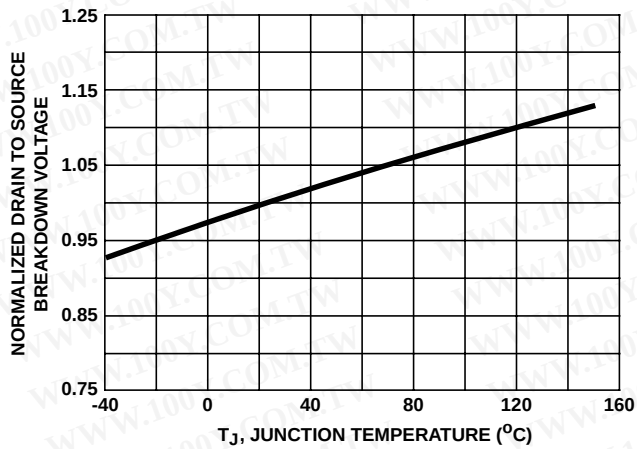


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

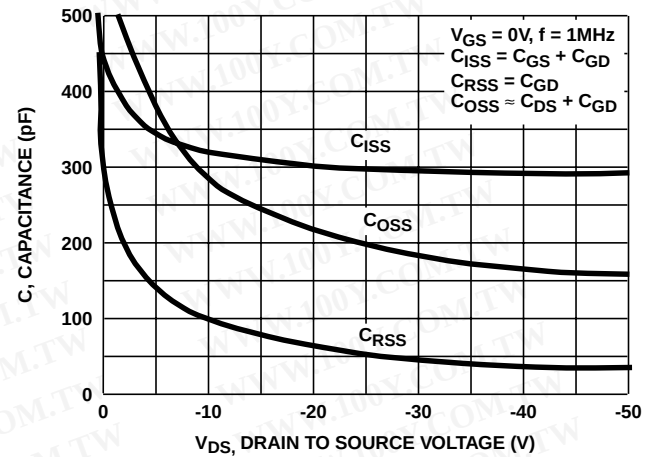


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

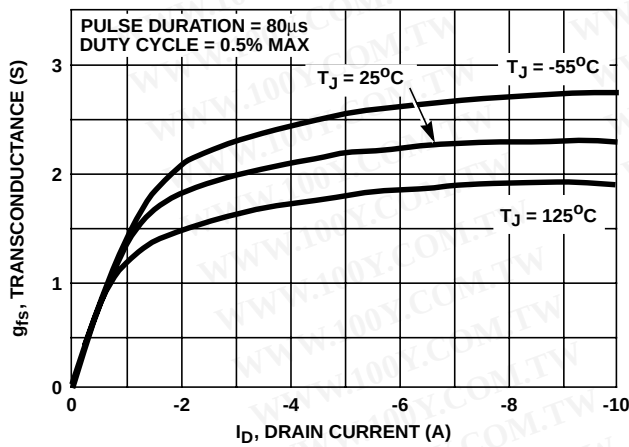


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

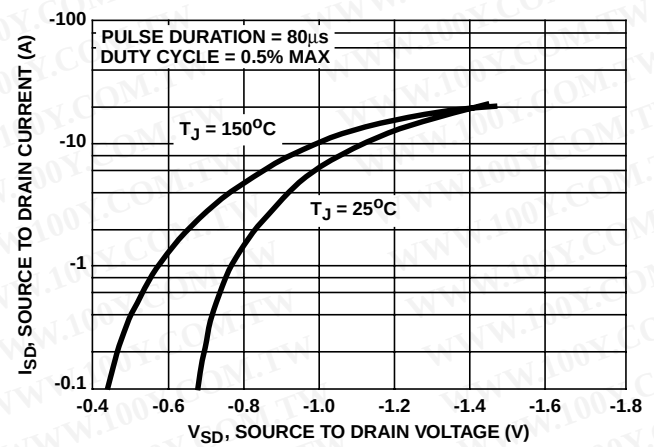


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

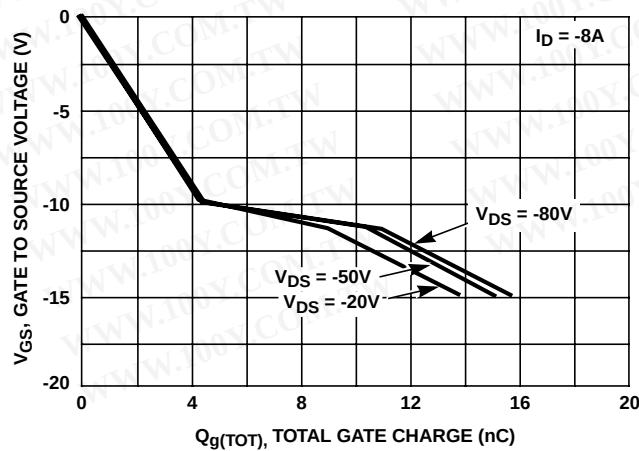


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

IRFF9120

Typical Performance Curves (Continued)

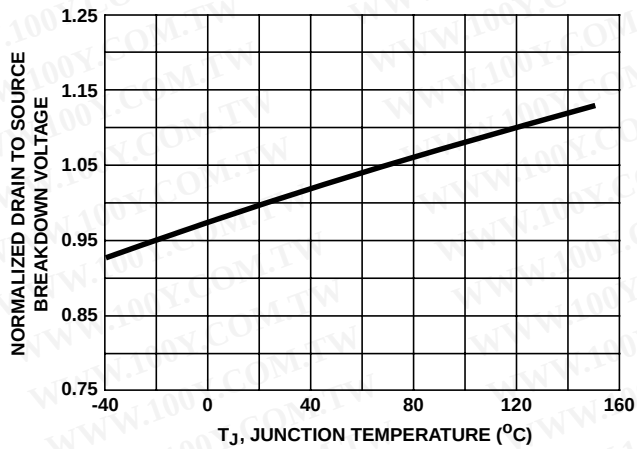


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

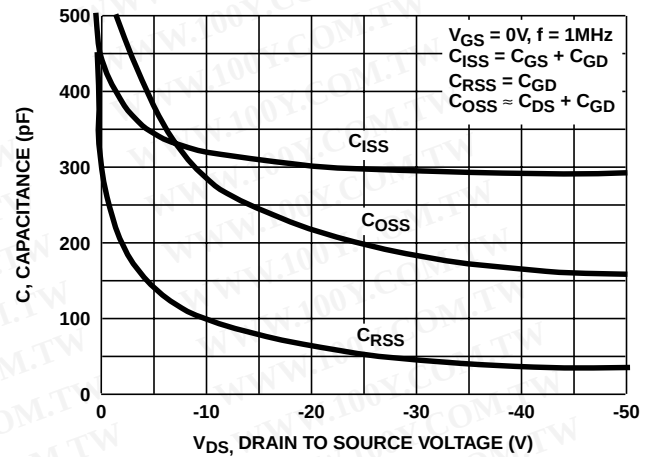


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

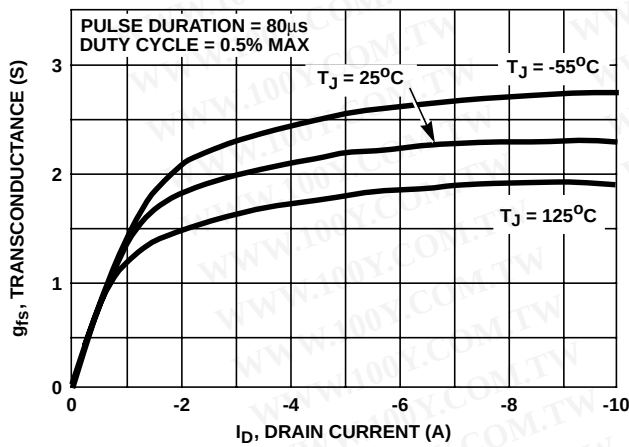


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

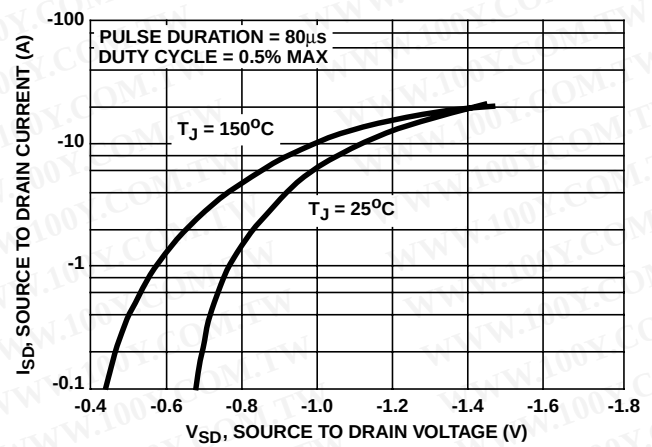


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

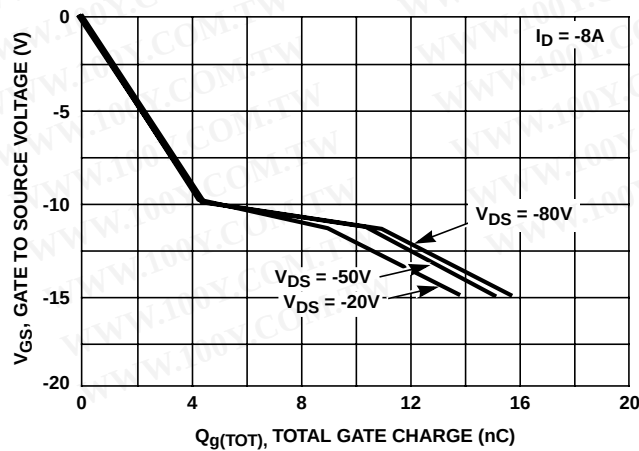


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE