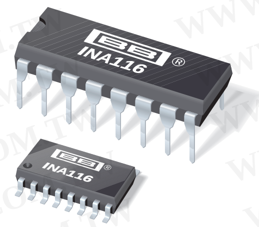
BURR - BROWN®



INA116

Ultra Low Input Bias Current INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW INPUT BIAS CURRENT: 3fA typ**
- **BUFFERED GUARD DRIVE PINS**
- **LOW OFFSET VOLTAGE: 2mV max**
- **HIGH COMMON-MODE REJECTION: 84dB (G = 10)**
- **LOW QUIESCENT CURRENT: 1mA**
- **INPUT OVER-VOLTAGE PROTECTION: ±40V**

APPLICATIONS

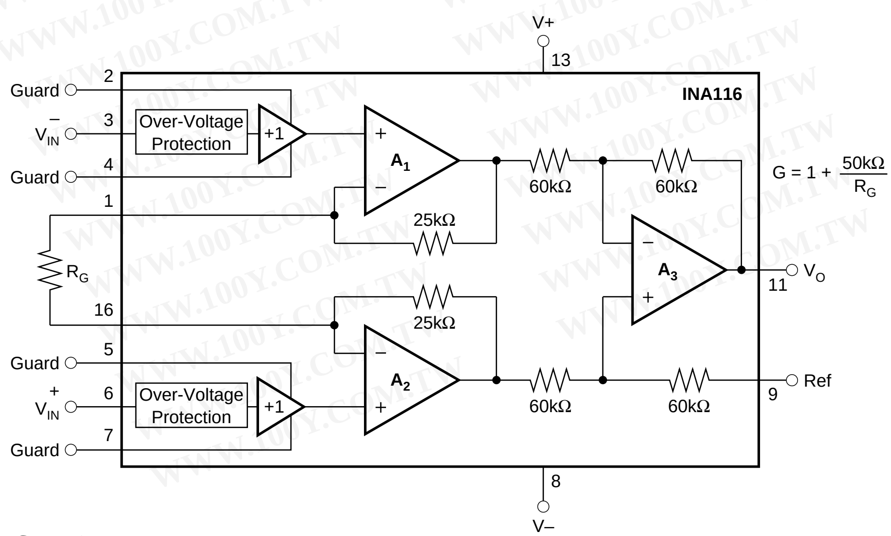
- **LABORATORY INSTRUMENTATION**
- **pH MEASUREMENT**
- **ION–SPECIFIC PROBES**
- **LEAKAGE CURRENT MEASUREMENT**

DESCRIPTION

The INA116 is a complete monolithic FET-input instrumentation amplifier with extremely low input bias current. ***Difet***® inputs and special guarding techniques yield input bias currents of 3fA at 25°C, and only 25fA at 85°C. Its 3-op amp topology allows gains to be set from 1 to 1000 by connecting a single external resistor.

Guard pins adjacent to both input connections can be used to drive circuit board and input cable guards to maintain extremely low input bias current.

The INA116 is available in 16-pin plastic DIP and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.



Difet®; Burr-Brown Corporation

 PDS-1242B Printed in U.S.A. May, 1995

SPECIFICATIONS

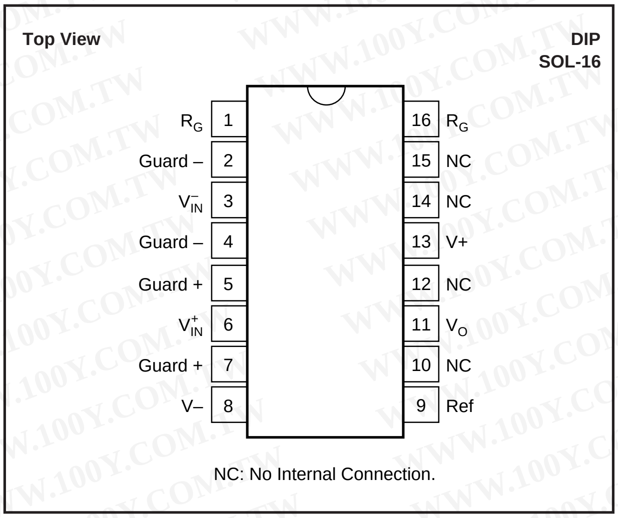
AT T_A = +25°C, V_S = ±15V, R_L = 10kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	INA116P, U			INA116PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±0.5 ±0.5/G	±2 ±2/G		*	±5 ±5/G	mV
vs Temperature	T_A = T_{MIN} to T_{MAX}		See Typical Curve			*		
vs Power Supply	V_S = ±4.5V to ±18V		±10 ±15/G	±50 ±100/G		*	±100 ±200/G	µV/V
Long-Term Stability			±1 ±5/G			*		µV/mo
Bias Current			±3	±25		*	±100	fA
vs Temperature			See Typical Curve			*		
Offset Current			±1	±25		*	±100	fA
vs Temperature			See Typical Curve			*		
Impedance, Differential			$>10^{15}/0.2$			*		Ω/pF
Common-Mode			$>10^{15}/7$			*		Ω/pF
Common-Mode Voltage Range		(V+)–4	(V+)–2		*	*		V
		(V–)+4	(V–)+2.4		*	*		V
Safe Input Voltage		±40			*			V
Common-Mode Rejection	V_{CM} = ±11V, ΔR_S = 1kΩ							
	G = 1	80	89		73	*		dB
	G = 10	84	92		78	*		dB
	G = 100	86	94		80	*		dB
	V_{CM} = ±5V, G = 1000	86	94		80	*		dB
NOISE								
Voltage Noise, RTI	G = 1000, R_S = 0Ω							
f = 1kHz			28			*		nV/√Hz
f_B = 0.1Hz to 10Hz			2			*		µVp-p
Current Noise								
f = 1kHz			0.1			*		fA/√Hz
GAIN								
Gain Equation			1+(50kΩ/R_G)			*		V/V
Range of Gain		1		1000	*		*	V/V
Gain Error	G = 1		±0.01	±0.05		*	0.1	%
	G = 10		±0.25	±0.4		*	±0.5	%
	G = 100		±0.35	±0.5		*	±0.7	%
	G = 1000		±1.25			*		%
Gain vs Temperature(1)	G = 1		±5	±10		*	±20	ppm/°C
50kΩ Resistance(1)(2)			±25	±100		*	±100	ppm/°C
Nonlinearity	G = 1		±0.0005	±0.005		*	±0.01	% of FSR
	G = 10		±0.001	±0.005		*	±0.01	% of FSR
	G = 100		±0.001	±0.005		*	±0.01	% of FSR
	G = 1000		±0.005			*		% of FSR
GUARD OUTPUTS								
Offset Voltage			±15	±50		*	*	mV
Output Impedance			650			*		Ω
Current Drive			+2/–0.05			*		mA
OUTPUT								
Voltage Positive	R_L = 10kΩ	(V+) –1	(V+) –0.7		*	*		V
Negative	R_L = 10kΩ	(V–) +0.35	(V–) +0.2		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+5/–12			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		800			*		kHz
	G = 10		500			*		kHz
	G = 100		70			*		kHz
	G = 1000		7			*		kHz
Slew Rate	G = 10 to 200		0.8			*		V/µs
Settling Time, 0.01%	10V Step, G = 1		22			*		µs
	G = 10		25			*		µs
	G = 100		145			*		µs
	G = 1000		400			*		µs
Output Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±4.5	±15	±18	*	*	*	V
Current	V_{IN} = 0V		±1	±1.4		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as INA116P

NOTE: (1) Guaranteed by wafer test. (2) Temperature coefficient of the "50kΩ" term in the gain equation.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

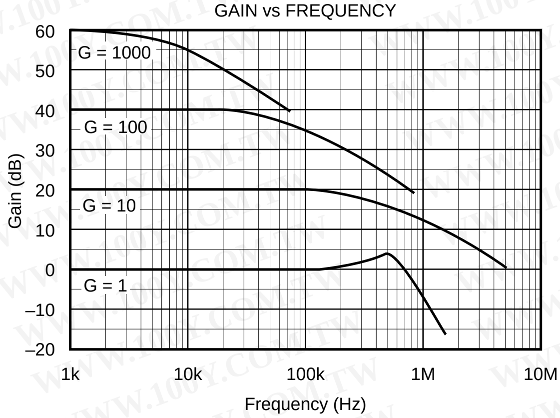
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA116PA	16-Pin Plastic DIP	180
INA116P	16-Pin Plastic DIP	180
INA116UA	SOL-16 Surface-Mount	211
INA116U	SOL-16 Surface-Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

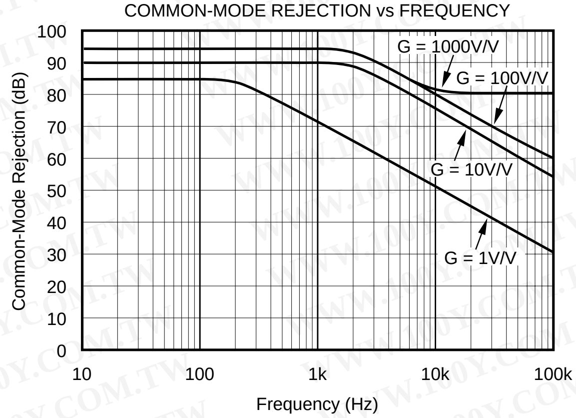
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, unless otherwise noted.

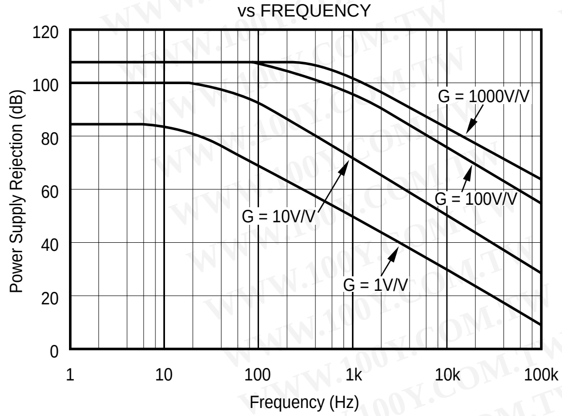
GAIN vs FREQUENCY



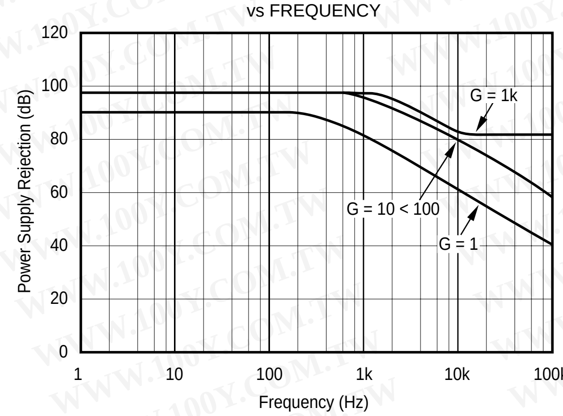
COMMON-MODE REJECTION vs FREQUENCY



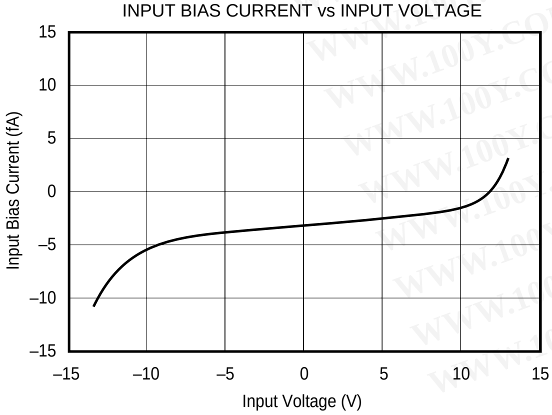
POSITIVE POWER SUPPLY REJECTION
vs FREQUENCY



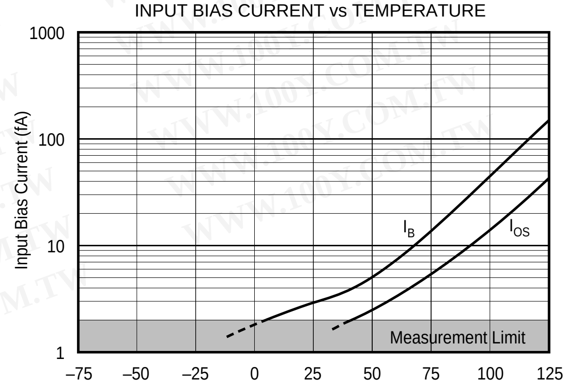
NEGATIVE POWER SUPPLY REJECTION
vs FREQUENCY



INPUT BIAS CURRENT vs INPUT VOLTAGE



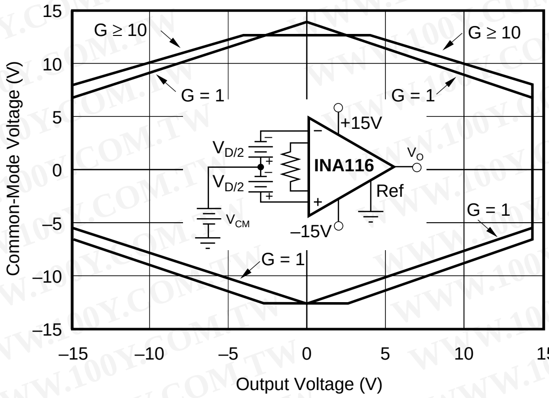
INPUT BIAS CURRENT vs TEMPERATURE



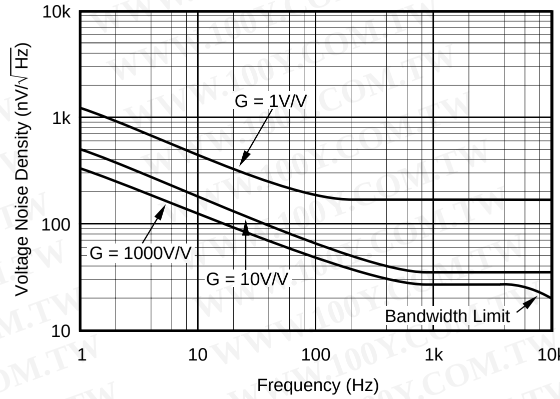
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, unless otherwise noted.

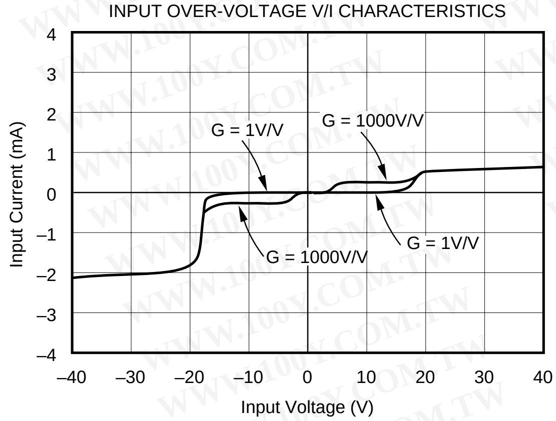
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE



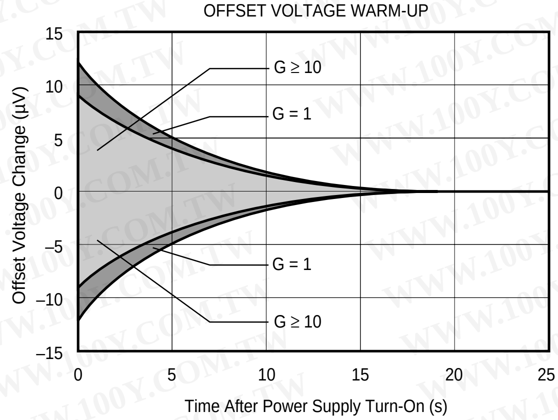
INPUT REFERRED NOISE vs FREQUENCY



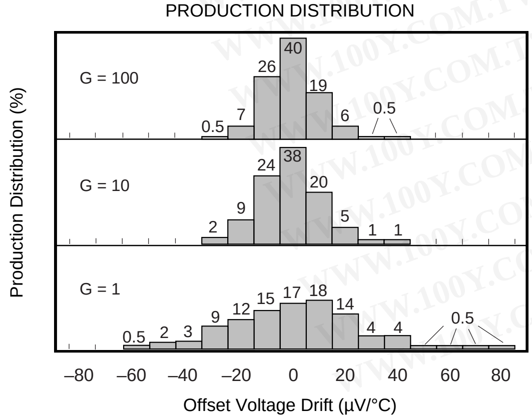
INPUT OVER-VOLTAGE V/I CHARACTERISTICS



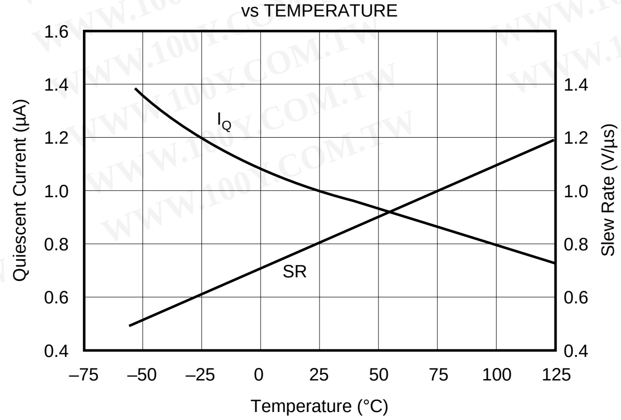
OFFSET VOLTAGE WARM-UP



INPUT OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



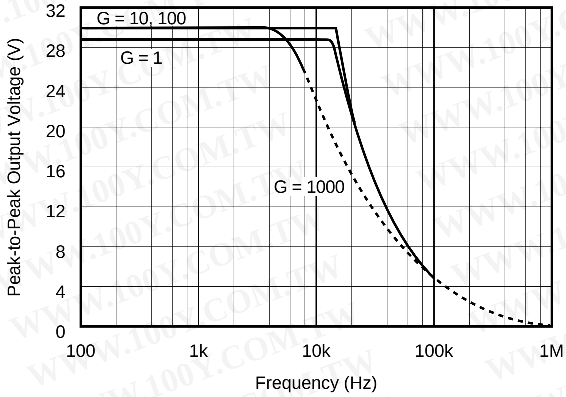
QUIESCENT CURRENT AND SLEW RATE vs TEMPERATURE



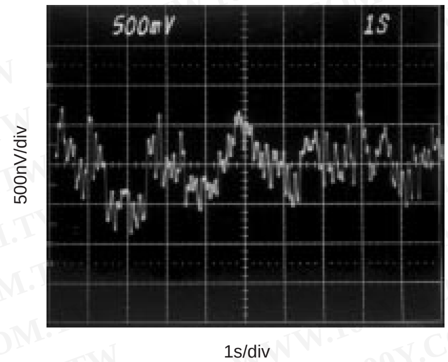
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, unless otherwise noted.

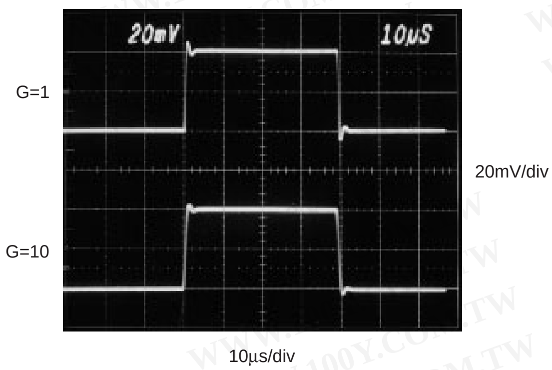
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



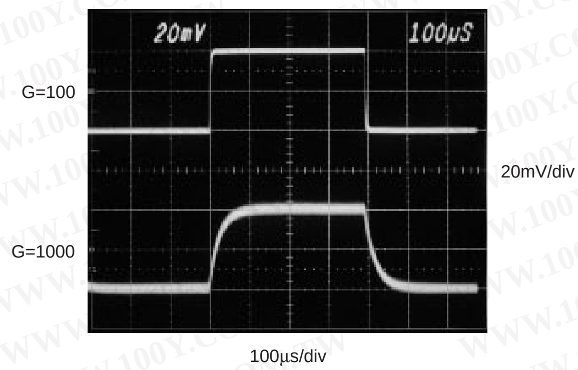
VOLTAGE NOISE, 0.1 TO 10Hz
INPUT-REFERRED, G ≥ 100



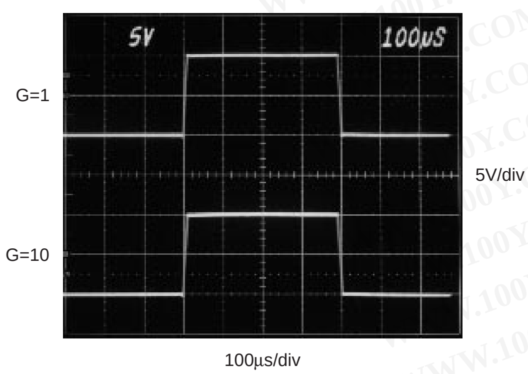
SMALL SIGNAL RESPONSE



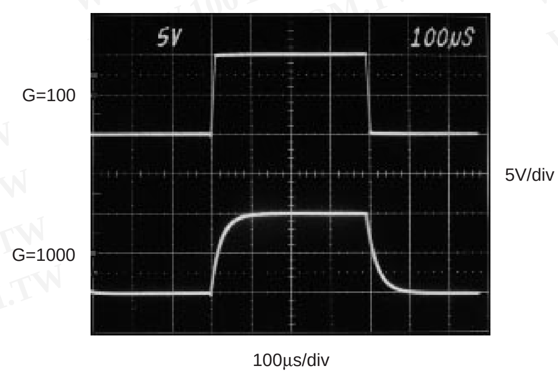
SMALL SIGNAL RESPONSE



LARGE SIGNAL RESPONSE



LARGE SIGNAL RESPONSE



APPLICATIONS INFORMATION

Figure 1 shows the connections required for basic operation of the INA116. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the supply pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low impedance connection to assure good common-mode rejection. A resistance of 30Ω in series with this connection will cause a typical device to degrade to approximately 72dB CMR at G = 1.

SETTING THE GAIN

Gain of the INA116 is set by connecting a single external resistor, R_G, as shown. The gain is—

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

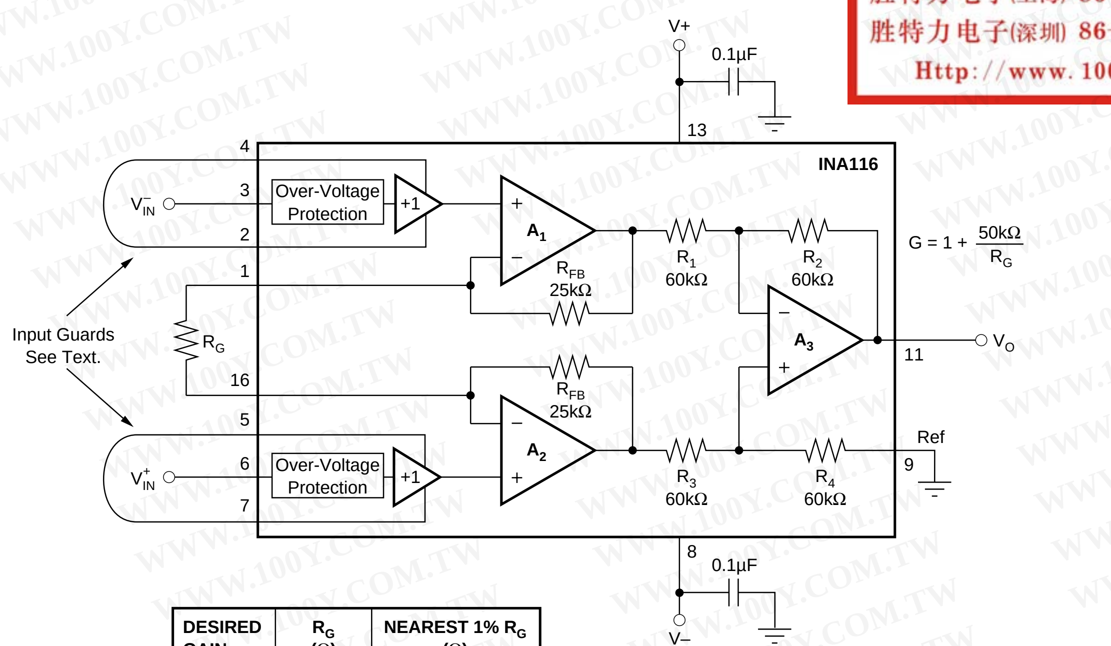
Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in equation 1 is the sum of the two feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA116.

The stability and temperature drift of R_G also affect gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain make wiring resistance important. Sockets add to the wiring resistance that will contribute additional gain error in gains of approximately 100 or greater.

OFFSET TRIMMING

The INA116 is laser trimmed for low offset voltage and offset voltage drift; most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. A voltage applied to the Ref terminal is summed at the output. Op amp A_1 provides a low source impedance for the Ref terminal, assuring good common-mode rejection.



DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.

Also drawn in simplified form:

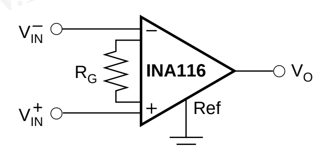


FIGURE 1. Basic Connections.

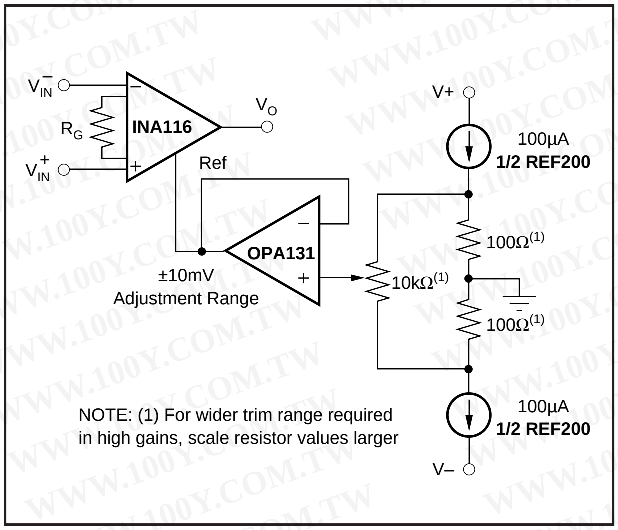


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

Input circuitry must provide an input bias current path for proper operation. Figure 3 shows resistors R_1 and R_2 to provide an input current path. Without these resistors, the inputs would eventually float to a potential that exceeds the common-mode range of the INA116 and the input amplifiers would saturate. Because of its exceedingly low input bias current, improperly biased inputs may operate normally for a period of time after power is first applied, or operate intermittently.

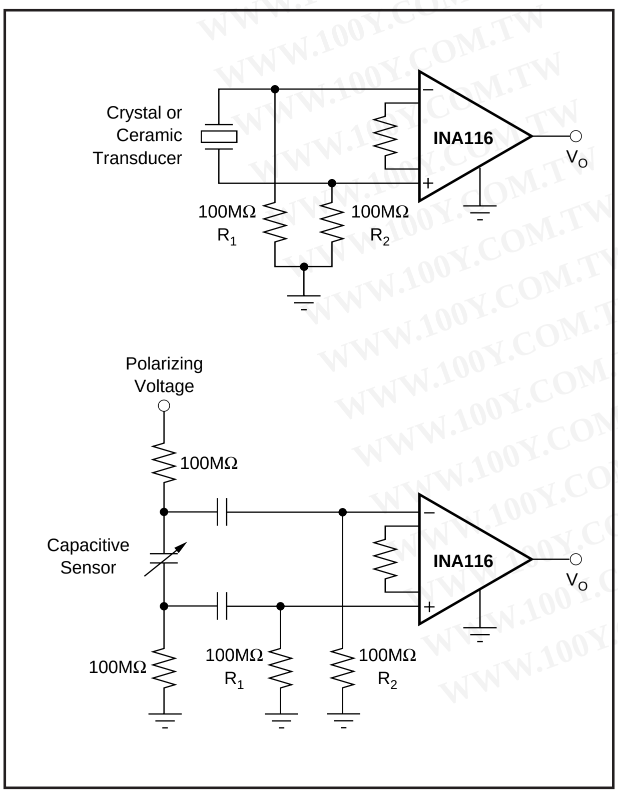


FIGURE 3. Providing An Input Bias Current Path.

CIRCUIT BOARD LAYOUT AND ASSEMBLY

Careful circuit board layout and assembly techniques are required to achieve the exceptionally low input bias current performance of the INA116. Guard terminals adjacent to both inputs make it easy to properly guard the critical input terminal layout. Since traces are not required to run between device pins, this layout is easily accomplished, even with the surface mount package. The guards should completely encircle their respective input connections—see Figure 4. Both sides of the circuit board should be guarded, even if only one side has an input terminal conductor. Route any time-varying signals away from the input terminals. Solder mask should not cover the input and guard traces since this can increase leakage.

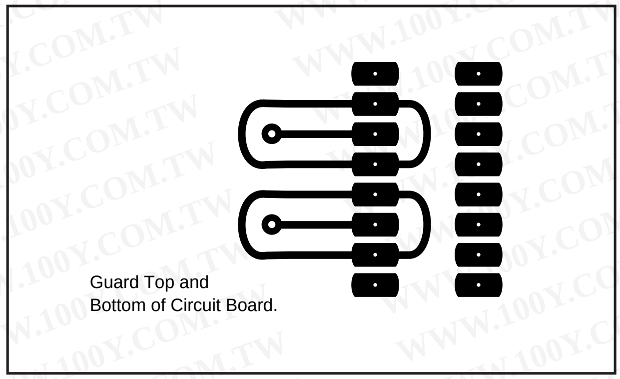


FIGURE 4. Circuit Board Guard Layout.

After assembly, the circuit board should be cleaned. Commercial solvents should be chosen according to the soldering method and flux used. Solvents should be cleaned and replaced often. Solvent cleaning should be followed by a deionized water rinse and 85°C bake out.

Sockets can be used, but select and evaluate them carefully for best results. Use caution when installing the INA116 in a socket. Careless handling can contaminate the plastic near the input pins, dramatically increasing leakage current.

A proven low leakage current assembly method is to bend the input pins outward so they do not contact the circuit board. Input connections are made in air and soldered directly to the input pin. This technique is often not practical or production-worthy. It is, however, a useful technique for evaluation and testing and provides a benchmark with which to compare other wiring techniques. The circuit board guarding techniques discussed normally reduce leakage to acceptable levels.

A solid mechanical assembly is required for good results. Nearby plastic parts can be especially troublesome since a static charge can develop and the slightest motion or vibration will couple charge to the inputs. Place a Faraday shield around the whole amplifier and input connection assembly to eliminate stray fields.

INPUT CONNECTIONS

Some applications must make high impedance input connections to external sensors or input connectors. To assure low leakage, the input should be guarded all the way to the signal source—see Figure 5. Coaxial cable can be used with the shield driven by the guard. A separate connection is required to provide a ground reference at the signal source. Triaxial cable may reduce noise pickup and provides the ground reference at the source. Drive the inner shield at guard potential and ground the outer shield. Two separate guarded lines are required if both the inverting and non-inverting inputs are brought to the source.

The guard drive output current is limited to approximately +2mA/–50µA. For slow input signals the internal guard output can directly drive a cable shield. With fast input signals, however, the guard may not provide sufficient output current to rapidly charge the cable capacitance. An op amp buffer may be required as shown in Figure 6.

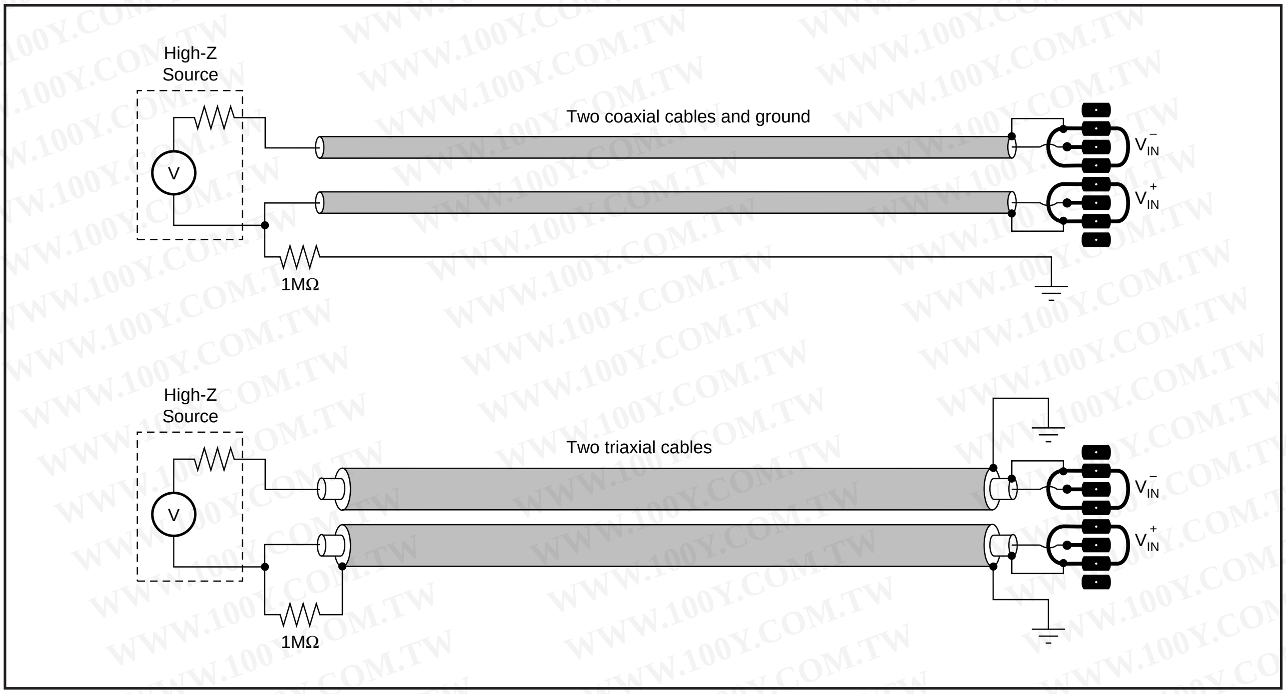


FIGURE 5. Input Cable Guarding Circuits.

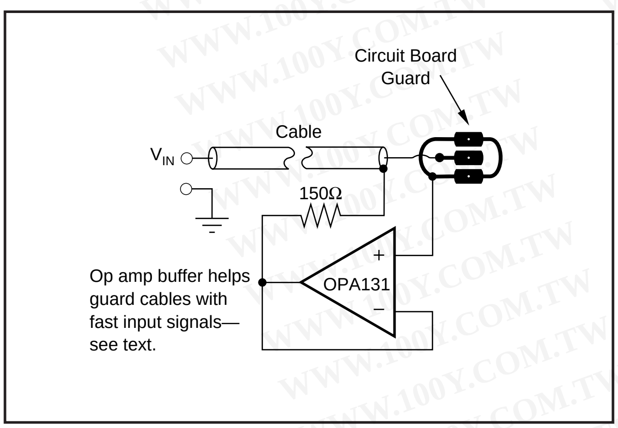


FIGURE 6. Buffered Guard Drive.

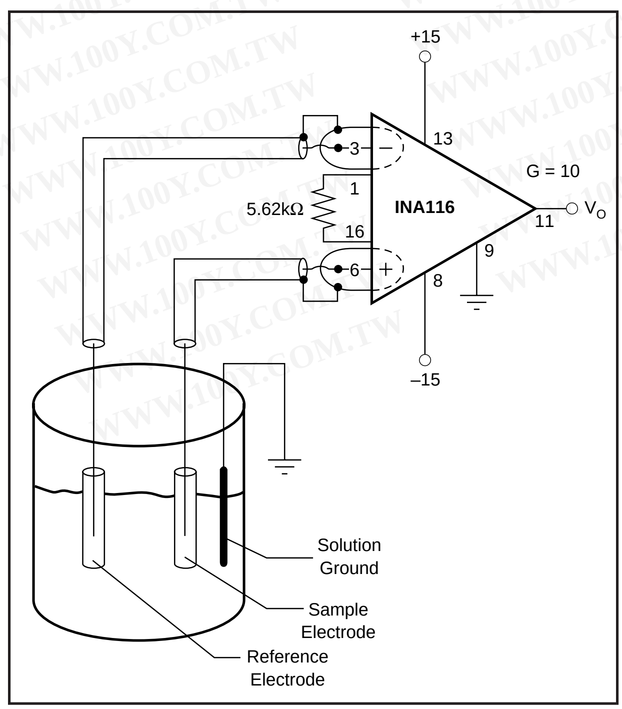


FIGURE 7. pH or Ion Measurement System.