

HN27C4096AG/ACC Series

262144-word × 16-bit CMOS UV Erasable and Programmable
ROM

HITACHI

Description

The Hitachi HN27C4096AG/ACC is a 4-Mbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation. Fabricated on advanced fine process and high speed circuitry technique, the HN27C4096A makes high speed access time possible. Therefore, it is suitable for 16-bit microcomputer systems using high speed microcomputer such as the 80286 and 68020. The HN27C4096A offers high speed programming using page programming mode. This device has the package variation of cerdip-40pin and JLCC-44pin.

Features

- High speed: Access time 100 ns/120 ns/150 ns (max)
- Low power dissipation:
 - Standby mode; 5 μ W (typ)
 - Active mode; 35 mW/MHz (typ)
- Fast high reliability page programming and fast high-reliability programming
 - Programming voltage; +12.5 V D.C.
 - Program time; 3.5 sec (min) (Theoretical in Page programming)
- Inputs and outputs TTL compatible during both read and program modes
- Pin arrangement: 40-pin JEDEC standard
 - 44-pin JLCC JEDEC standard
- Device identifier mode: Manufacturer code and device code
- Fully compatible with the HN27C4096G/CC Series

勝 特 力 材 料 886-3-5753170
勝特力电子(上海) 86-21-54151736
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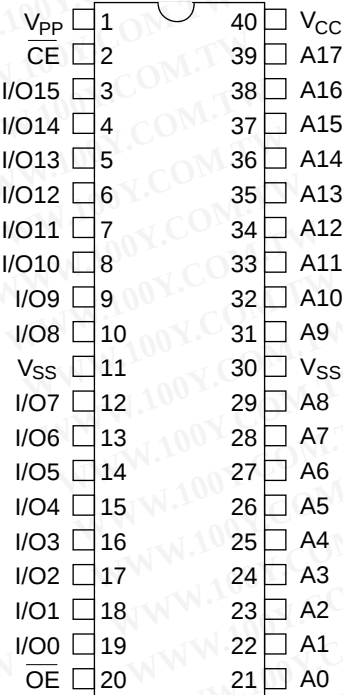
Ordering Information

Type No.	Access Time	Package
HN27C4096AG-10	100 ns	600-mil 40-pin cerdip (DG-40A)
HN27C4096AG-12	120 ns	
HN27C4096AG-15	150 ns	
HN27C4096ACC-10	100 ns	44-pin J-bend leaded chip carrier (CC-44)
HN27C4096ACC-12	120 ns	
HN27C4096ACC-15	150 ns	

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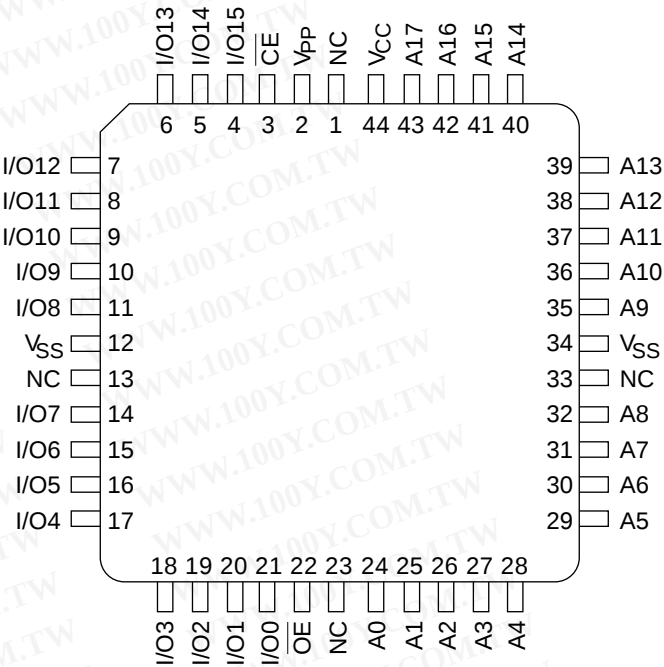
Pin Arrangement

HN27C4096AG Series



(Top view)

HN27C4096ACC Series



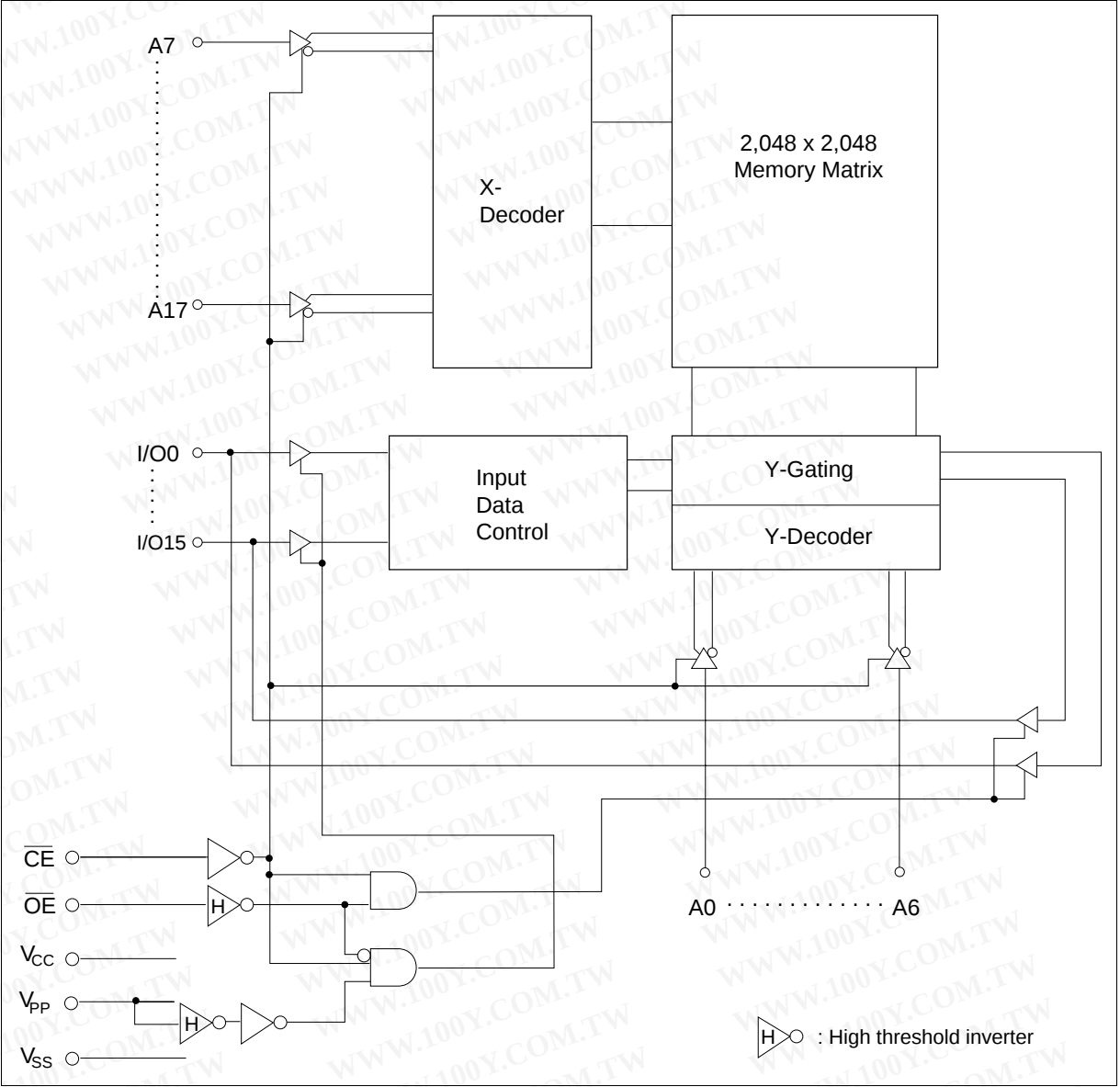
(Top view)

Pin Description

Pin Name	Function
A0 – A17	Address
I/O0 – I/O15	Input/output
CE	Chip enable
OE	Output enable
V _{CC}	Power supply
V _{PP}	Programming power supply
V _{SS}	Ground

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Block Diagram



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Mode Selection

	Pin	$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	V_{CC}	I/O
	CC-44	(3)	(22)	(35)	(2)	(44)	(4 – 11, 14 – 21)
	DG-40A	(2)	(20)	(31)	(1)	(40)	(3 – 10, 12 – 19)
Read		V_{IL}	V_{IL}	X	$V_{SS} - V_{CC}$	V_{CC}	Dout
Output disable		V_{IL}	V_{IH}	X	$V_{SS} - V_{CC}$	V_{CC}	High-Z
Standby		V_{IH}	X	X	$V_{SS} - V_{CC}$	V_{CC}	High-Z
Page program	Page program set	V_{IH}	V_H^{*2}	X	V_{PP}	V_{CC}	High-Z
	Page data latch	V_{IL}	V_H^{*2}	X	V_{PP}	V_{CC}	Din
	Page program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	High-Z
	Page program verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
	Page program reset	V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High-Z
Word program	Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
	Program verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
	Optional verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	Dout
	Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High-Z
Identifier		V_{IL}	V_{IL}	V_H^{*2}	$V_{SS} - V_{CC}$	V_{CC}	Code

Notes: 1. X: Don't care.

2. V_H : 12.0 V $\pm$ 0.5 V

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
All input and output voltages ¹	V_{in}, V_{out}	-0.6 ² to +7.0	V
Voltage on pin A9 and $\overline{OE}$	V_{ID}	-0.6 ² to +13.0	V
V_{PP} voltage ¹	V_{PP}	-0.6 to +13.5	V
V_{CC} voltage ¹	V_{CC}	-0.6 to +7.0	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range ³	T_{stg}	-65 to +125	°C
Storage temperature under bias	T_{bias}	-20 to +80	°C

Notes: 1. Relative to V_{SS} .

2. V_{in}, V_{out}, V_{ID} min = -2.0 V for pulse width $\leq$ 20 ns

3. Storage temperature range of device before programming.

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Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	12	pF	Vin = 0 V
Output capacitance	Cout	—	—	20	pF	Vout = 0 V

Read Operation

DC Characteristics (VCC = 5 V ± 10%, VPP = VSS to VCC, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	ILi	—	—	2	μA	Vin = 5.5 V
Output leakage current	ILo	—	—	2	μA	Vout = 5.5 V/0.45 V
VPP current	IPP1	—	1	20	μA	VPP = 5.5 V
Standby VCC current	ISB1	—	—	1	mA	CE = VIH
	ISB2	—	1	20	μA	CE = VCC ± 0.3 V
Operating VCC current	ICC1	—	—	30	mA	Iout = 0 mA, f = 1 MHz
	ICC2	—	—	100	mA	Iout = 0 mA, f = 10 MHz
Input voltage	VIL	−0.3 ¹	—	0.8	V	
	VIH	2.2	—	VCC+1 ²	V	
Output voltage	VOL	—	—	0.45	V	IOL = 2.1 mA
	VOH	2.4	—	—	V	IOL = −400 μA

Notes: 1. VIL min = −1.0 V for pulse width ≤ 50 ns
VIL min = −2.0 V for pulse width ≤ 20 ns
2. VIH max = VCC + 1.5 V for pulse width ≤ 20 ns
If VIH is over the specified maximum value, read operation cannot be guaranteed.

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AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{SS}$ to V_{CC} , $T_a = 0$ to $+70^{\circ}\text{C}$)

Test Conditions

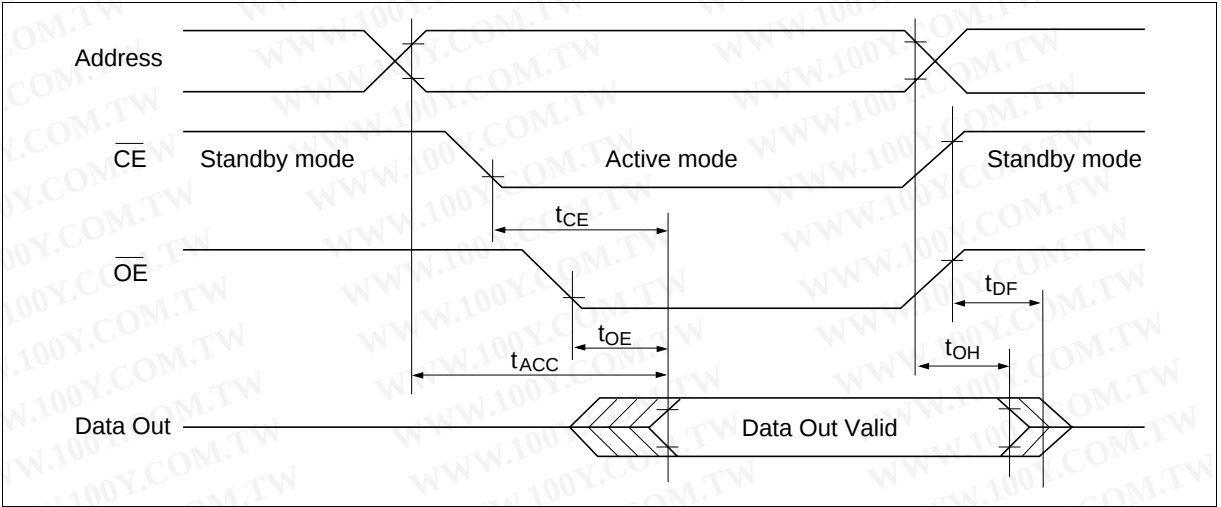
- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time: $\leq 10\text{ ns}$
- Output load: 1 TTL gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

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		HN27C4096A							
		-10		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Address to output delay	t _{ACC}	—	100	—	120	—	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t _{CE}	—	100	—	120	—	150	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t _{OE}	—	60	—	60	—	70	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float*1	t _{DF}	0	35	0	40	0	50	ns	$\overline{CE} = V_{IL}$
Address to output hold	t _{OH}	5	—	5	—	5	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

Page Program Set

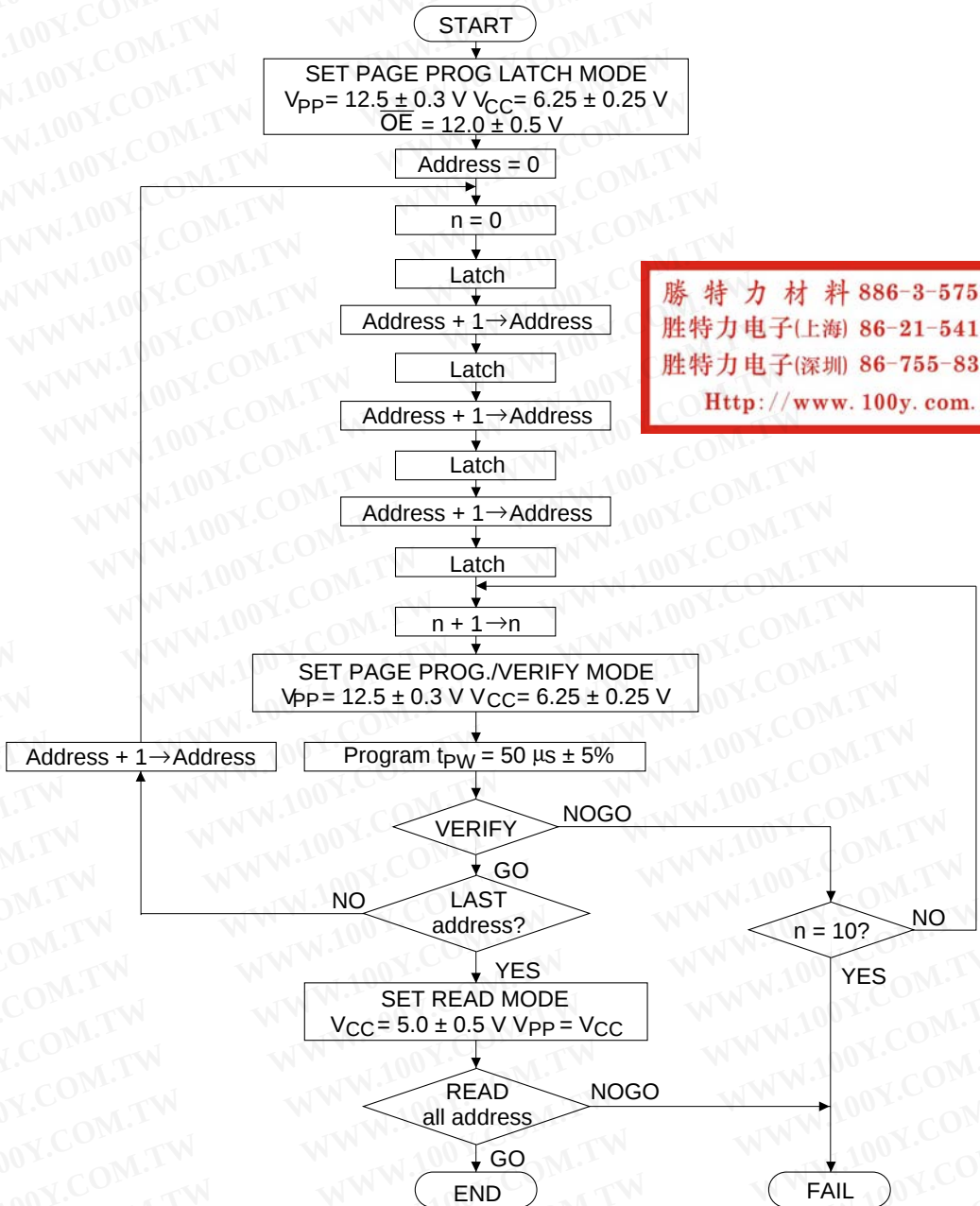
Apply 12 V to $\overline{OE}$ pin after applying 12.5 V to V_{pp} to set a page program mode.

The device operates in a page program mode until reset.

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Page Program Reset

Set V_{PP} to V_{CC} level or less to reset a page program mode.



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Fast High-Reliability Page Programming Flowchart

HN27C4096AG/ACC Series

DC Characteristics ($V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.5\text{ V}/0.45\text{ V}$
Output voltage during verify	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	-0.1^{*5}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}$	V	
	V_H	11.5	12.0	12.5	V	
V_{PP} supply current	I_{PP}	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
- V_{CC} must be applied before V_{PP} and removed after V_{PP} .
 - V_{PP} must not exceed 13 V including overshoot.
 - An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5\text{ V}$.
 - Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 - $V_{IL}\text{ min} = -0.6\text{ V}$ for pulse width $\leq 20\text{ ns}$.
 - If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

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AC Characteristics ($V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time: $\leq 20\text{ ns}$
- Reference levels for measuring timing:
Inputs; 0.8 V, 2.0 V,
Outputs; 0.8 V, 2.0 V

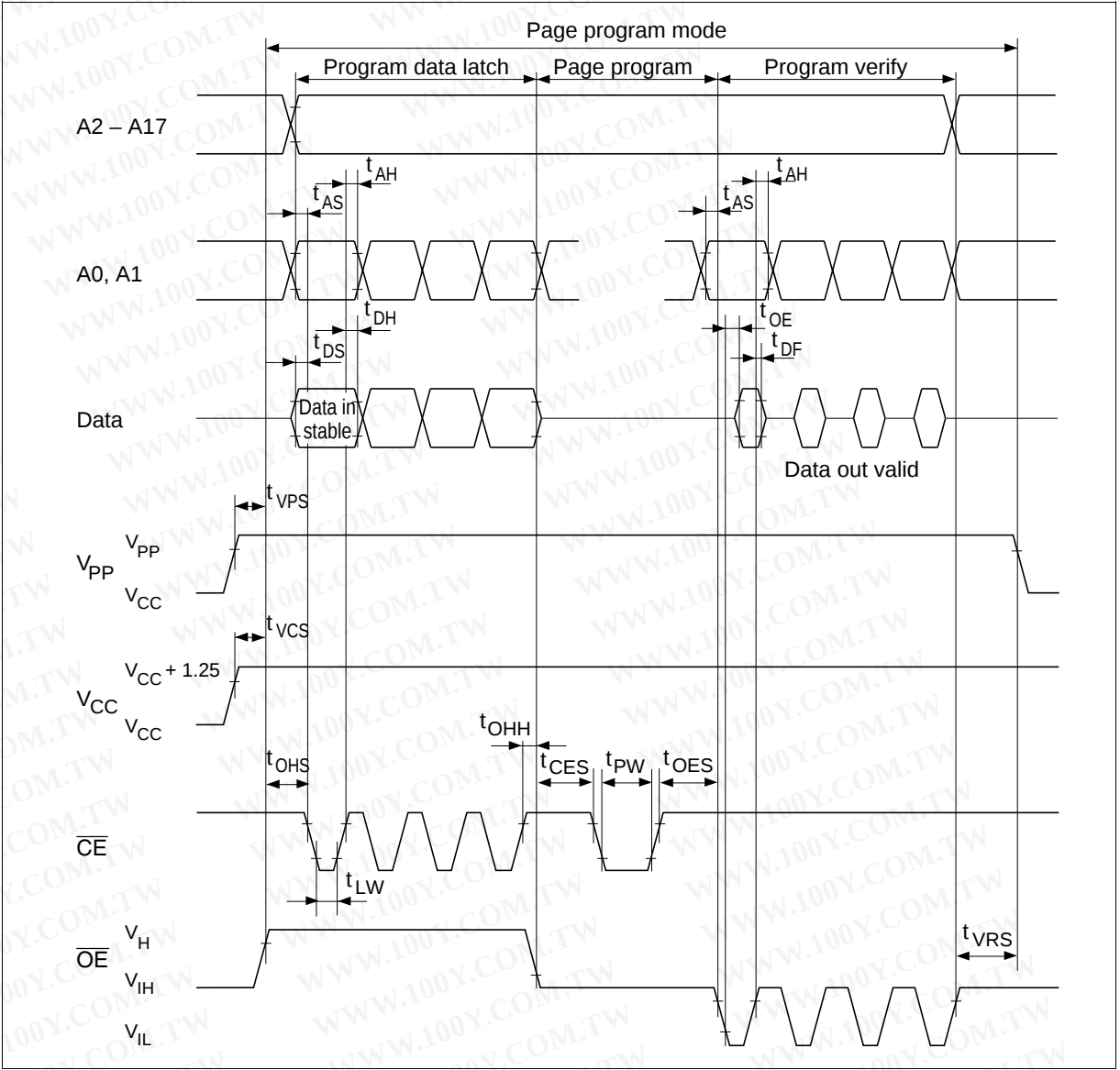
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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	μs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
$\overline{OE}$ high to output float delay	t_{DF}^{*1}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
$\overline{CE}$ programming pulse width	t_{PW}	47.5	50.0	52.5	μs	
$\overline{CE}$ setup time	t_{CES}	2	—	—	μs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	
$\overline{CE}$ pulse width during data latch	t_{LW}	1	—	—	μs	
$\overline{OE} = V_H$ setup time	t_{OHS}	2	—	—	μs	
$\overline{OE} = V_H$ hold time	t_{OHH}	2	—	—	μs	
V_{PP} hold time ^{*2}	t_{VRS}	1	—	—	μs	

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

2. Page program mode will be reset when V_{PP} is set to V_{CC} or less.

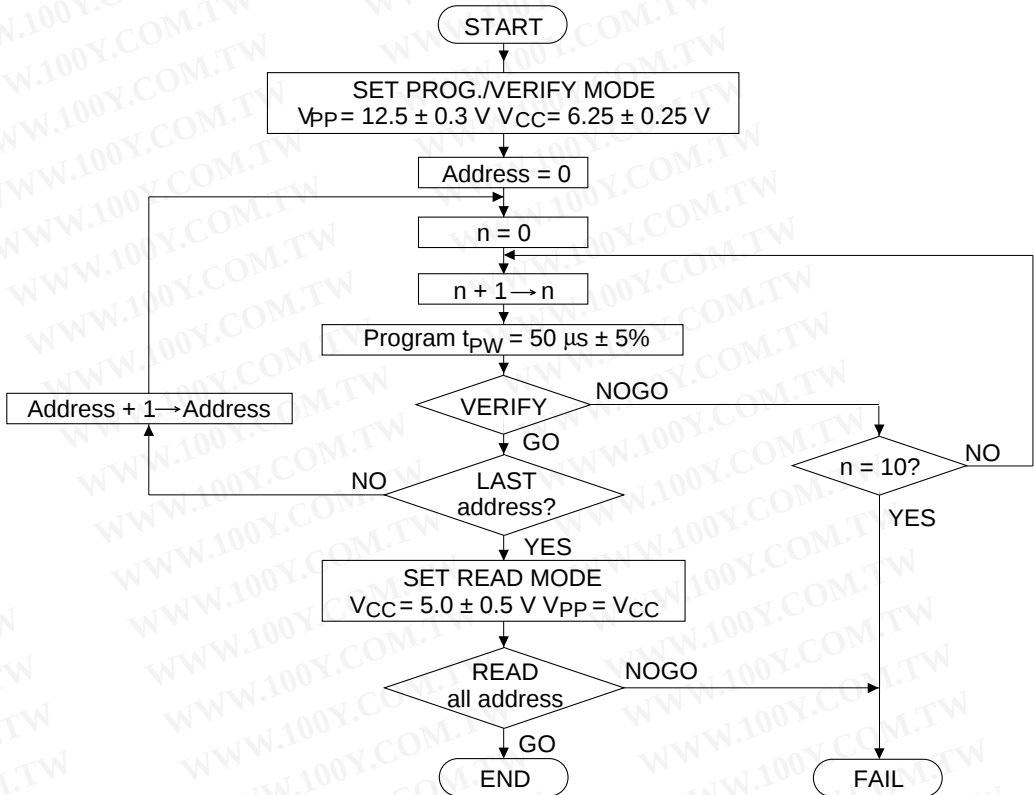
Fast High-Reliability Page Programming Timing Waveform



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Fast High-Reliability Programming

This device can be applied the fast high-reliability programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

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DC Characteristics ($V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.5\text{ V}/0.45\text{ V}$
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE} = V_{IL}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	-0.1^{*5}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}$	V	
Output voltage	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$

- Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .
2. V_{PP} must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5\text{ V}$.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
5. $V_{IL} \text{ min} = -0.6\text{ V}$ for pulse width $\leq 20\text{ ns}$.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

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AC Characteristics ($V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Test Conditions

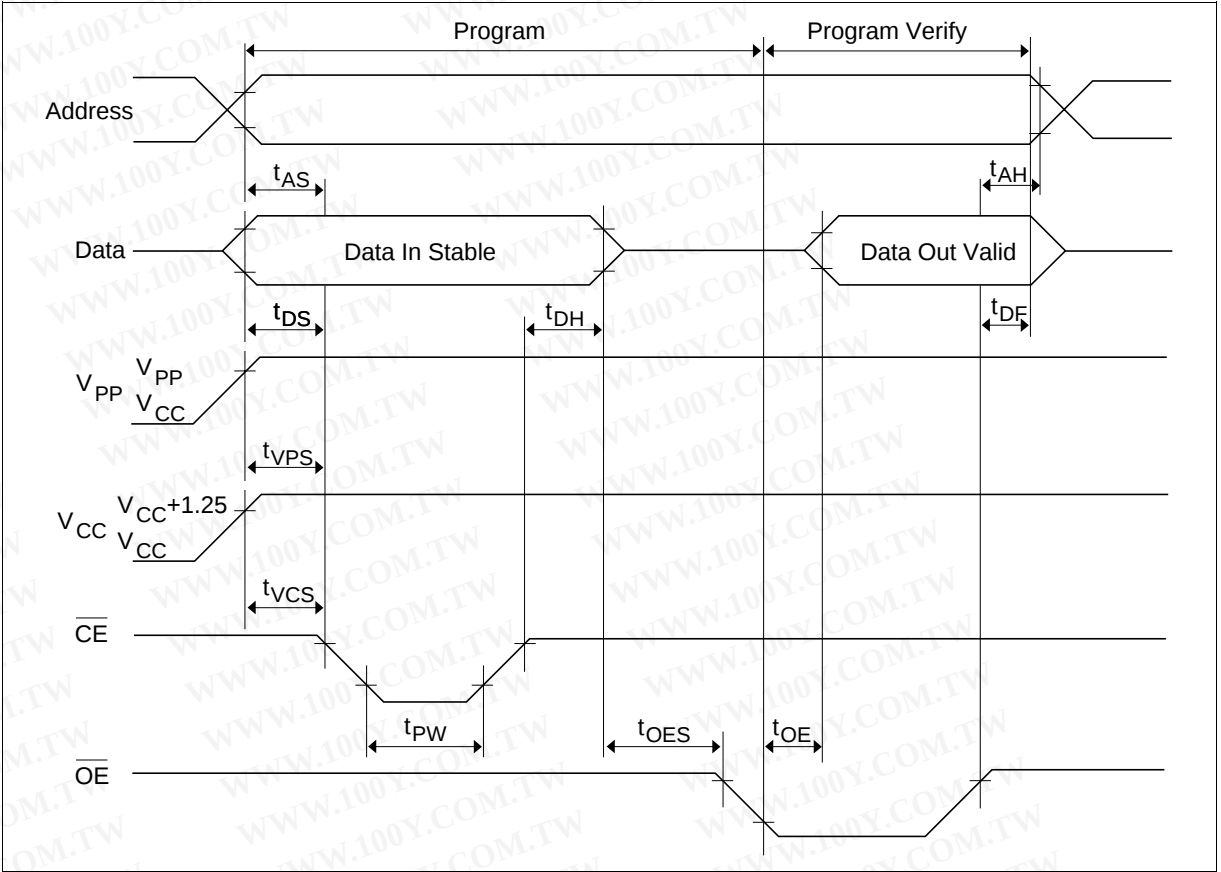
- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time: $\leq 20\text{ ns}$
- Reference levels for measuring timings:
Inputs: 0.8 V, 2.0 V
Outputs: 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	μs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
$\overline{OE}$ to output float delay	t_{DF}^{*1}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
$\overline{CE}$ programming pulse width	t_{PW}	47.5	50.0	52.5	μs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	

Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

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Fast High-Reliability Programming Timing Waveform



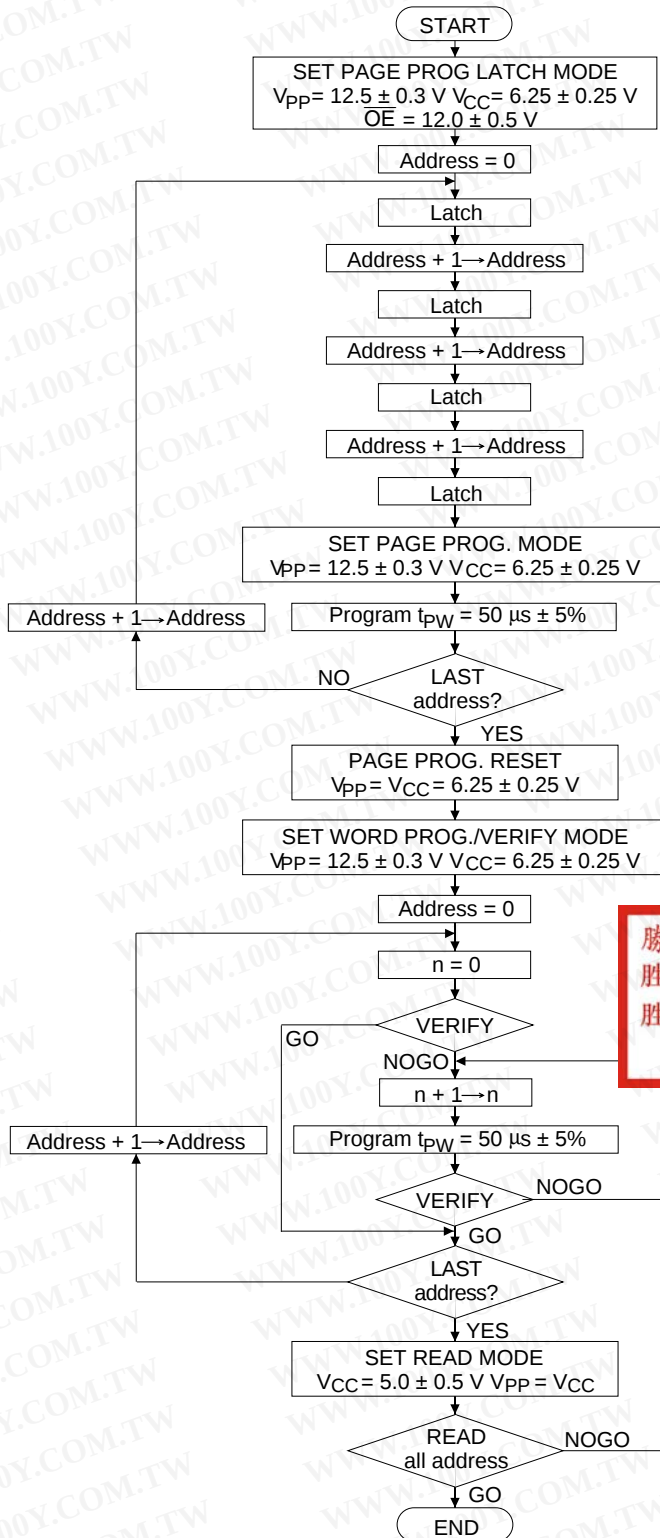
Optional Page Programming

This device can be applied the optional page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

This programming algorithm is the combination of page programming and word verify. It can avoid the increase of programming verify time when a programmer with slow machine cycle is used, and shorten the total programming time.

Regarding the timing specifications for page programming and word verify, please refer to the specifications for fast high-reliability page programming and fast high-reliability programming.

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Optional Page Programming Flowchart

HN27C4096AG/ACC Series

DC Characteristics ($V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.5\text{ V}/0.45\text{ V}$
Output voltage during verify	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	-0.1^{+5}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 0.5^{+6}$	V	
	V_H	11.5	12.0	12.5	V	
V_{PP} supply current	I_{PP}	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
- V_{CC} must be applied before V_{PP} and removed after V_{PP} .
 - V_{PP} must not exceed 13 V including overshoot.
 - An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5\text{ V}$.
 - Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 - V_{IL} min = -0.6 V for pulse width $\leq 20\text{ ns}$.
 - If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

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AC Characteristics ($V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time: $\leq 20\text{ ns}$
- Reference levels for measuring timings:
Inputs; 0.8 V, 2.0 V
Outputs; 0.8 V, 2.0 V

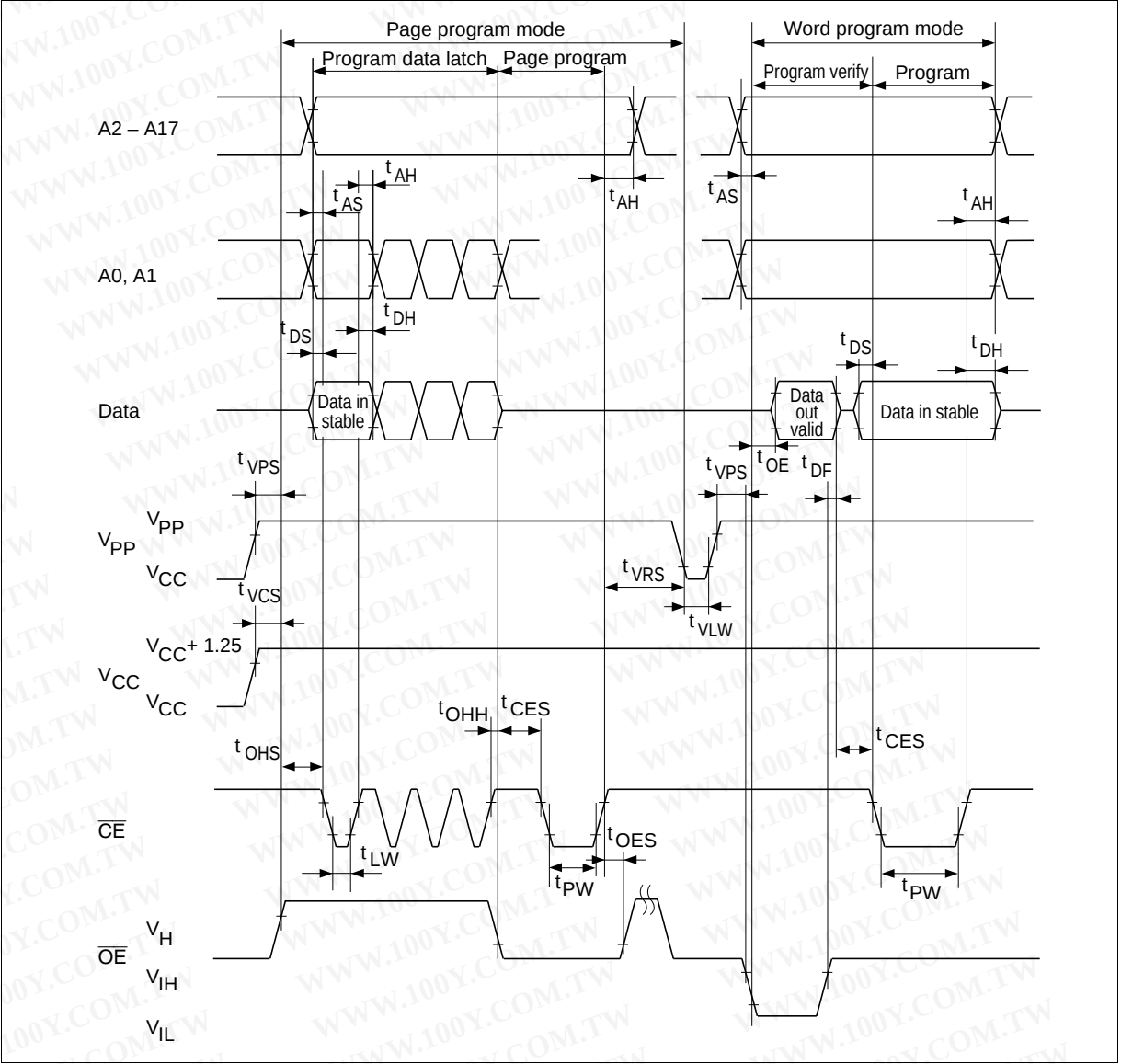
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	μs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
$\overline{OE}$ high to output float delay	t_{DF}^{*1}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
$\overline{CE}$ initial programming pulse width	t_{PW}	47.5	50.0	52.5	μs	
$\overline{CE}$ setup time	t_{CES}	2	—	—	μs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	
$\overline{CE}$ pulse width during data latch	t_{LW}	1	—	—	μs	
$\overline{OE} = V_H$ setup time	t_{OHS}	2	—	—	μs	
$\overline{OE} = V_H$ hold time	t_{OHH}	2	—	—	μs	
Page programming reset time ^{*2}	t_{VLW}	1	—	—	μs	
V_{PP} hold time ^{*2}	t_{VRS}	1	—	—	μs	

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

2. Page program mode will be reset when V_{PP} is set to V_{CC} or less.

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Option Page Programming Timing Waveform



Erase

Erasure of the HN27C4096AG/ACC is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to “1” after this erasure procedure. The minimum integrated dose (i.e. UV intensity X exposure time) for erasure is 15 W · sec/cm².

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Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C4096A Identifier Code

	A0	I/O8 – I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0		
	CC-44	(24)	(11 — 4)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	
Identifier	DG-40A	(21)	(10 — 3)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	Hex Data
Manufacturer code	V _{IL}	X		0	0	0	0	0	1	1	1	07
Device code	V _{IH}	X		1	0	1	0	0	0	1	0	A2

- Notes: 1. $V_{CC} = 5.0\text{ V} \pm 10\%$
2. $A_9 = 12.0\text{ V} \pm 0.5\text{ V}$
3. $A_1 - A_8, A_{10} - A_{17}, \overline{CE}, \overline{OE} = V_{IL}$
4. X: Don't care.

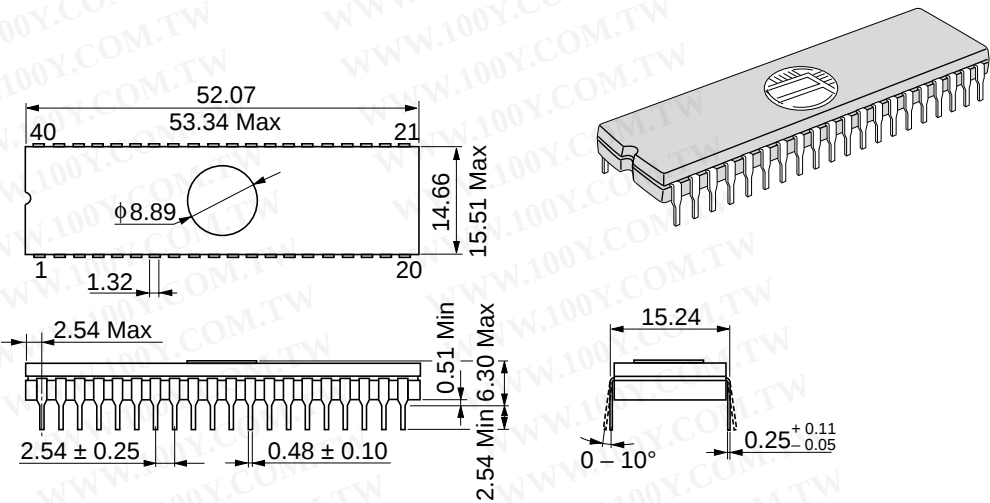
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HN27C4096AG/ACC Series

Package Dimensions

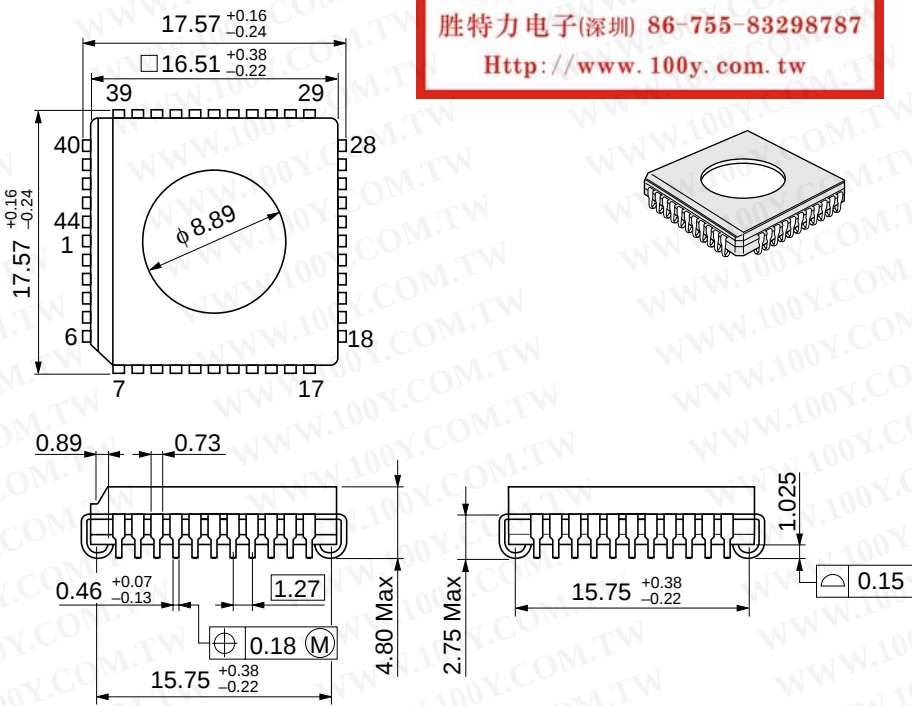
HN27C4096HG Series (DG-40A)

Unit: mm



HN27C4096HCC Series (CC-44)

Unit: mm



HN27C4096A Series

4M (256K x 16-bit) UV and OTP EPROM

■ DESCRIPTION

The Hitachi HN27C4096A is a 4-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 262,144 x 16-bits.

The HN27C4096A features fast address access times of 100, 120 and 150 ns and low power dissipation. This combination makes the HN27C4096A suitable for high speed 16 and 32-bit microcomputer systems. The HN27C4096A offers high speed programming using page programming mode.

Hitachi's HN27C4096A is offered in JEDEC-Standard Word-Wide EPROM pinouts in 40-pin Ceramic DIP and 44-lead Ceramic and Plastic LCC packages. This allows socket replacement with Mask ROMs.

The Ceramic DIP and Ceramic LCC packages are erasable by exposure to Ultraviolet light. The PLCC packaged device is One-Time Programmable and once programmed, can not be rewritten.

■ FEATURES

- Fast Access Times:
100 ns/120 ns/150 ns (max)
- Single Power Supply:
 $V_{CC} = 5 V \pm 10\%$
- Low Power Dissipation:
Active Mode: 35 mW/MHz (typ)
Standby Mode: 5 μ W (max)
- High Speed Page and Word Programming:
Page Programming Time: 3.5 sec (min)
- Programming Power Supply:
 $V_{PP} = 12.5 V \pm 0.3 V$
- Pin Arrangement:
JEDEC Standard Word-Wide EPROM
Mask ROM Compatible
- Packages:
40-pin Ceramic DIP
44-lead Ceramic LCC
44-lead PLCC

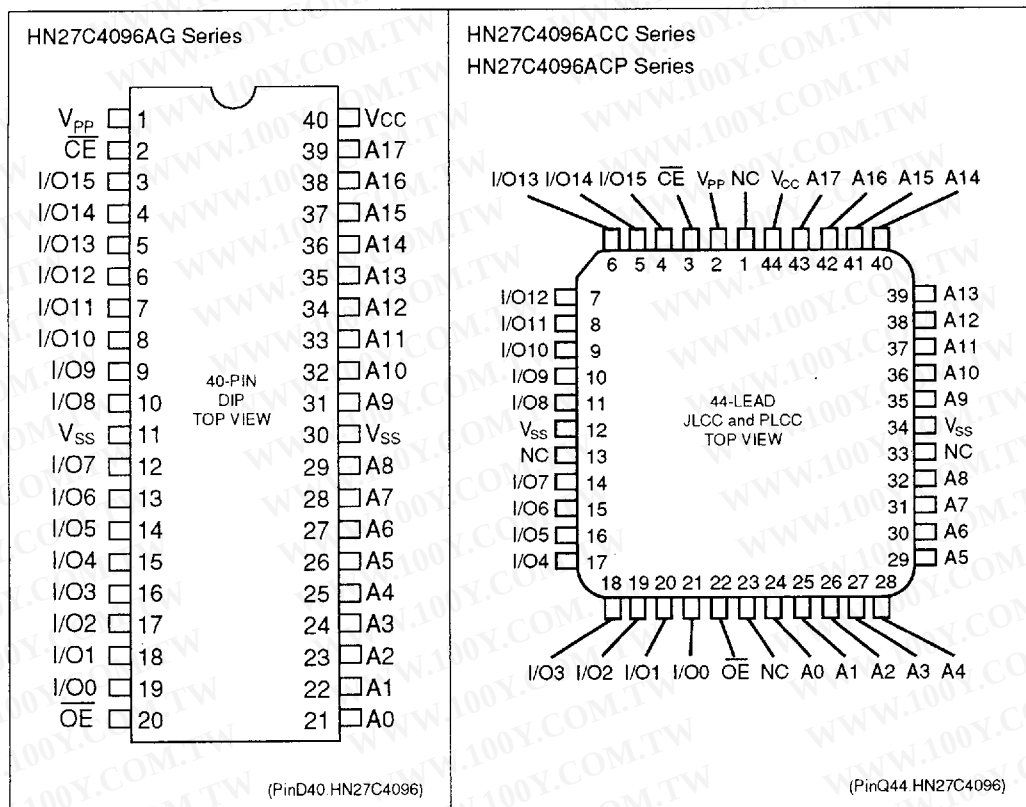
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■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4096AG-10	100 ns	40-pin Ceramic DIP (DG-40A)
HN27C4096AG-12	120 ns	
HN27C4096AG-15	150 ns	
HN27C4096ACC-10	100 ns	44-lead Ceramic LCC (CC-44)
HN27C4096ACC-12	120 ns	
HN27C4096ACC-15	150 ns	
HN27C4096ACP-12	120 ns	44-lead PLCC (CP-44)
HN27C4096ACP-15	150 ns	

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PIN ARRANGEMENT



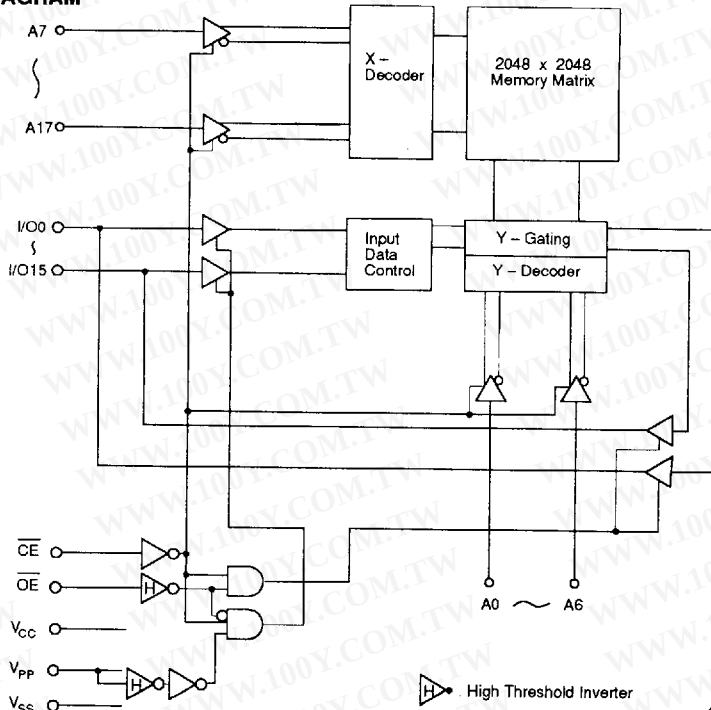
PIN DESCRIPTION

Pin Name	Function
A ₀ - A ₁₇	Address
I/O ₀ - I/O ₁₅	Input/Output
CE	Chip Enable
OE	Output Enable
V _{CC}	Power Supply
V _{PP}	Programming Supply
V _{SS}	Ground
NC	No Connection

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■ BLOCK DIAGRAM



■ MODE SELECTION

Mode	V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	A_9	I/O
Read	$V_{SS}-V_{CC}$	V_{CC}	V_{IL}	V_{IL}	X ¹	D_{OUT}
Output Disable	$V_{SS}-V_{CC}$	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby	$V_{SS}-V_{CC}$	V_{CC}	V_{IH}	X	X	High-Z
Page Prog.	Page Prog. Set	V_{PP}	V_{CC}	V_{IH}	V_H^2	High-Z
	Page Data Latch	V_{PP}	V_{CC}	V_{IL}	V_H	D_{IN}
	Page Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	High-Z
	Page Prog. Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	D_{OUT}
	Page Prog. Reset	V_{CC}	V_{CC}	V_{IH}	V_{IH}	High-Z
Word Prog.	Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	D_{IN}
	Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	D_{OUT}
	Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	D_{OUT}
	Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	High-Z
Identifier	$V_{SS}-V_{CC}$	V_{CC}	V_{IL}	V_{IL}	V_H	ID

- Notes: 1. X = Don't Care. $V_{PP} = 0$ V to V_{CC} .
2. 11.5 V $\leq V_H \leq 12.5$ V

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage ¹	V_{CC}	-0.6 to +7.0	V
Programming Voltage ¹	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage ^{1,2}	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_0 and $\overline{OE}$ Voltage ²	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range ³	T_{STG}	-65 to +125 ⁴ -55 to +125 ⁵	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

- Notes: 1. Relative to V_{SS} .
 2. V_{IN} , V_{OUT} , and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
 3. Device storage temperature range before programming.
 4. HN27C4096AG and HN27C4096ACC.
 5. HN27C4096ACP.

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	12	pF	$V_{IN} = 0\text{V}$
Output Capacitance	C_{OUT}	-	-	20	pF	$V_{OUT} = 0\text{V}$

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($V_{CC} = 5\text{V} \pm 10\%$, $V_{PP} = V_{SS}$ to V_{CC} , $T_a = 0$ to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	μA	$V_{IN} = 5.5\text{V}$
Output Leakage Current	I_{LO}	-	-	2	μA	$V_{OUT} = 5.5\text{V}/0.45\text{V}$
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	$I_{OUT} = 0\text{mA}$, $f = 1\text{MHz}$
	I_{CC2}	-	-	100	mA	$I_{OUT} = 0\text{mA}$, $f = 10\text{MHz}$
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE} = V_{IH}$
	I_{SB2}	-	1	20	μA	$\overline{CE} = V_{CC} \pm 0.3\text{V}$
V_{PP} Current	I_{PP1}	-	1	20	μA	$V_{PP} = 5.5\text{V}$
Input Voltage	V_{IH}	2.2	-	$V_{CC} + 1^2$	V	
	V_{IL}	-0.3 ¹	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -400\mu\text{A}$
	V_{OL}	-	-	0.45	V	$I_{OL} = 2.1\text{mA}$

- Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
 V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
 2. V_{IH} max = $V_{CC} + 1.5\text{V}$ for pulse width ≤ 20 ns.
 If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

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■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($V_{CC} = 5V \pm 10\%$, $V_{PP} = V_{SS}$ to V_{CC} , $T_a = 0$ to $70^\circ C$)

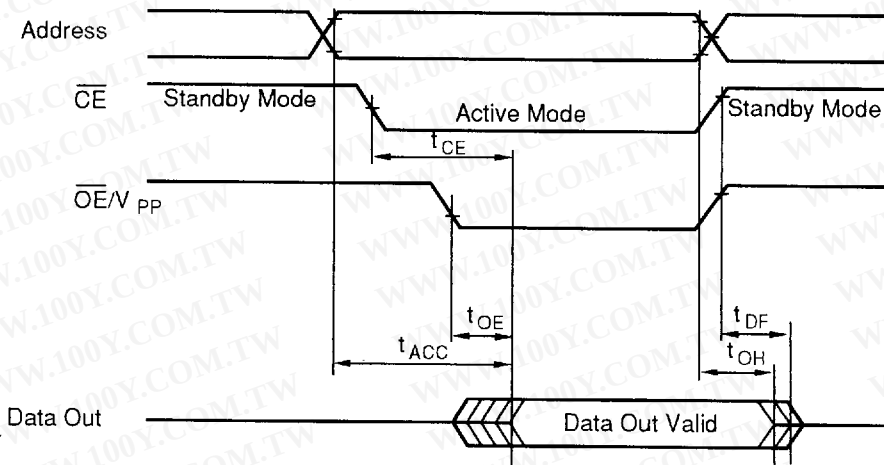
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	HN27C4096A-10		HN27C4096A-12		HN27C4096A-15		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	100	-	120	-	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$
Chip Enable Access Time	t_{CE}	-	100	-	120	-	150	ns	$\overline{OE} = V_{IL}$
Output Enable Access Time	t_{OE}	-	60	-	60	-	70	ns	$\overline{CE} = V_{IL}$
Output Disable to High-Z ¹	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE} = V_{IL}$
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C4096)

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HN27C4096A Series

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	μA	$V_{IN} = 6.5 \text{ V} / 0.45 \text{ V}$
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	-	70	mA	$\overline{CE} = V_{IL}$
Input Voltage ³	V_{IH}	2.2	-	$V_{CC} + .5$	V	
	V_{IL}	-0.1 ⁵	-	0.8	V	
	V_H	11.5	12.0	12.5	V	
Output Voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -400 \mu\text{A}$
	V_{OL}	-	-	0.45	V	$I_{OH} = 2.1 \text{ mA}$

- Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .
 2. V_{PP} must not exceed 13 V, including overshoot.
 3. Device reliability may be adversely affected if the device is installed or removed while $V_{PP} = 12.5 \text{ V}$.
 4. Do not change V_{PP} from V_L to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 5. $V_{IL \text{ min}} = -0.6 \text{ V}$ for pulse width $\leq 20 \text{ ns}$.
 6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.
 7. $I_{PP} = 40 \text{ mA}$ in Word Programming Mode.

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■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: $\leq 20 \text{ ns}$
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	μs	
Address Hold Time	t_{AH}	0	-	-	μs	
Data Setup Time	t_{DS}	2	-	-	μs	
Data Hold Time	t_{DH}	2	-	-	μs	
Chip Enable Setup Time	t_{CES}	2	-	-	μs	
V_{PP} Setup Time	t_{VPS}	2	-	-	μs	
V_{CC} Setup Time	t_{VCS}	2	-	-	μs	
Output Enable Setup Time	t_{OES}	2	-	-	μs	
Output Disable Time	t_{DF}	0	-	130	ns	
Programming Pulse Width	t_{PW}	47.5	50.0	52.5	μs	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Chip Enable Pulse Width During Data Latch	t_{LW}	1	-	-	μs	
Output Enable = V_H Setup Time	t_{OHS}	2	-	-	μs	
Output Enable = V_H Hold Time	t_{OHH}	2	-	-	μs	
Output Enable Hold Time	t_{OEH}	2	-	-	μs	
V_{PP} Hold Time	t_{VRS}	1	-	-	μs	
Page Programming Reset Time	t_{VLW}	1	-	-	μs	

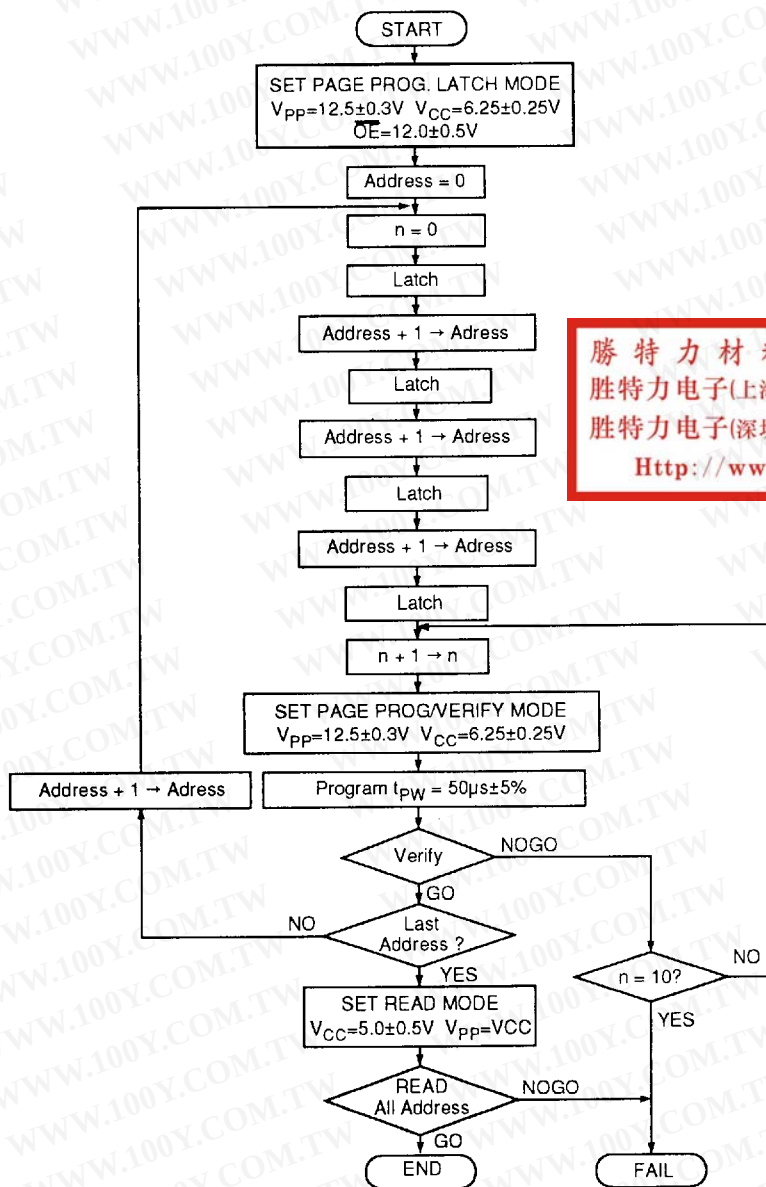
- Note:
1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.
 2. Page Program Mode will be reset when V_{PP} is set to V_{CC} or less.

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PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4096A can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

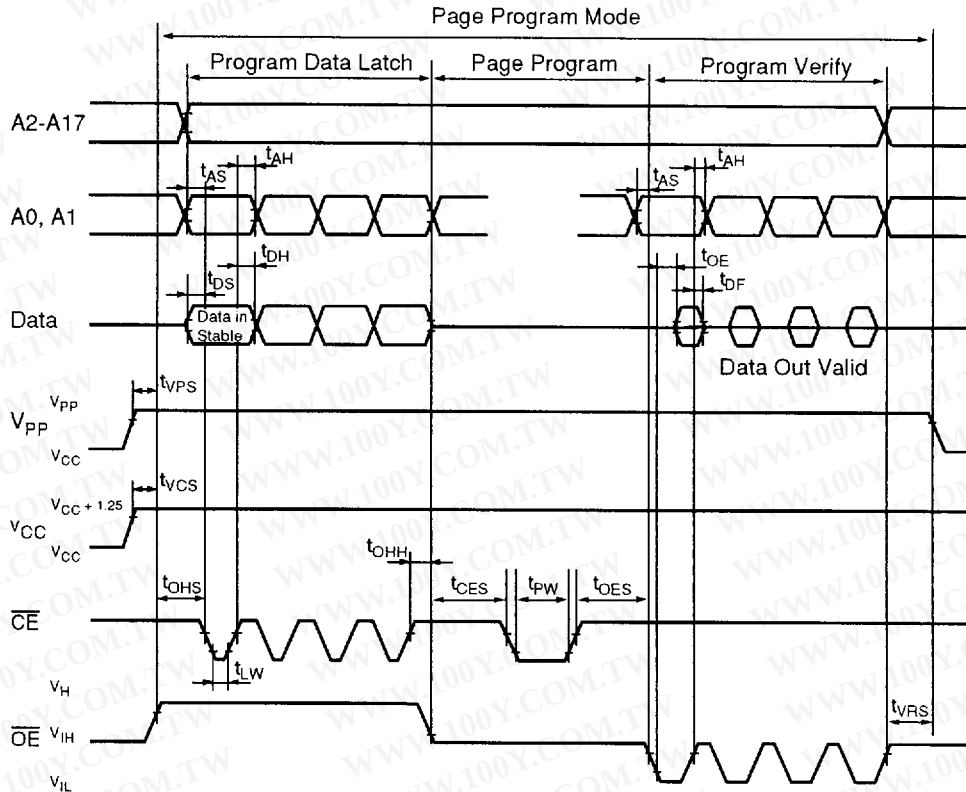
- Note:**
1. To set the device into Page Programming, apply 12.5 V to V_{PP} then followed by applying 12 V to $\overline{OE}$. The device operates in Page Program Mode until reset.
 2. To reset the Page Program Mode, set $V_{PP} = V_{CC}$ or less.



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(FC.PP.HN27C4096)

■ PAGE PROGRAMMING TIMING WAVEFORM



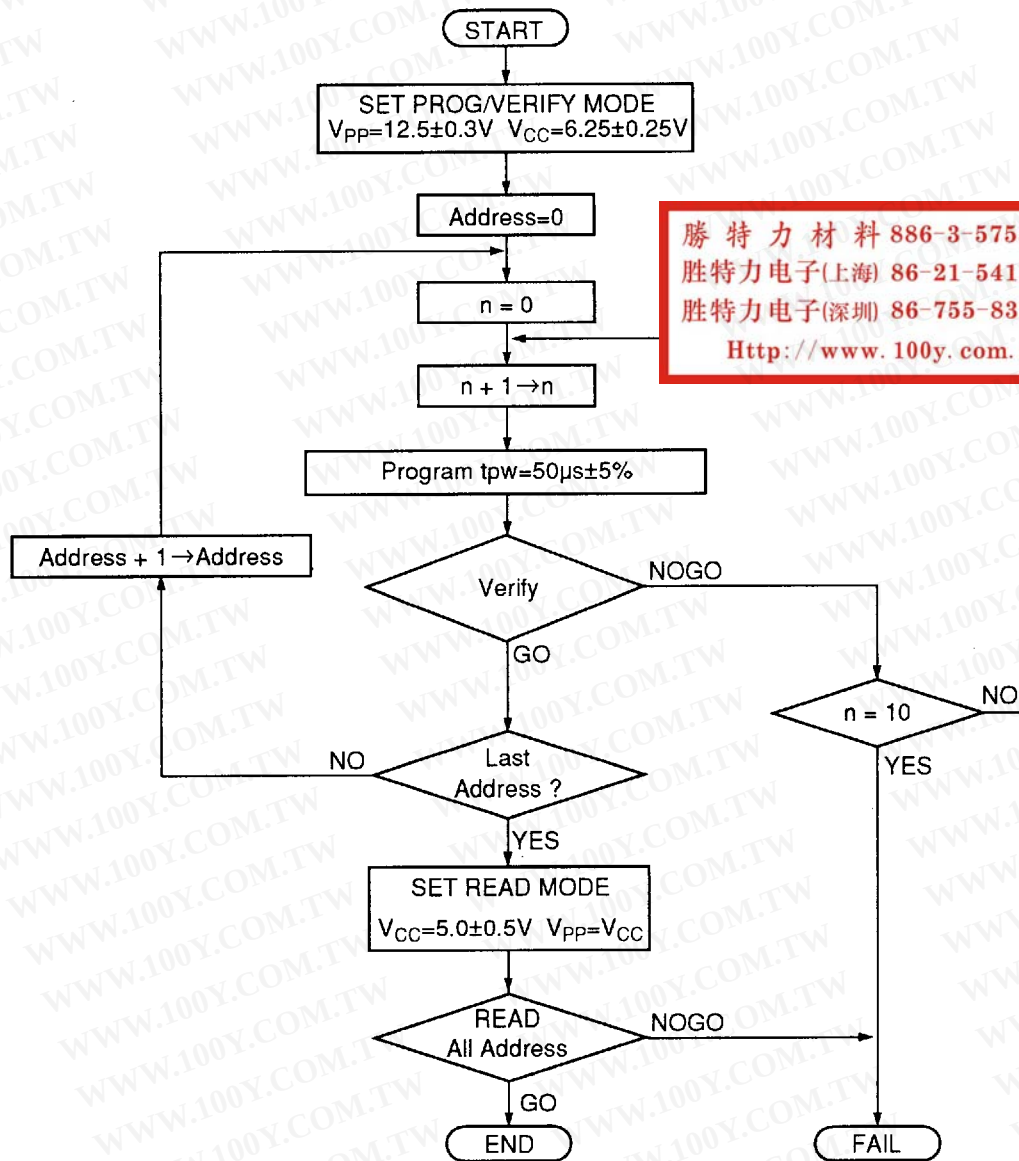
(TD.PP HN27C4096)

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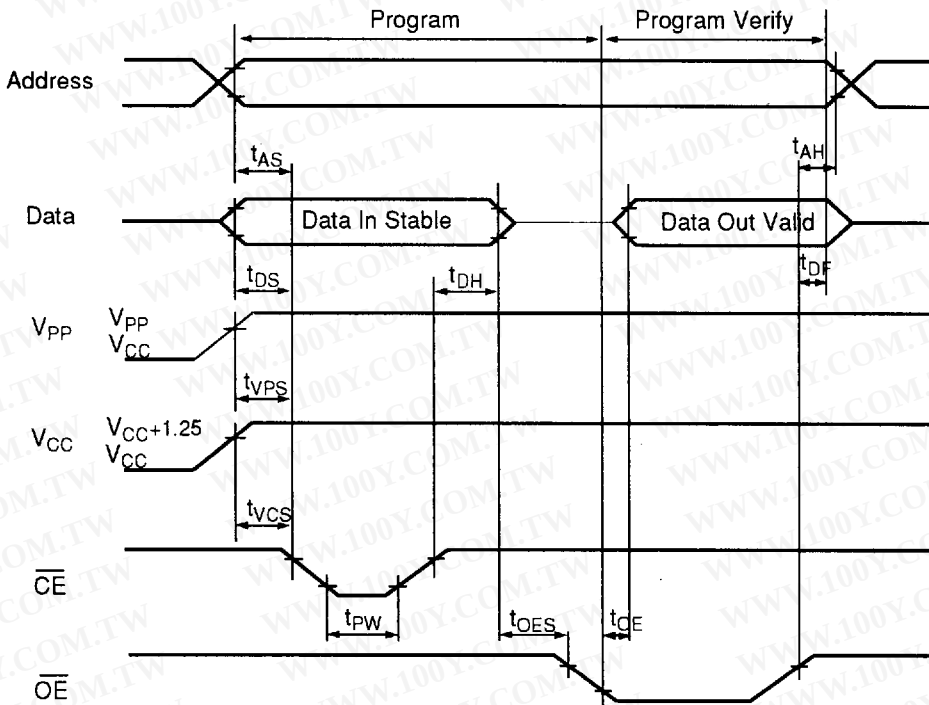
WORD PROGRAMMING FLOWCHART

The Hitachi HN27C4096A can be programmed with the high performance Word Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C4096)

■ WORD PROGRAMMING TIMING WAVEFORM



(TD.P.HN27C4096)

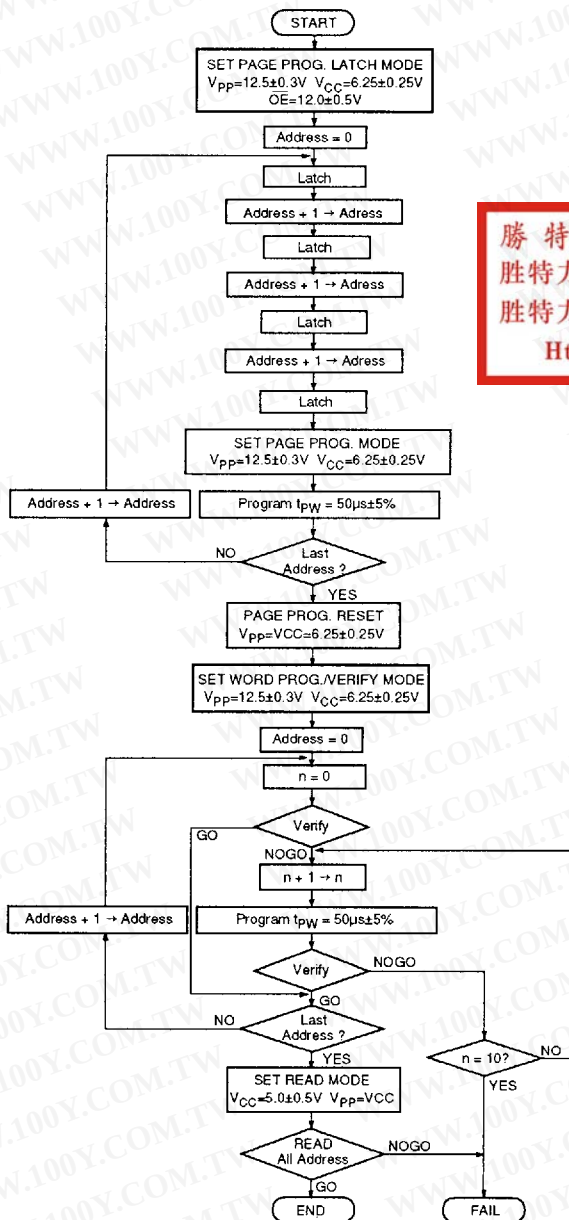
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OPTIONAL PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4096A can be programmed with the high performance Optional Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

This programming algorithm is a combination of Page Programming and Word Verify. It can be used to avoid the increased programming verify time when a programmer with a slower machine cycle is used and shorten the total programming time.

Please refer to the timing specifications for page programming and word programming.

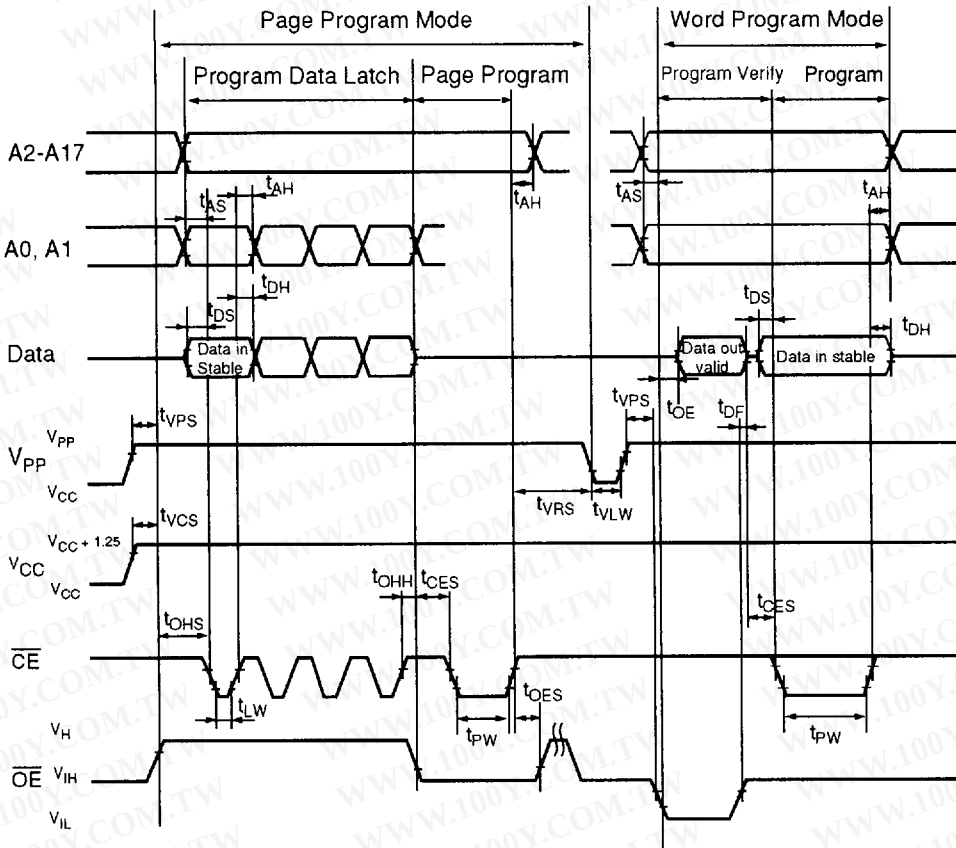


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(FC, OPP, HN27C4096)

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■ OPTIONAL PAGE PROGRAMMING TIMING WAVEFORM



(TD, OPP, HN27C4096)

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HN27C4096A Series

■ ERASING THE HN27C4096A

The Hitachi HN27C4096A Ceramic DIP and Ceramic LCC packages allow these devices to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm².

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

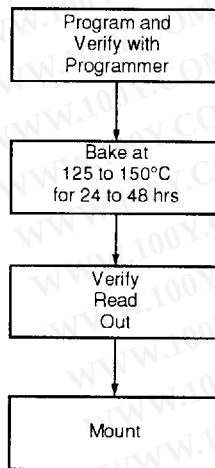
■ HN27C4096A SERIES IDENTIFIER CODE

Identifier	A ₀	I/O ₈ -I/O ₁₅	I/O ₇	I/O ₆	I/O ₅	I/O ₄	I/O ₃	I/O ₂	I/O ₁	I/O ₀	Hex Data
Manufacturer Code	V _{IL}	X	0	0	0	0	0	1	1	1	07
Device Code	V _{IH}	X	1	0	1	0	0	0	1	0	A2

- Notes: 1. V_{CC} = 5.0 V ± 10%
2. A₉ = 12.0 V ± 0.5V
3. A₁-A₈, A₁₀-A₁₇, $\overline{CE}$, $\overline{OE}$ = V_{IL}
4. X = Don't Care

■ HN27C4096ACP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C4096ACP package, please make the following screening (baking without bias) shown below:



(ASC.EPROM)

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