DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4538B
MSI
Dual precision monostable multivibrator

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Dual precision monostable multivibrator

HEF4538B
MSI

DESCRIPTION

The HEF4538B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW trigger/retrigger input ($\overline{I}_0$), an active HIGH trigger/retrigger input (I_1), an overriding active LOW direct reset input ($\overline{C}_D$), an output (O) and its complement ($\overline{O}$), and two pins (C_{TC},(1) RC_{TC}) for connecting the external timing components C_t and R_t. Typical pulse width variation over temperature range is ± 0,2%.

The HEF4538B may be triggered by either the positive or the negative edges of the input pulse and will produce an accurate output pulse with a pulse width range of 10 µs to infinity. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t. The output pulse width (T) is equal to $R_t \times C_t$. The linear design techniques in LOCMOS guarantee precise control of the output pulse width.

A LOW level at $\overline{C}_D$ terminates the output pulse immediately. Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

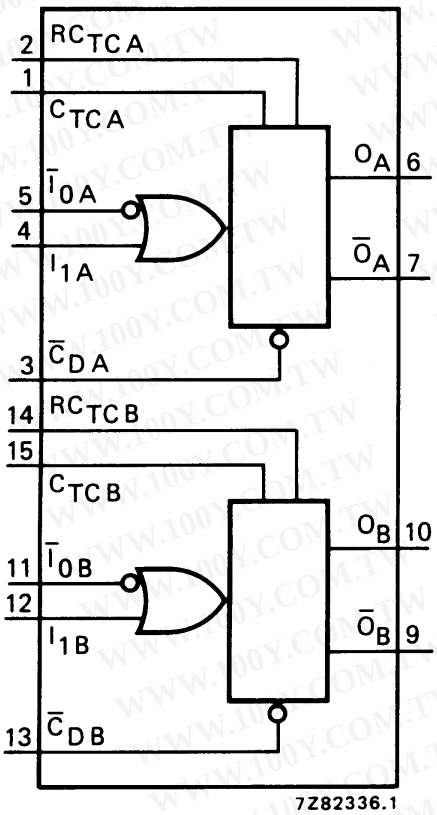


Fig.1 Functional diagram.

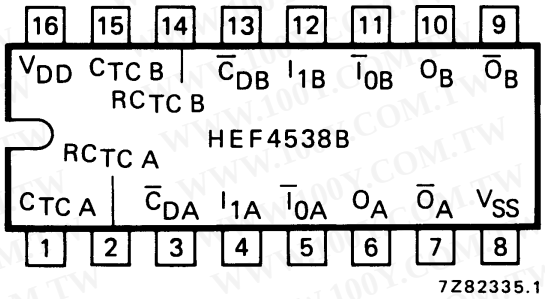


Fig.2 Pinning diagram.

HEF4538BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4538BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4538BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

$\overline{I}_{0A}$, $\overline{I}_{0B}$	input (HIGH to LOW triggered)
I_{1A}, I_{1B}	input (LOW to HIGH triggered)
$\overline{C}_{DA}$, $\overline{C}_{DB}$	direct reset input (active LOW)
O_A, O_B	output
$\overline{O}_A$, $\overline{O}_B$	complementary output (active LOW)
$C_{TC\,A}$, $C_{TC\,B}$	external capacitor connections(1)
$RC_{TC\,A}$, $RC_{TC\,B}$	external capacitor/ resistor connections

Note

1. Always connected to ground.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family specifications.

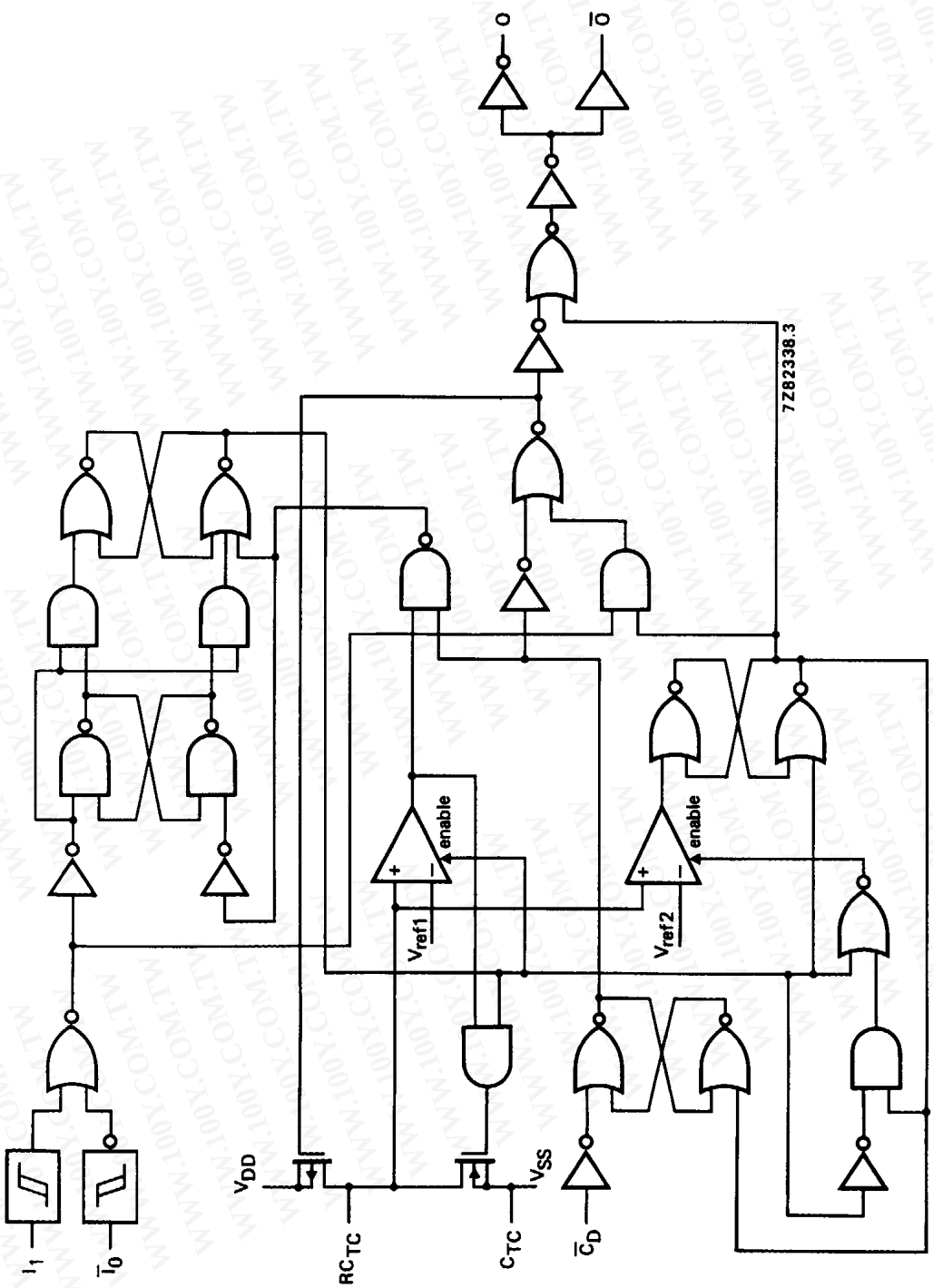


Fig.3 Logic diagram.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{I}_0$	I_1	$\overline{C}_D$	O	$\overline{O}$
↘	L	H	⎍	⎎
H	↗	H	⎍	⎎
X	X	L	L	H

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   ⎍ = positive output pulse
   ⎎ = negative output pulse
   ↗ = positive-going transition
   ↘ = negative-going transition

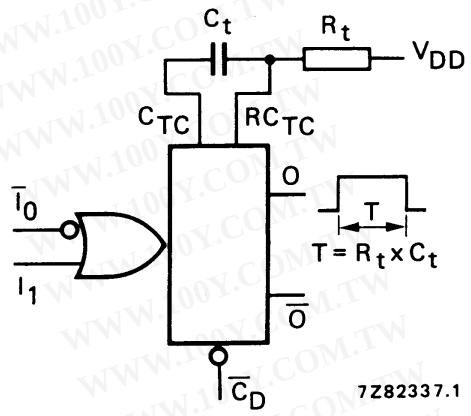


Fig.4 Connection of the external timing components R_t and C_t.

DC CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	SYMBOL	T_{amb} (°C)					
			−40		+25		+85	
			TYP.	MAX.	TYP.	MAX.	TYP.	MAX.
Supply current	5				55			µA
active state	10	I_D			150			µA
(see note)	15				220			µA
Input leakage current (pins 2 and 14)	15	$\pm I_{IN}$			300		1000	nA

Note

1. Only one monostable is switching: current present during output pulse (output O is HIGH).

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$\overline{I}_0$, $I_1 \rightarrow O$	5			200	460	ns	173 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$\overline{I}_0$, $I_1 \rightarrow \overline{O}$	5			220	440	ns	193 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		85	190	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$\overline{C}_D \rightarrow O$	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{C}_D \rightarrow \overline{O}$	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Recovery times	5			20	40	ns	
$\overline{C}_D \rightarrow \overline{I}_0$, I_1	10	t_{RCD}		10	20	ns	
	15			5	10	ns	
Retrigger times	5		0			ns	
O, $\overline{O} \rightarrow \overline{I}_0$, I_1	10	t_{RO}	0			ns	
	15		0			ns	
Minimum $\overline{I}_0$	5		90	45		ns	
pulse width; LOW	10	t_{WI0L}	30	15		ns	
	15		24	12		ns	
Minimum I_1	5		50	25		ns	
pulse width; HIGH	10	t_{WI1H}	24	12		ns	
	15		20	10		ns	
Minimum $\overline{C}_D$	5		55	25		ns	
pulse width; LOW	10	t_{WCDL}	25	12		ns	
	15		20	10		ns	
Output O or $\overline{O}$	5		218	230	242	µs	R_t = 100 kΩ
pulse width	10	t_{WO}	213	224	235	µs	C_t = 0,002 µF
	15		211	223	234	µs	
Output O or $\overline{O}$	5		10,3	10,8	11,3	ms	R_t = 100 kΩ
pulse width	10	t_{WO}	10,2	10,7	11,2	ms	C_t = 0,1 µF
	15		10,1	10,6	11,1	ms	
Output O or $\overline{O}$	5		1,01	1,09	1,11	s	R_t = 100 kΩ
pulse width	10	t_{WO}	0,99	1,04	1,09	s	C_t = 10 µF
	15		0,99	1,04	1,09	s	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
Change in output O pulse width over temperature (T_{amb})	5 10 15	Δt_{WO}		± 0,2 ± 0,2 ± 0,2		% % %	
Change in output O pulse width over V_{DD} range 5 to 15 V		Δt_{WO}		± 1,5		%	
Pulse width variation between circuits in same package	5 10 15	Δt_{WO}		± 1 ± 1 ± 1		% % %	R_t = 100 kΩ C_t = 2 nF to 10 µF
External timing resistor		R_t	5	–	(1)	kΩ	
External timing capacitor		C_t	2000	–	no limits	pF	
Input capacitance (pin 2 or 14)		C_{IN}		15		pF	

Note

1. The maximum permissible resistance R_t , which holds the specified accuracy of t_{WO}, depends on the leakage current of the capacitor C_t and the leakage of the HEF4538B.

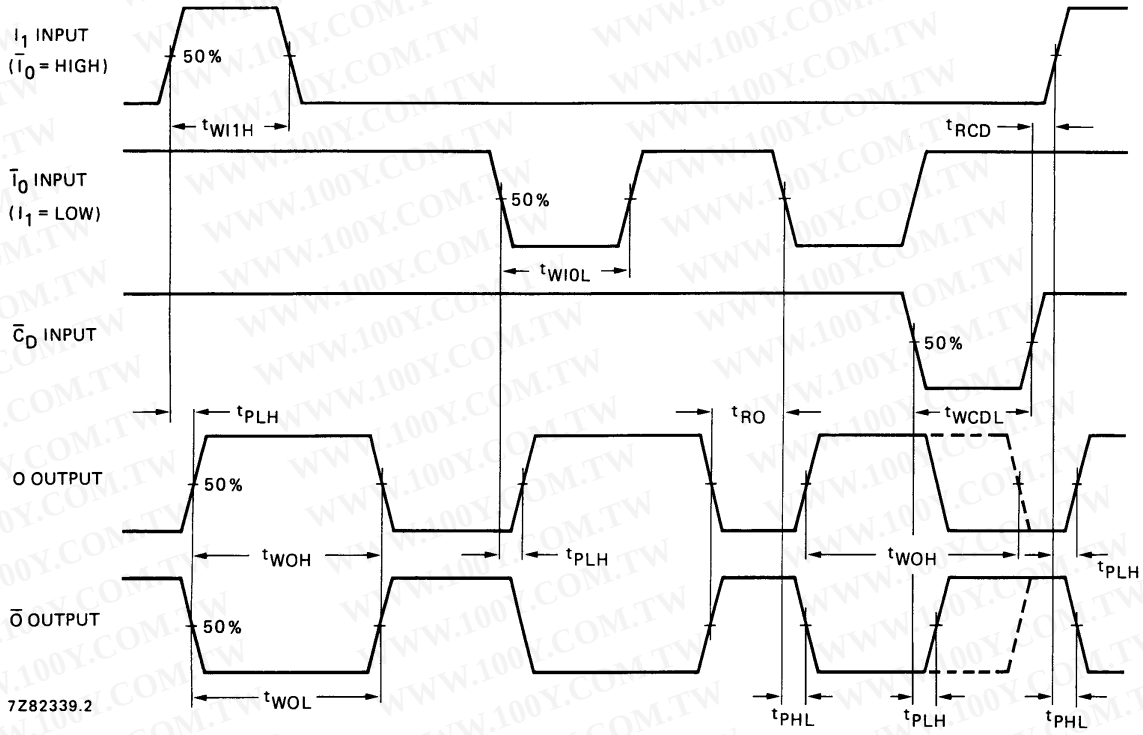
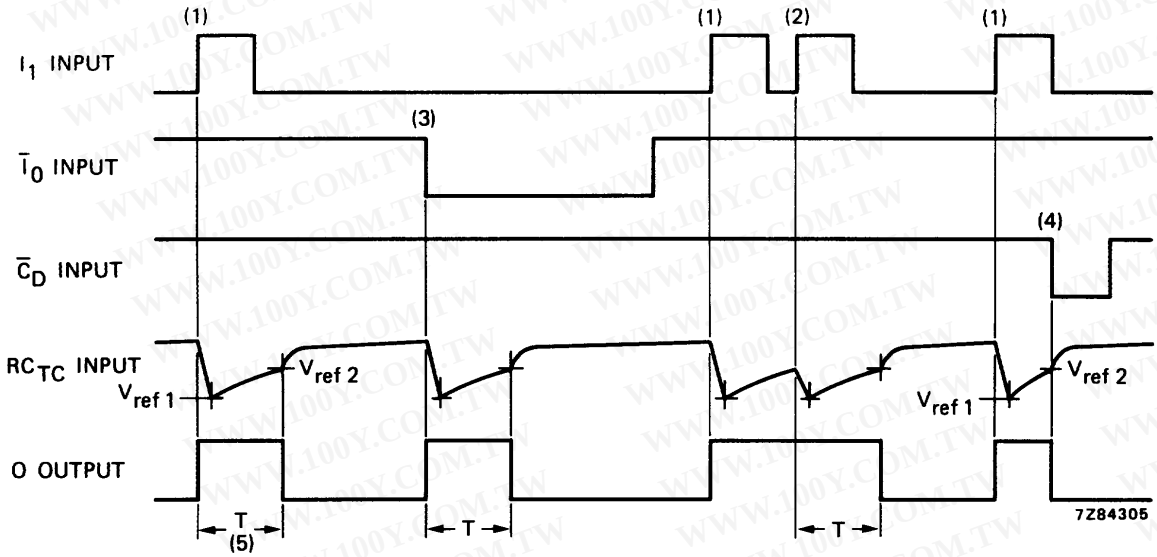
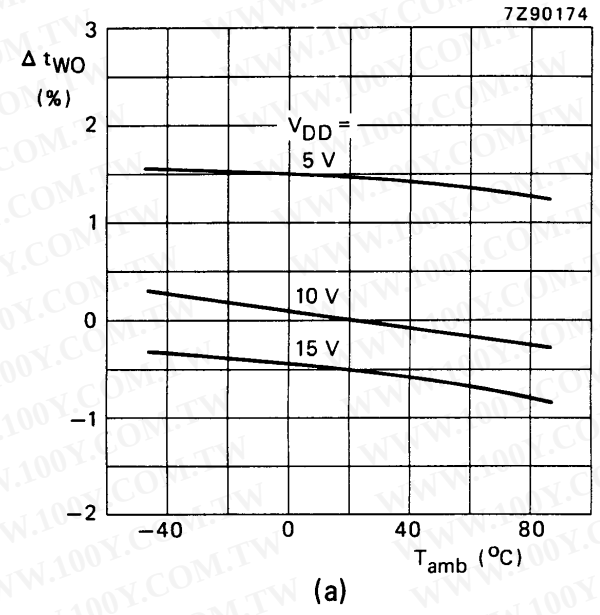


Fig.5 Waveforms showing minimum $\bar{I}_0$, I_1, O and $\overline{C}_D$ pulse widths, recovery times and propagation delays.

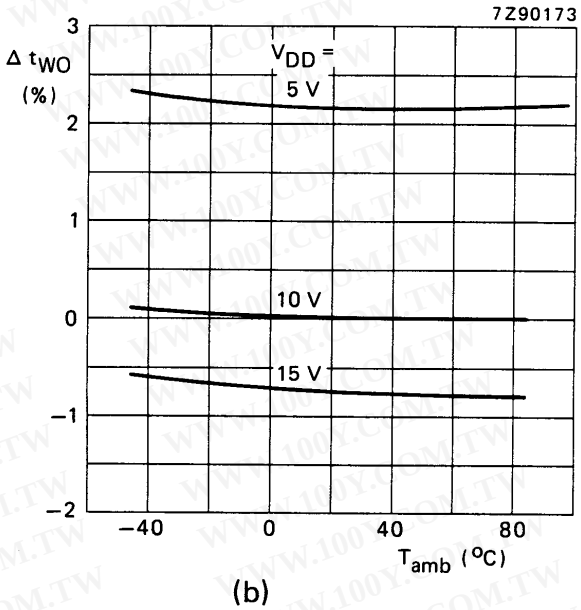


(1) Positive edge triggering.
(2) Positive edge re-triggering (pulse lengthening).
(3) Negative edge triggering.
(4) Reset (pulse shortening).
(5) $T = R_t \times C_t$.

Fig.6 Timing diagram.



(a) R_t = 100 kΩ; C_t = 100 nF..



(b) R_t = 100 kΩ; C_t = 2 nF.

Fig.7 Typical normalized change in output pulse width as a function of ambient temperature; 0% at V_{DD} = 10 V and T_{amb} = 25 °C.

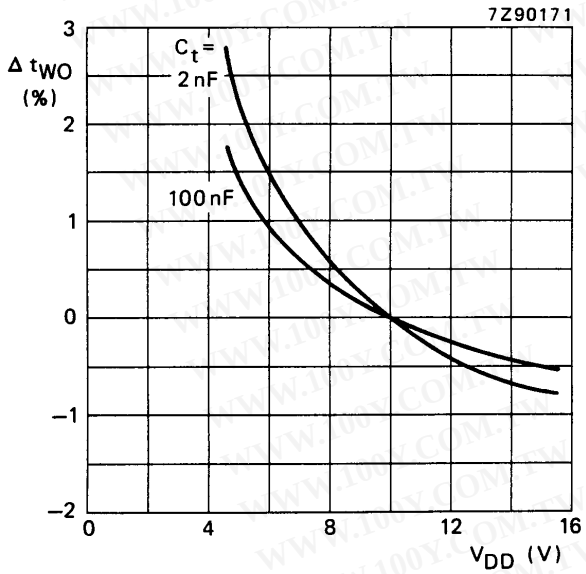


Fig.8 Typical normalized change in output pulse width as a function of the supply voltage at T_{amb} = 25 °C; 0% at V_{DD} = 10 V; R_t = 100 kΩ.

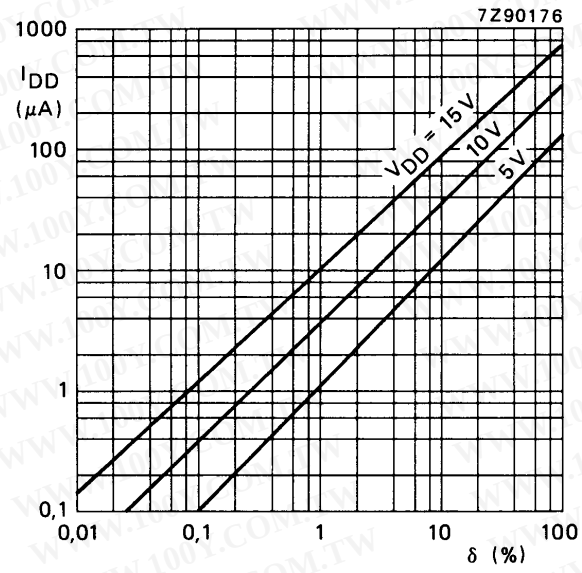


Fig.9 Total supply current as a function of the output duty factor; R_t = 100 kΩ; C_t = 100 nF; C_L = 50 pF. One monostable multivibrator switching only.