

# DATA SHEET

勝特力材料 886-3-5753170  
勝特力电子(上海) 86-21-54151736  
勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4502B buffers Strobed hex inverter/buffer

Product specification  
File under Integrated Circuits, IC04

January 1995

Strobed hex inverter/buffer

HEF4502B  
 buffers

DESCRIPTION

The HEF4502B consists of six inverter/buffers with 3-state outputs. When the output enable input ( $\overline{EO}$ ) is HIGH all six outputs ( $O_1$  to  $O_6$ ) are in the high impedance OFF-state. When the enable input ( $\overline{E}$ ) is HIGH all six outputs are switched to LOW. The outputs have a 2-TTL load drive capability.

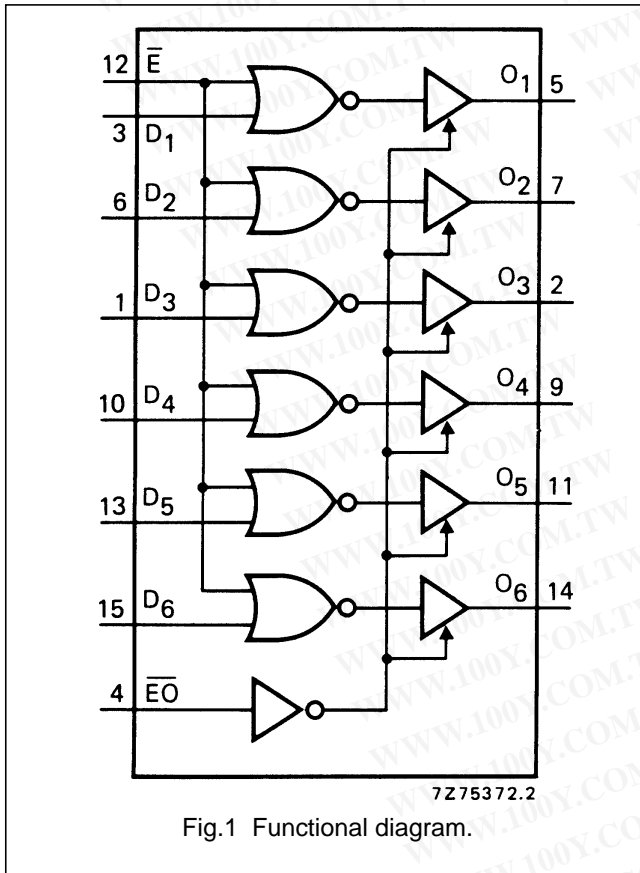


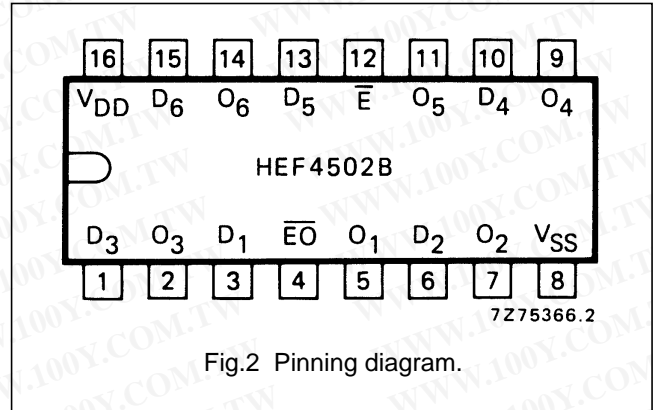
Fig.1 Functional diagram.

TRUTH TABLE

INPUTS			OUTPUT
$D_n$	$\overline{E}$	$\overline{EO}$	$O_n$
L	L	L	H
H	L	L	L
X	H	L	L
X	X	H	Z

Notes

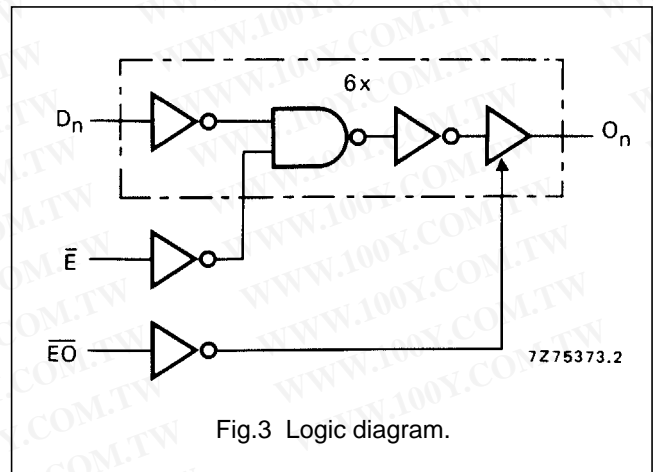
- H = HIGH state (the more pos. voltage)  
 L = LOW state (the less pos. voltage)  
 X = state is immaterial  
 Z = high impedance off state



- HEF4502BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4502BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4502BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

PINNING

- $D_1$  to  $D_6$  data inputs
- $\overline{E}$  enable input
- $\overline{EO}$  output enable input
- $O_1$  to  $O_6$  3-state outputs



FAMILY DATA,  $I_{DD}$  LIMITS category BUFFERS

See Family Specifications

## Strobed hex inverter/buffer

HEF4502B  
buffers

## DC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ 

	$V_{DD}$ V	$V_{OH}$ V	$V_{OL}$ V	SYMBOL	$T_{amb} (\text{°C})$						
					-40		+25		+85		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output current HIGH	5	4,6		$-I_{OH}$	1,2		1,0		0,8		mA
	10	9,5			3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
Output current HIGH	5	2,5		$-I_{OH}$	3,8		3,2		2,5		mA
Output current LOW	4,75		0,4	$I_{OL}$	3,5		2,9		2,3		mA
	10		0,5		12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

## AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$5\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$25\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$85\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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## AC CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $C_L = 50 \text{ pF}$ ; input transition times  $\leq 20 \text{ ns}$ 

	$V_{DD}$ V	SYMBOL	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $D_n, \bar{E} \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	85	170 ns	$77 \text{ ns} + (0,17 \text{ ns/pF}) C_L$	
	10		40	80 ns	$37 \text{ ns} + (0,06 \text{ ns/pF}) C_L$	
	15		35	70 ns	$33 \text{ ns} + (0,04 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$	80	160 ns	$66 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
		10		35	70 ns	$28 \text{ ns} + (0,13 \text{ ns/pF}) C_L$
		15		30	60 ns	$25 \text{ ns} + (0,10 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	25	50 ns	$10 \text{ ns} + (0,30 \text{ ns/pF}) C_L$	
	10		12	24 ns	$7 \text{ ns} + (0,11 \text{ ns/pF}) C_L$	
	15		8	15 ns	$5 \text{ ns} + (0,07 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{TLH}$	30	60 ns	$5 \text{ ns} + (0,50 \text{ ns/pF}) C_L$
		10		15	30 ns	$3 \text{ ns} + (0,24 \text{ ns/pF}) C_L$
		15		12	24 ns	$3 \text{ ns} + (0,18 \text{ ns/pF}) C_L$
3-state propagation delays Output disable times $\bar{E}O \rightarrow O_n$ HIGH	5	$t_{PHZ}$	60	160 ns		
	10		55	140 ns		
	15		55	140 ns		
	LOW	5	$t_{PLZ}$	50	100 ns	
		10		35	70 ns	
		15		30	60 ns	
Output enable times $\bar{E}O \rightarrow O_n$ HIGH	5	$t_{PZH}$	60	120 ns		
	10		35	70 ns		
	15		30	60 ns		
	LOW	5	$t_{PZL}$	55	110 ns	
		10		25	50 ns	
		15		20	40 ns	