

# DATA SHEET

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For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4093B

### gates

### Quadruple 2-input NAND Schmitt trigger

Product specification  
File under Integrated Circuits, IC04

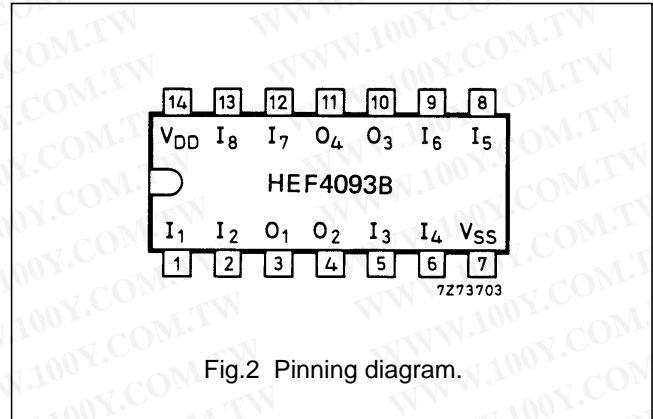
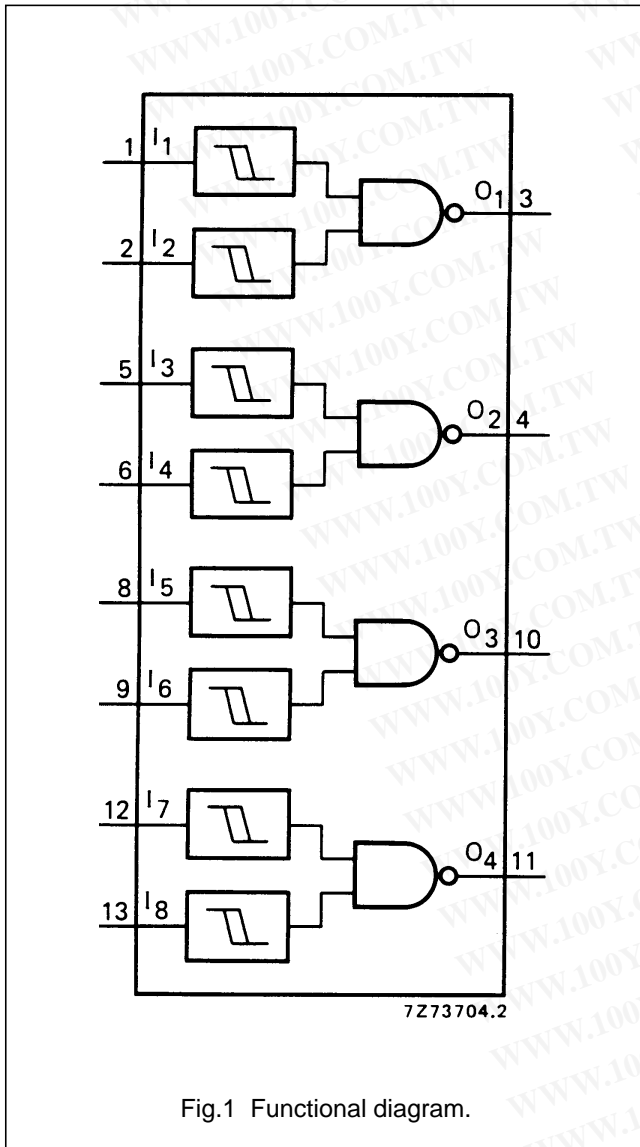
January 1995

Quadruple 2-input NAND Schmitt trigger

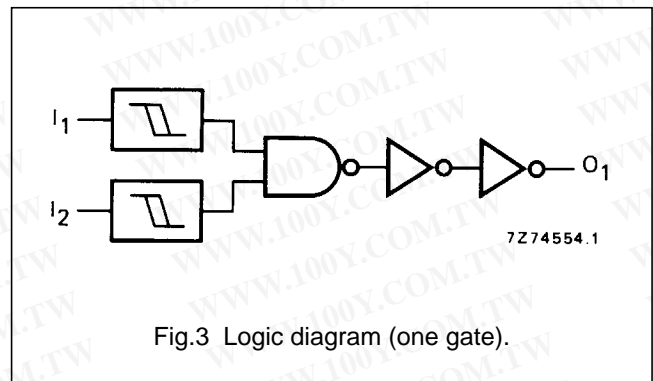
HEF4093B gates

DESCRIPTION

The HEF4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive voltage ( $V_P$ ) and the negative voltage ( $V_N$ ) is defined as hysteresis voltage ( $V_H$ ).



- HEF4093BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4093BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4093BT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America



FAMILY DATA,  $I_{DD}$  LIMITS category GATES

See Family Specifications

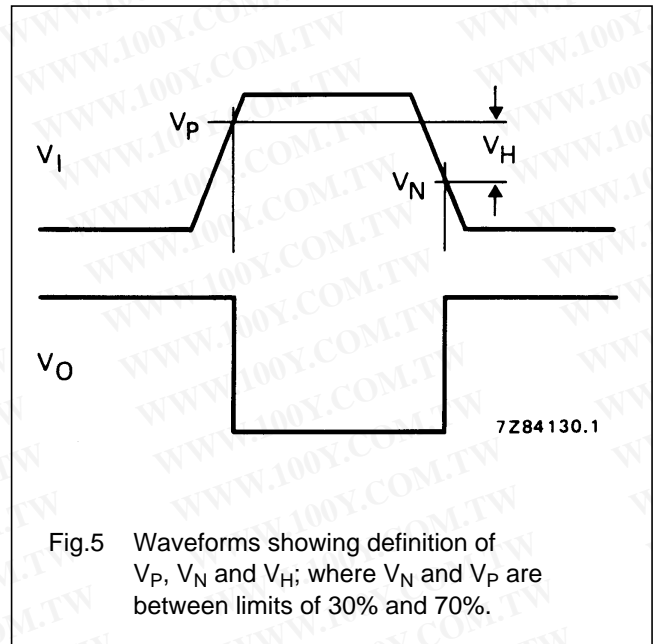
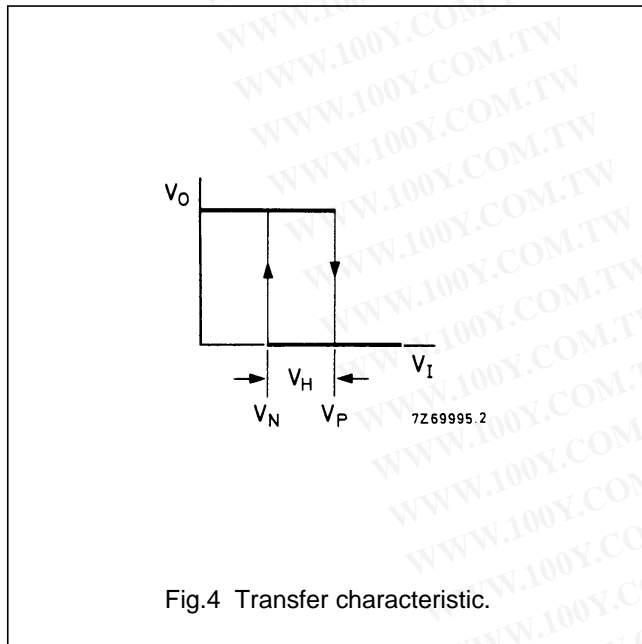
Quadruple 2-input NAND Schmitt trigger

HEF4093B  
gates

DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.		
Hysteresis voltage	5	$V_H$	0,4	0,7	–	V	
	10		0,6	1,0	–	V	
	15		0,7	1,3	–	V	
Switching levels	5	$V_P$	1,9	2,9	3,5	V	
	10		3,6	5,2	7	V	
	15		4,7	7,3	11	V	
	negative-going input voltage	5	$V_N$	1,5	2,2	3,1	V
		10		3	4,2	6,4	V
		15		4	6,0	10,3	V



Quadruple 2-input NAND Schmitt trigger

HEF4093B  
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AC CHARACTERISTICS

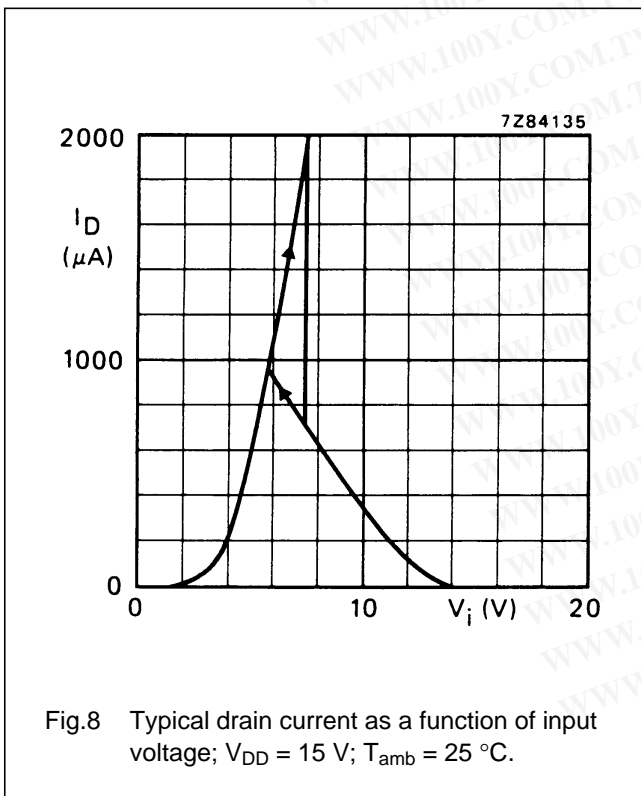
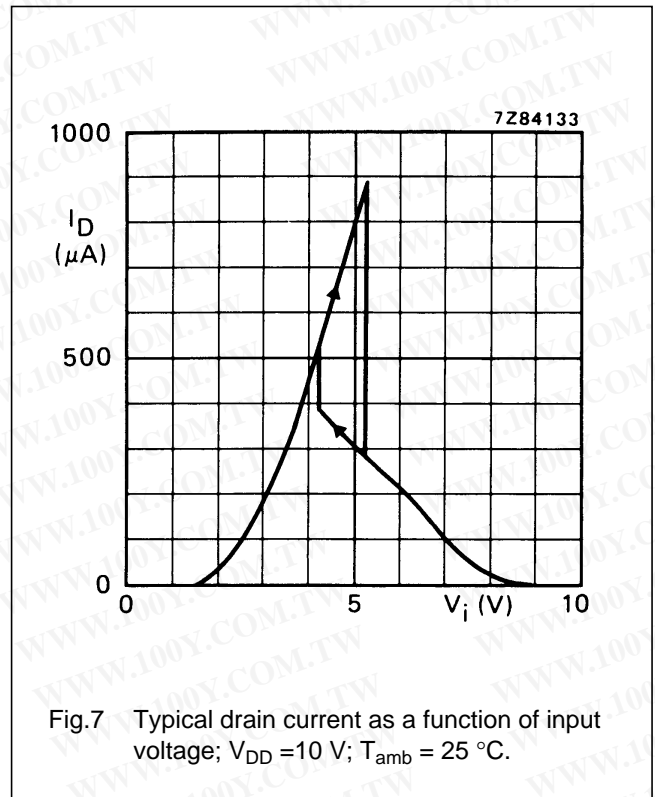
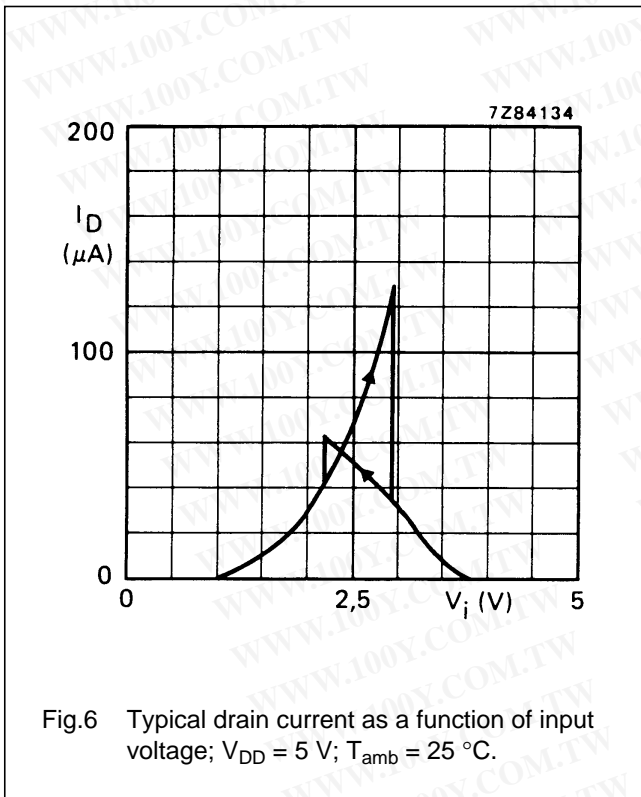
$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	SYMBOL	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	90	185 ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		40	80 ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60 ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$	85	170 ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		40	80 ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		30	60 ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{TLH}$	60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
		15		20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$1300 f_i + \sum(f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum(f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$6400 f_i + \sum(f_o C_L) \times V_{DD}^2$	
	15	$18\ 700 f_i + \sum(f_o C_L) \times V_{DD}^2$	

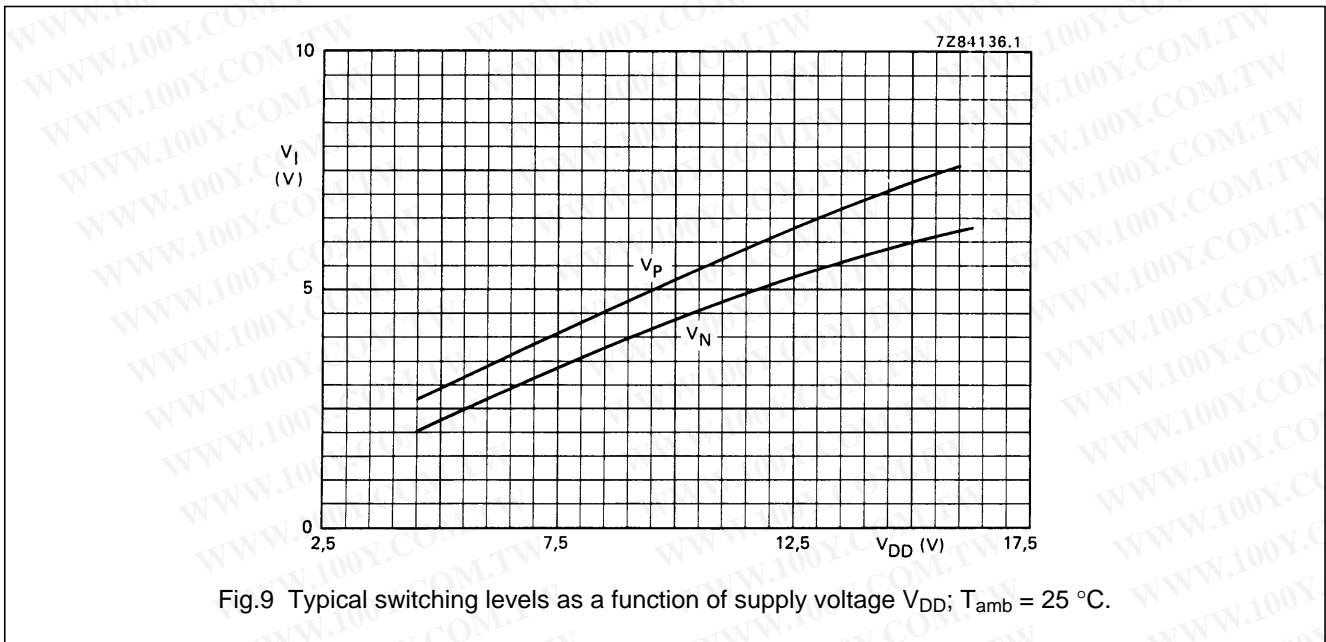
Quadruple 2-input NAND Schmitt trigger

HEF4093B gates



Quadruple 2-input NAND Schmitt trigger

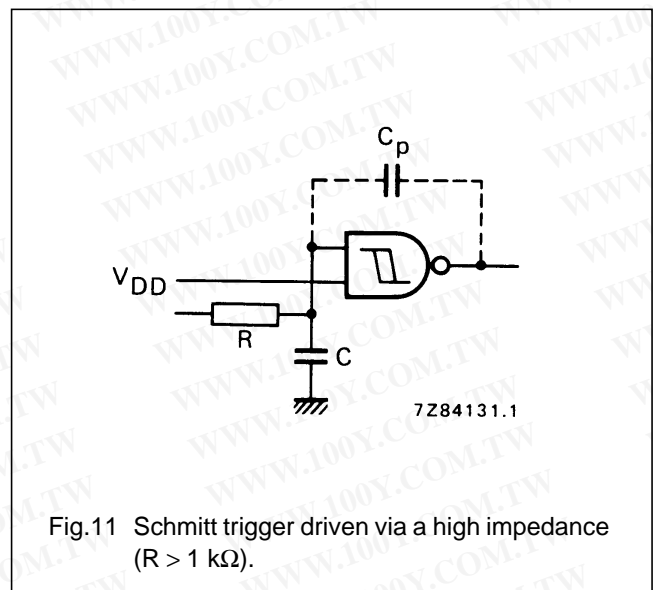
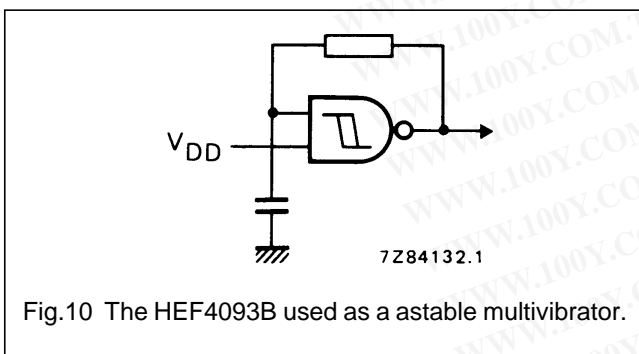
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APPLICATION INFORMATION

Some examples of applications for the HEF4093B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.



If a Schmitt trigger is driven via a high impedance ( $R > 1\text{ k}\Omega$ ) then it is necessary to incorporate a capacitor C of such value that:

$$\frac{C}{C_p} > \frac{V_{DD} - V_{SS}}{V_H}, \text{ otherwise oscillation can occur on the edges of a pulse.}$$

$C_p$  is the external parasitic capacitance between inputs and output; the value depends on the circuit board layout.

Note

The two inputs may be connected together, but this will result in a larger through-current at the moment of switching.