DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4040B
MSI
12-stage binary counter

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

12-stage binary counter

HEF4040B
MSI

DESCRIPTION

The HEF4040B is a 12-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0 to O_{11}). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of $\overline{CP}$. Each counter stage is a static toggle flip-flop. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

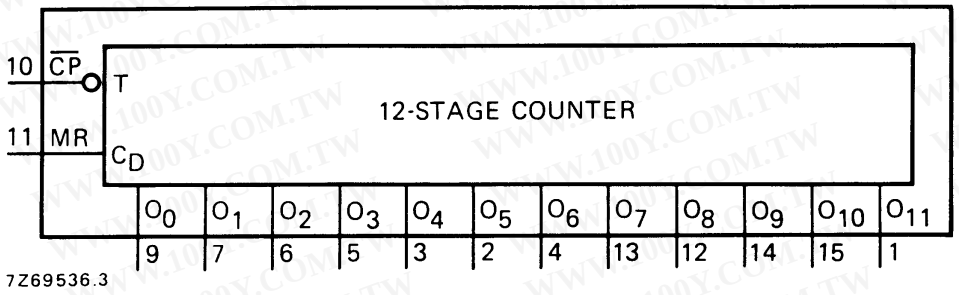

Fig.1 Functional diagram.

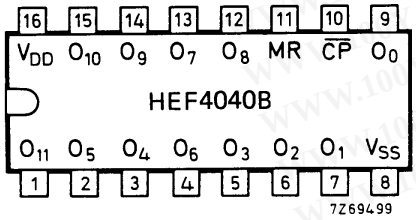

Fig.2 Pinning diagram.

PINNING

$\overline{CP}$	clock input (HIGH to LOW edge-triggered)
MR	master reset input (active HIGH)
O_0 to O_{11}	parallel outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4040B are:

- Frequency dividing circuits
- Time delay circuits
- Control counters

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

HEF4040BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4040BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4040BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

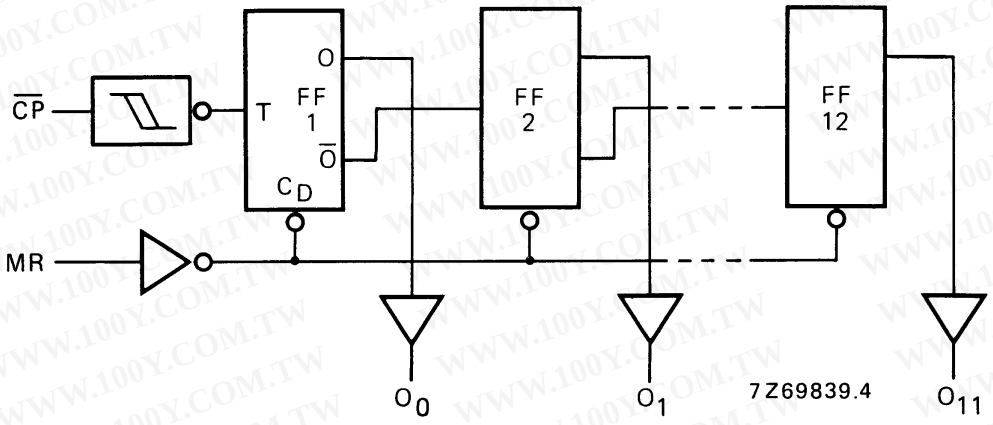

Fig.3 Logic diagram.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$\overline{CP} \rightarrow O_0$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$O_n \rightarrow O_{n+1}$	5			35	70	ns	note 1 (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		15	30	ns	note 1 (0,23 ns/pF) C_L
	15			10	20	ns	note 1 (0,16 ns/pF) C_L
	5			35	70	ns	note 1 (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		15	30	ns	note 1 (0,23 ns/pF) C_L
	15			10	20	ns	note 1 (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Minimum clock pulse width; HIGH	5	t_{WCPH}	50	25		ns	see also waveforms Fig.4
	10		30	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	40	20		ns	
	10		30	15		ns	
	15		20	10		ns	
Recovery time for MR	5	t_{RMR}	40	20		ns	
	10		30	15		ns	
	15		20	10		ns	
Maximum clock pulse frequency	5	f_{max}	10	20		MHz	
	10		15	30		MHz	
	15		25	50		MHz	

Note

1. For other loads than 50 pF at the n^{th} output, use the slope given.

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$400\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$5\ 200\ f_i + \sum (f_o C_L) \times V_{DD}^2$	

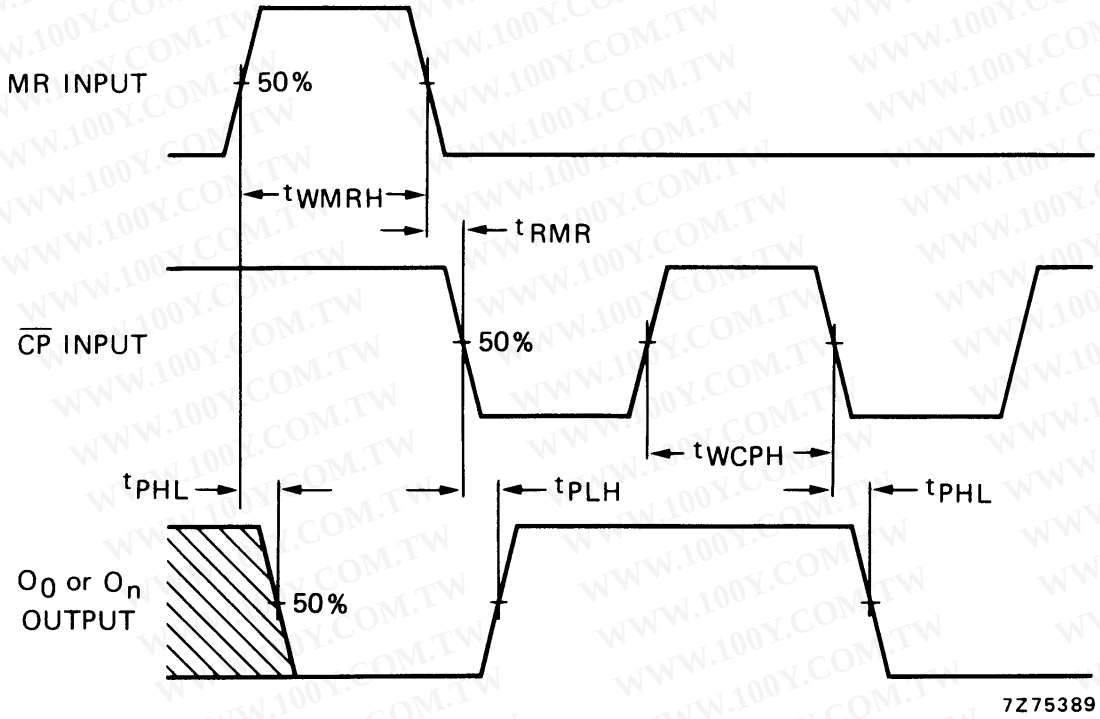

Fig.4 Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths.