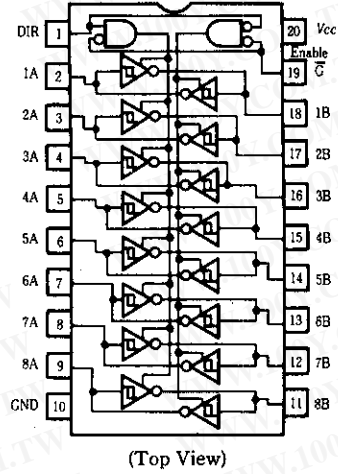


HD74LS642 ● Octal Bus Transceivers (inverted open-collector outputs)

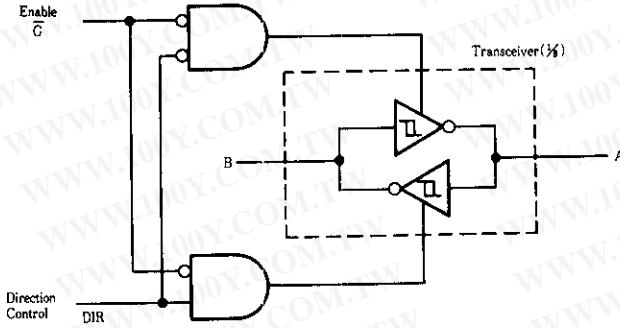
This octal bus transceiver is designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so that the buses are effectively isolated.

■ PIN ARRANGEMENT



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■ BLOCK DIAGRAM



■ RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | min | typ | max | unit |
|-----------------------------|-----------|------|------|------|------|
| Output current | V_{CC} | 4.75 | 5.00 | 5.25 | V |
| Output voltage | V_{OH} | — | — | 5.5 | V |
| Output current | I_{OL} | — | — | 24 | mA |
| Operating temperature range | T_{opr} | -20 | 25 | 75 | °C |

■ FUNCTION TABLE

| Enable \bar{G} | Direction Control DIR | Operation |
|------------------|-----------------------|-------------------------|
| L | L | \bar{B} data to A bus |
| L | H | \bar{A} data to B bus |
| H | X | Isolation |

H; high level,
 L; low level,
 X; irrelevant

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

| Item | Symbol | Test Conditions | min | typ* | max | Unit | |
|---------------------|-----------------|--|------------------------|------|------|---------------|----|
| Input voltage | V_{IH} | | 2.0 | | | V | |
| | V_{IL} | | | | 0.8 | | |
| Hysteresis | $V_T^+ - V_T^-$ | $V_{CC} = 4.75\text{V}$ | 0.2 | | | V | |
| Output current | I_{OH} | $V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$, $V_{OH} = 5.5\text{V}$ | | | 100 | μA | |
| Output voltage | V_{OL} | $V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$ | $I_{OL} = 12\text{mA}$ | | 0.4 | V | |
| | | | $I_{OL} = 24\text{mA}$ | | 0.5 | | |
| Input current | I_{IH} | $V_{CC} = 5.25\text{V}$, $V_I = 2.7\text{V}$ | | | 20 | μA | |
| | I_{IL} | $V_{CC} = 5.25\text{V}$, $V_I = 0.4\text{V}$ | | | -400 | μA | |
| Supply current** | I_{CCB} | $V_{CC} = 5.25\text{V}$ | | | 48 | 70 | mA |
| | | | | | 62 | 90 | |
| | | | | | 64 | 95 | |
| Input clamp voltage | V_{IK} | $V_{CC} = 4.75\text{V}$, $I_{IN} = -18\text{mA}$ | | | -1.5 | V | |

* $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

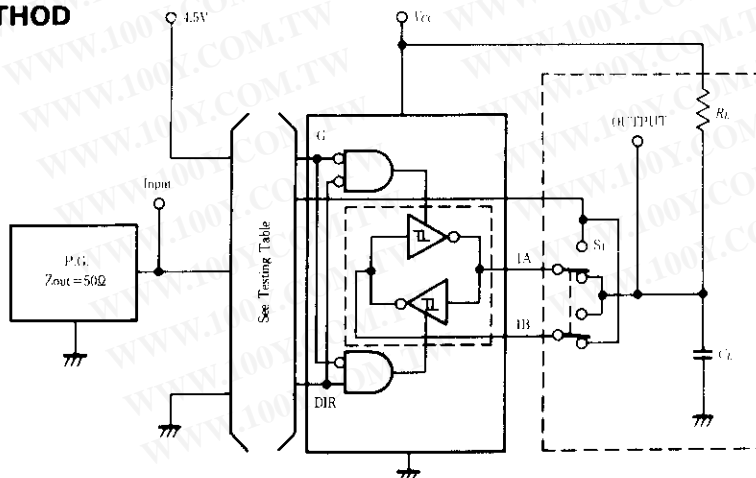
** I_{CC} is measured with all outputs open.

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$)

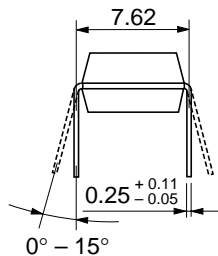
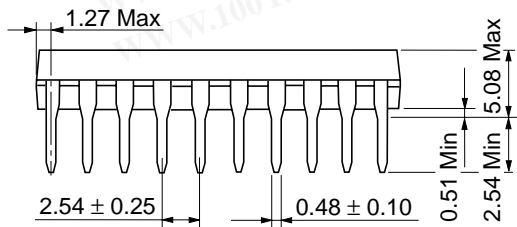
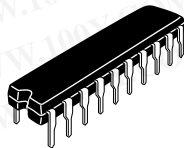
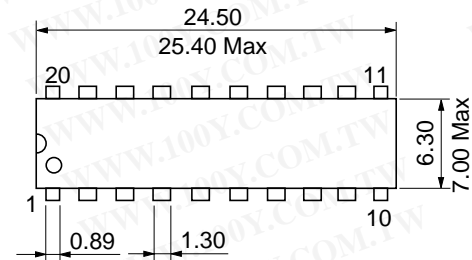
| Item | Symbol | Input | Output | Test Conditions | min | typ | max | Unit |
|------------------------|-----------|-------|--------|--|-----|-----|-----|------|
| Propagation delay time | t_{PLH} | A | B | $C_L = 45\text{pF}$ $R_L = 667\ \Omega$ | - | 19 | 25 | ns |
| | | B | A | | - | 19 | 25 | ns |
| | t_{PHL} | A | B | | - | 14 | 25 | ns |
| | | B | A | | - | 14 | 25 | ns |
| Output enable time | t_{PLH} | G | A | | - | 26 | 40 | ns |
| | | G | B | | - | 28 | 40 | ns |
| | t_{PHL} | G | A | | - | 43 | 60 | ns |
| | | G | B | | - | 39 | 60 | ns |

TESTING METHOD

Test Circuit



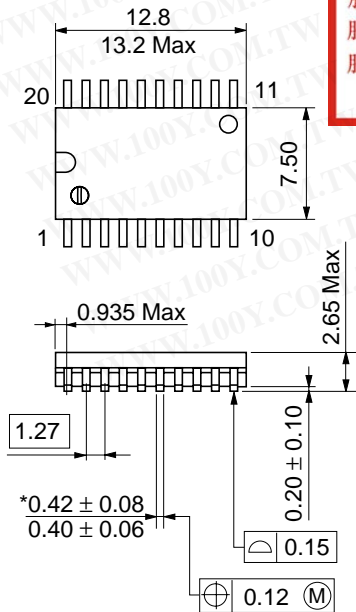
- Notes)
1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B are identical to above load circuit.
 2. C_L includes probe and jig capacitance.
 3. S_1 is a input-output switch.



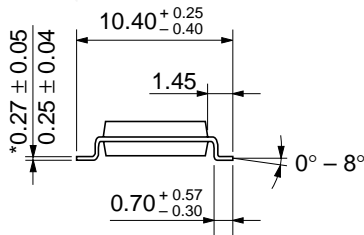
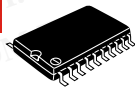
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| | |
|--------------------------|----------|
| Hitachi Code | DP-20N |
| JEDEC | — |
| EIAJ | Conforms |
| Weight (reference value) | 1.26 g |

Unit: mm



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| | |
|--------------------------|----------|
| Hitachi Code | FP-20DB |
| JEDEC | Conforms |
| EIAJ | — |
| Weight (reference value) | 0.52 g |

*Dimension including the plating thickness
 Base material dimension