élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2072C

730 MHz Closed Loop Buffer

Features

- 730 MHz −3 dB bandwidth (0.5 V_{PP})
- 5 ns settling to 0.2%
- V_S = ±5V @ 15 mA
- Low distortion: HD2, HD3 of −65 dBc at 20 MHz
- Overload/short-circuit protected
- Closed-loop, unity gain
- Low cost
- Direct replacement for CLC110

Applications

- Video buffer
- Video distribution
- HDTV buffer
- High-speed A/D buffer
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2072CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2072CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description

The EL2072 is a wide bandwidth, fast settling monolithic buffer built using an advanced complementary bipolar process. This buffer is closed loop to achieve lower output impedance and higher gain accuracy. Designed for closed-loop unity gain, the EL2072 has a 730 MHz −3 dB bandwidth and 5 ns settling to 0.2% while consuming only 15 mA of supply current.

The EL2072 is an obvious high-performance solution for video distribution and line-driving applications. With low 15 mA supply current and a 70 mA output drive, performance in these areas is assured.

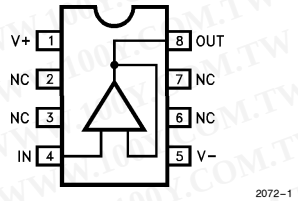
The EL2072's settling to 0.2% in 5 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 730 MHz bandwidth and extremely linear phase allow unmatched signal fidelity.

The EL2072 can be used inside an amplifier loop or PLL as its wide bandwidth and fast rise time have minimal effect on loop dynamics.

Elantec products and facilities comply with MIL-I-45028A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document *QRA-1: Elantec's Processing, Monolithic Integrated Circuits*.

Connection Diagram

DIP and SO Package



Top View

Manufactured under U.S. Patent No. 4,893,091

December 1995 Rev E

EL2072C
730 MHz Closed Loop Buffer

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V	Operating Temperature	−40°C to +85°C
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.	Junction Temperature	175°C
		Storage Temperature	−60°C to +150°C
		Thermal Resistance	θ_{JA} = 95°C/W P-DIP
			θ_{JA} = 175°C/W SO
Input Voltage	±V_S	Note: See EL2071/EL2171 for Thermal Impedance curves.	

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics
V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Output Offset Voltage		25°C		2.0	8.0	I	mV
			T_{MIN}			16.0	V	mV
			T_{MAX}			13.0	V	mV
TCV_{OS}	Average Offset Voltage Drift		25°C − T_{MAX}		20.0	50.0	IV	µV/°C
			25°C − T_{MIN}		20.0	100.0		
I_B	Input Bias Current		25°C, T_{MAX}		10.0	50.0	II	µA
			T_{MIN}			100.0	V	µA
TCI_B	Average Input Bias Current Drift		25°C − T_{MAX}		200.0	300.0	IV	nA/°C
			25°C − T_{MIN}		200.0	700.0		
A_V	Small Signal Gain	R_L = 100Ω	25°C	0.96	0.98		I	V/V
			T_{MIN}, T_{MAX}	0.95			V	V/V
ILIN	Integral End Point linearity	±2V F.S.	25°C		0.2	0.4	IV	%F.S.
			T_{MIN}			0.8	IV	%F.S.
			T_{MAX}			0.3	IV	%F.S.
PSRR	Power Supply Rejection Ratio		All	45.0	65.0		II	dB
I_S	Supply Current—Quiescent	No Load	All		15.0	20.0	II	mA

TD is 3.3in

DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
R_{IN}	Input Resistance		25°C	100.0	160.0		I	kΩ
			T_{MIN}	50.0			V	kΩ
			T_{MAX}	200.0			V	kΩ
C_{IN}	Input Capacitance		25°C		1.6	2.2	IV	pF
			T_{MIN}, T_{MAX}			2.5	IV	pF
R_{OUT}	Output Impedance (DC)		25°C		2.0	3.0	IV	Ω
			T_{MIN}, T_{MAX}			3.5	IV	Ω
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		II	mA
			T_{MIN}	45.0			V	mA
V_{OUT}	Output Voltage Swing	R_L = 100Ω	25°C, T_{MAX}	±3.2	±4.0		II	V
			T_{MIN}	±3.0			V	V

AC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth (V_{OUT} < 0.5 V_{PP})		25°C	400.0	730.0		V	MHz
			T_{MIN}	400.0			IV	MHz
			T_{MAX}	300.0			IV	MHz
LSBW	−3 dB Bandwidth (V_{OUT} = 5.0 V_{PP})		25°C	55.0	90.0		IV	MHz
			T_{MIN}, T_{MAX}	50.0			IV	MHz
GAIN FLATNESS								
GFPL	Peaking V_{OUT} < 0.5 V_{PP}	<200 MHz	25°C		0.0	0.5	V	dB
			T_{MAX}			0.6	IV	dB
			T_{MIN}			0.8	IV	dB
GFR	Rolloff V_{OUT} < 0.5 V_{PP}	<200 MHz	25°C		0.0	0.8	V	dB
			T_{MIN}			1.0	IV	dB
			T_{MAX}			1.2	IV	dB
GDL	Group Delay	<200 MHz	25°C, T_{MIN}		0.75	1.0	IV	ns
			T_{MAX}			1.2	IV	ns
LPD	Linear Phase Deviation V_{OUT} < 0.5 V_{PP}	<200 MHz	25°C, T_{MIN}		0.7	1.5	IV	°
			T_{MAX}			2.0	IV	°

TD is 2.4in

TD is 3.5in

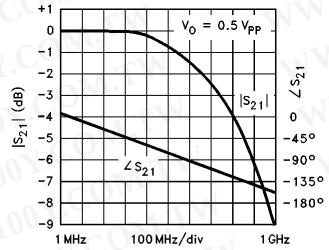
AC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$ unless otherwise specified

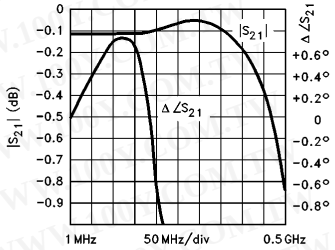
Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
TIME-DOMAIN RESPONSE								
TR1, TF1	Rise Time, Fall Time Input Signal Rise/Fall = 300 ps	0.5V Step	25°C, T_{MIN}		0.4	1.0	IV	ns
			T_{MAX}			1.4	IV	ns
TR2, TF2	Rise Time, Fall Time Input Signal Rise/Fall ≤ 1 ns	5.0V Step	25°C		4.5	7.5	IV	ns
			T_{MIN}, T_{MAX}			8.5	IV	ns
TS1	Settling Time to 0.2% Input Signal Rise/Fall ≤ 1 ns	2.0V Step	All		5.0	10.0	IV	ns
OS	Overshoot Input Signal Rise/Fall = 300 ps	0.5V Step	25°C		0.0	10.0	IV	%
			T_{MIN}, T_{MAX}			15.0	IV	%
SR	Slew Rate		25°C	500.0	800.0		IV	V/µs
			T_{MIN}, T_{MAX}	450.0			IV	V/µs
DISTORTION								
HD2	2nd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−55.0	−50.0	V	dBc
			T_{MIN}			−48.0	IV	dBc
			T_{MAX}			−55.0	IV	dBc
HD2A	2nd Harmonic Distortion at 50 MHz	2 V_{PP}	25°C , T_{MAX}		−50.0	−45.0	IV	dBc
			T_{MIN}			−40.0	IV	dBc
HD3	3rd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−65.0	−55.0	V	dBc
			T_{MIN}, T_{MAX}			−55.0	IV	dBc
HD3A	3rd Harmonic Distortion at 50 MHz	2 V_{PP}	25°C , T_{MIN}		−60.0	−50.0	IV	dBc
			T_{MAX}			−45.0	IV	dBc
EQUIVALENT INPUT NOISE								
NF	Noise Floor >100 kHz		25°C, T_{MIN}		−158.0	−155.0	IV	dBm (1 Hz)
			T_{MAX}			−154.0	IV	dBm (1 Hz)
INV	Integrated Noise 100 kHz to 200 MHz		25°C, T_{MIN}		40.0	57.0	IV	µV
			T_{MAX}			63.0	IV	µV

Typical Performance Curves (V_S = ±5V, R_L = 100Ω, R_S = 50Ω)

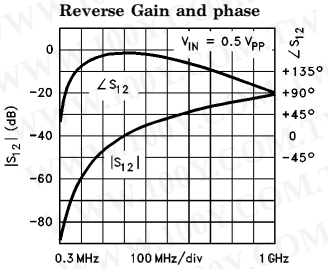
Forward Gain and Phase



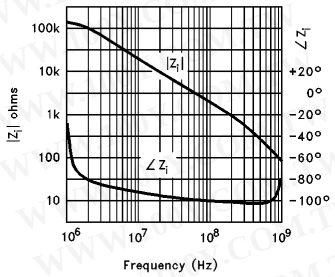
Gain Flatness & Deviation from Linear Phase



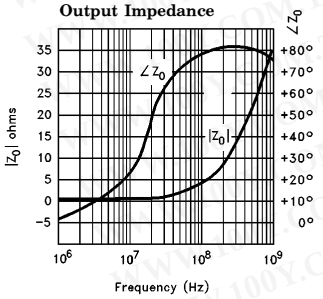
Reverse Gain and phase



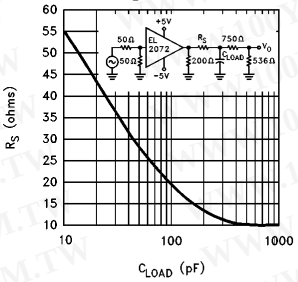
Input Impedance



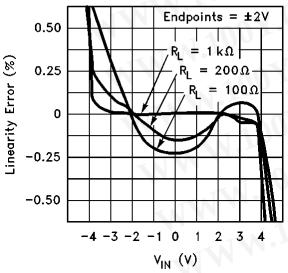
Output Impedance



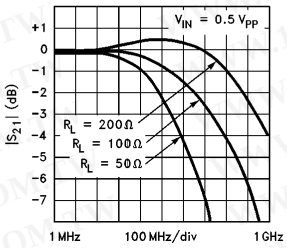
Recommended R_S vs Load Capacitance



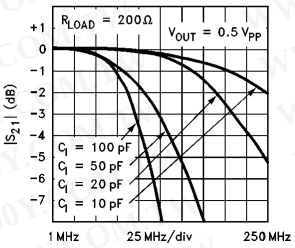
Integral Linearity Error



Frequency Response vs R_{load}



$|S_{21}|$ vs C_{load} with Recommended R_s



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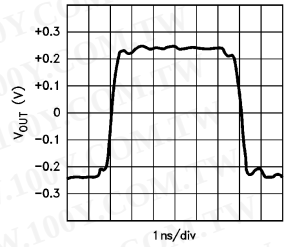
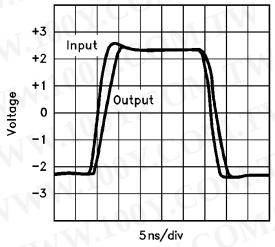
Typical Performance Curves (V_S = ±5V, R_L = 100Ω, R_S = 50Ω) — Contd.

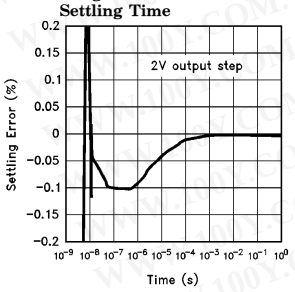
Small Signal Pulse Response



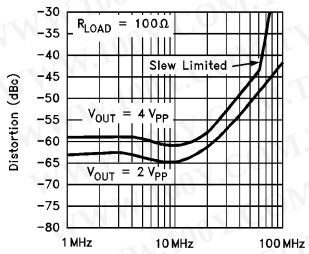
Large Signal Pulse Response



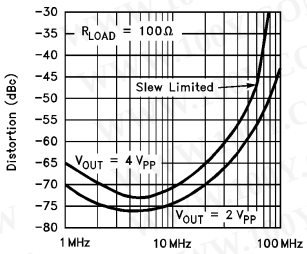
Long-Term Settling Time



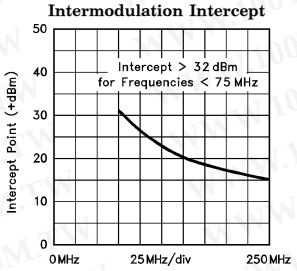
2nd Harmonic Distortion



3rd Harmonic Distortion



2-Tone, 3rd Order Intermodulation Intercept



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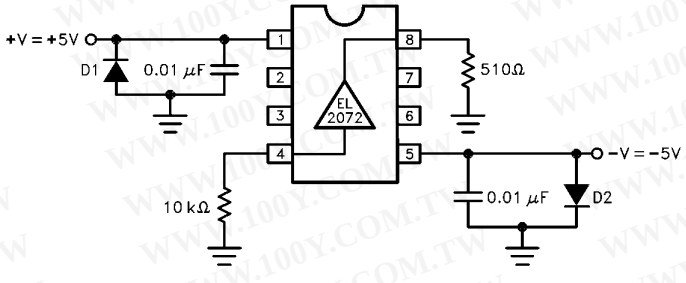
Burn-In Circuit



Printed Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. This is especially important for the EL2072, which has a typical bandwidth of 730 MHz. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. A closely-placed 0.01 µF ceramic capacitor between each supply pin and the ground plane is usually sufficient decoupling.

Pins 2, 3, 6, and 7 should be connected to the ground-plane to minimize capacitive feed-through, and all input and output traces should be laid out as transmission lines and terminated as close to the EL2072 package as possible.

Increasing capacitance on the output of the EL2072 will add phase shift, decreasing phase margin and increasing frequency-response peaking. A small series resistor before the capacitance decouples this effect, and should be used for large capacitance values. Please refer to the graphs for the appropriate resistor value to be used.