



勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
 Http://www.100y.com.tw

# CY7C199

## 32K x 8 Static RAM

### Features

- **High speed**  
— 10 ns
- **Fast  $t_{DOE}$**
- **CMOS for optimum speed/power**
- **Low active power**  
— 467 mW (max, 12 ns “L” version)
- **Low standby power**  
— 0.275 mW (max, “L” version)
- **2V data retention (“L” version only)**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

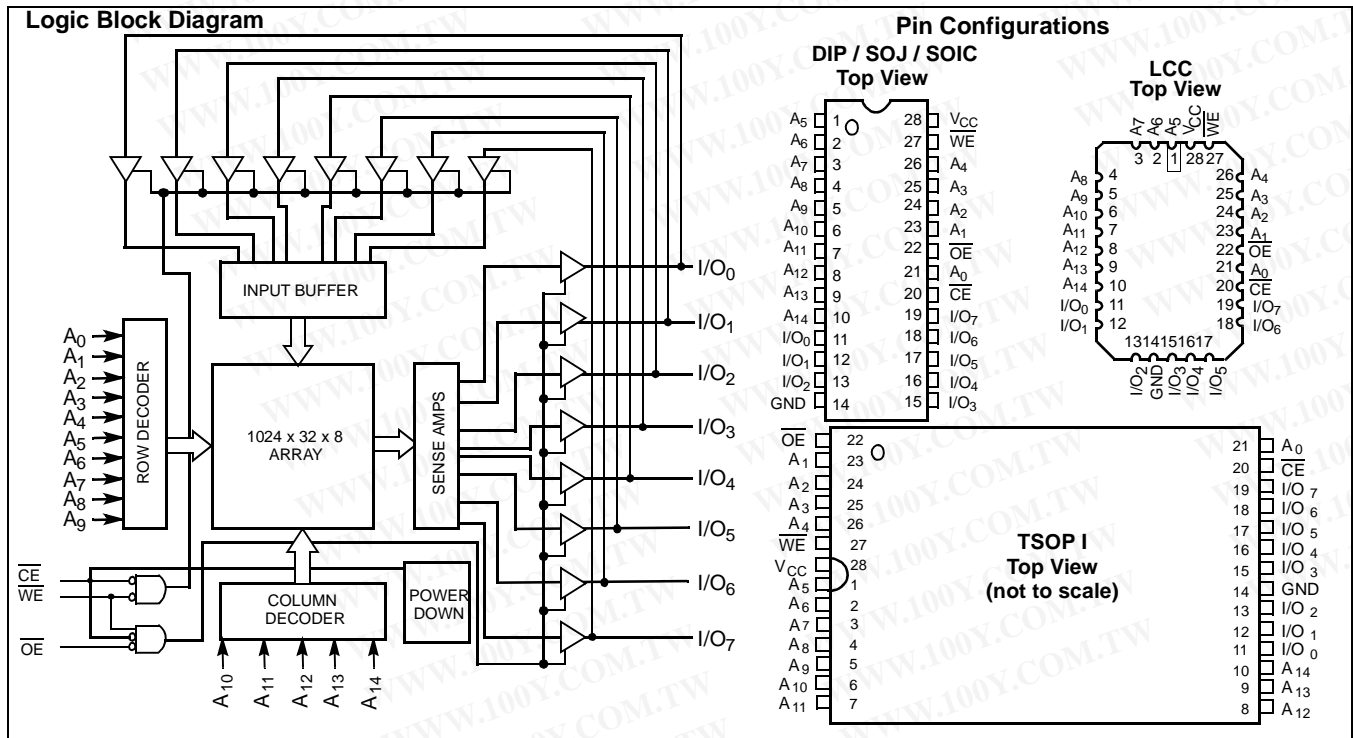
### Functional Description

The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion

is provided by an active LOW Chip Enable ( $\overline{CE}$ ) and active LOW Output Enable ( $\overline{OE}$ ) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW Write Enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ( $\overline{WE}$ ) is HIGH. A die coat is used to improve alpha immunity.



### Selection Guide

	7C199 -8	7C199 -10	7C199 -12	7C199 -15	7C199 -20	7C199 -25	7C199 -35	7C199 -45	Unit
Maximum Access Time	8	10	12	15	20	25	35	45	ns
Maximum Operating Current	120	110	160	155	150	150	140	140	mA
	L	90	90	90	90	80	70		
Maximum CMOS Standby Current	0.5	0.5	10	10	10	10	10	10	mA
	L	0.05	0.05	0.05	0.05	0.05	0.05		

Shaded area contains advance information.



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## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14) .....	-0.5V to +7.0V
DC Voltage Applied to Outputs in High-Z State <sup>[1]</sup> .....	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage <sup>[1]</sup> .....	-0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage .....	> 2001V (per MIL-STD-883, Method 3015)
Latch-up Current .....	> 200 mA

## Operating Range

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

## Electrical Characteristics Over the Operating Range (-8, -10, -12, -15)<sup>[3]</sup>

Parameter	Description	Test Conditions	7C199-8		7C199-10		7C199-12		7C199-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	-5	+5	-5	+5	µA
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	µA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	Com'l	120		110		160		155	mA
			L			85		85		100	mA
			Mil							180	mA
$I_{SB1}$	Automatic CE Power-down Current—TTL Inputs	Max. $V_{CC}$ , $CE \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	Com'l	5		5		30		30	mA
			L			5		5		5	mA
$I_{SB2}$	Automatic CE Power-down Current—CMOS Inputs	Max. $V_{CC}$ , $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = 0$	Com'l	0.5		0.5		10		10	mA
			L	0.05		0.05		0.05		0.05	mA
			Mil							15	mA

## Electrical Characteristics Over the Operating Range (-20, -25, -35, -45)<sup>[3]</sup>

Parameter	Description	Test Conditions	7C199-20		7C199-25		7C199-35		7C199-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	-5	+5	-5	+5	µA
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	µA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	Com'l	150		150		140		140	mA
			L	90		80		70		70	mA
			Mil	170		150		150		150	mA

Shaded area contains advance information.

### Notes:

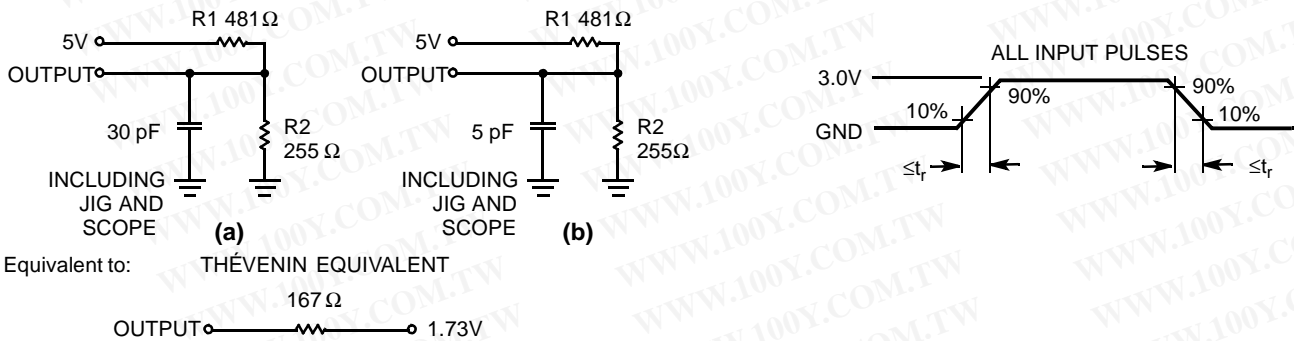
- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

**Electrical Characteristics** Over the Operating Range (-20, -25, -35, -45) (continued)<sup>[3]</sup>

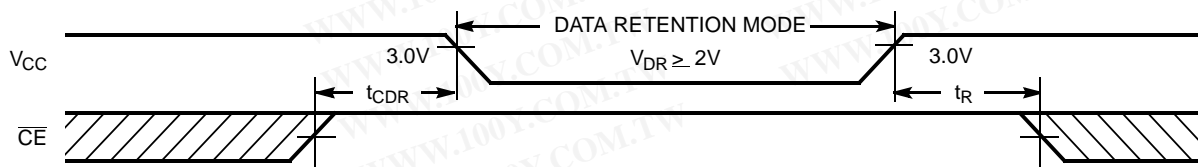
Parameter	Description	Test Conditions	7C199-20		7C199-25		7C199-35		7C199-45		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$I_{SB1}$	Automatic CE Power-down Current—TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	Com'l		30		30		25		25	mA
			L		5		5		5		5	mA
$I_{SB2}$	Automatic CE Power-down Current—CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f=0$	Com'l		10		10		10		10	mA
			L		0.05		0.05		0.05		0.05	$\mu A$
			Mil		15		15		15		15	mA

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ C$ , $f = 1$ MHz, $V_{CC} = 5.0V$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

**AC Test Loads and Waveforms<sup>[5]</sup>**

**Data Retention Characteristics** Over the Operating Range (L-version only)

Parameter	Description	Conditions <sup>[6]</sup>	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	Com'l	$V_{CC} = V_{DR} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		$\mu A$
		Com'l L		10	$\mu A$
$t_{CDR}$ <sup>[4]</sup>	Chip Deselect to Data Retention Time		0		ns
$t_R$ <sup>[5]</sup>	Operation Recovery Time		200		$\mu s$

**Data Retention Waveform**

**Note:**

4. Tested initially and after any design or process changes that may affect these parameters.
5.  $t_R \leq 3$  ns for the -12 and the -15 speeds.  $t_R \leq 5$  ns for the -20 and slower speeds
6. No input may exceed  $V_{CC} + 0.5V$ .



**Switching Characteristics** Over the Operating Range (-8, -10, -12, -15) [3, 7]

Parameter	Description	7C199-8		7C199-10		7C199-12		7C199-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	8		10		12		15		ns
t <sub>AA</sub>	Address to Data Valid		8		10		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
t <sub>ACE</sub>	CE LOW to Data Valid		8		10		12		15	ns
t <sub>DOE</sub>	OE LOW to Data Valid		4.5		5		5		7	ns
t <sub>LZOE</sub>	OE LOW to Low-Z <sup>[8]</sup>	0		0		0		0		ns
t <sub>HZOE</sub>	OE HIGH to High-Z <sup>[8, 9]</sup>		5		5		5		7	ns
t <sub>LZCE</sub>	CE LOW to Low-Z <sup>[8]</sup>	3		3		3		3		ns
t <sub>HZCE</sub>	CE HIGH to High-Z <sup>[8, 9]</sup>		4		5		5		7	ns
t <sub>PU</sub>	CE LOW to Power-up	0		0		0		0		ns
t <sub>PD</sub>	CE HIGH to Power-down		8		10		12		15	ns
<b>Write Cycle</b> <sup>[10, 11]</sup>										
t <sub>WC</sub>	Write Cycle Time	8		10		12		15		ns
t <sub>SCE</sub>	CE LOW to Write End	7		7		9		10		ns
t <sub>AW</sub>	Address Set-up to Write End	7		7		9		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	WE Pulse Width	7		7		8		9		ns
t <sub>SD</sub>	Data Set-up to Write End	5		5		8		9		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>HZWE</sub>	WE LOW to High-Z <sup>[9]</sup>		5		6		7		7	ns
t <sub>LZWE</sub>	WE HIGH to Low-Z <sup>[8]</sup>	3		3		3		3		ns

**Switching Characteristics** Over the Operating Range (-20, -25, -35, -45)<sup>[3, 7]</sup>

Parameter	Description	7C199-20		7C199-25		7C199-35		7C199-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	20		25		35		45		ns
t <sub>AA</sub>	Address to Data Valid		20		25		35		45	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
t <sub>ACE</sub>	CE LOW to Data Valid		20		25		35		45	ns
t <sub>DOE</sub>	OE LOW to Data Valid		9		10		16		16	ns
t <sub>LZOE</sub>	OE LOW to Low-Z <sup>[8]</sup>	0		0		0		0		ns
t <sub>HZOE</sub>	OE HIGH to High-Z <sup>[8, 9]</sup>		9		11		15		15	ns
t <sub>LZCE</sub>	CE LOW to Low-Z <sup>[8]</sup>	3		3		3		3		ns
t <sub>HZCE</sub>	CE HIGH to High-Z <sup>[8, 9]</sup>		9		11		15		15	ns
t <sub>PU</sub>	CE LOW to Power-up	0		0		0		0		ns

Shaded area contains advance information.

**Notes:**

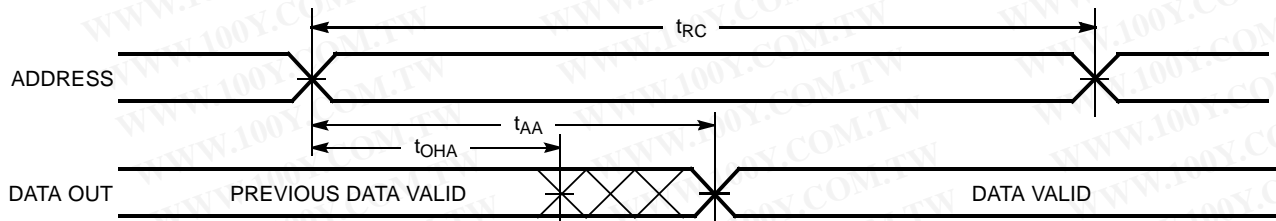
- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Switching Characteristics** Over the Operating Range (-20, -25, -35, -45)<sup>[3, 7]</sup>

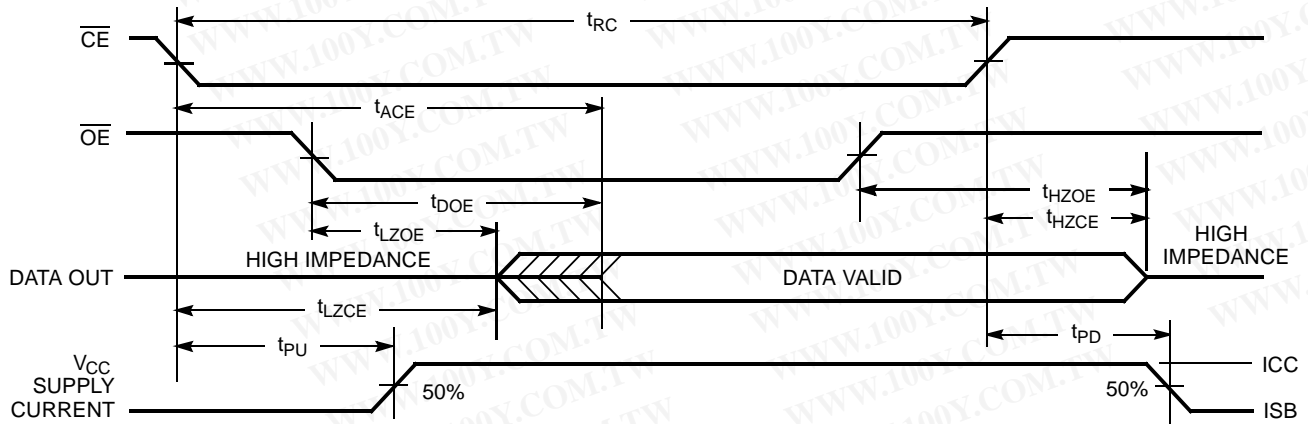
Parameter	Description	7C199-20		7C199-25		7C199-35		7C199-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PD}$	CE HIGH to Power-down		20		20		20		25	ns
<b>Write Cycle<sup>[10,11]</sup></b>										
$t_{WC}$	Write Cycle Time	20		25		35		45		ns
$t_{SCE}$	CE LOW to Write End	15		18		22		22		ns
$t_{AW}$	Address Set-up to Write End	15		20		30		40		ns
$t_{HA}$	Address Hold from Write End	0		0		0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		0		0		ns
$t_{PWE}$	WE Pulse Width	15		18		22		22		ns
$t_{SD}$	Data Set-up to Write End	10		10		15		15		ns
$t_{HD}$	Data Hold from Write End	0		0		0		0		ns
$t_{HZWE}$	WE LOW to High-Z <sup>[9]</sup>		10		11		15		15	ns
$t_{LZWE}$	WE HIGH to Low-Z <sup>[8]</sup>	3		3		3		3		ns

**Switching Waveforms**

**Read Cycle No. 1<sup>[12, 13]</sup>**



**Read Cycle No. 2<sup>[13, 14]</sup>**

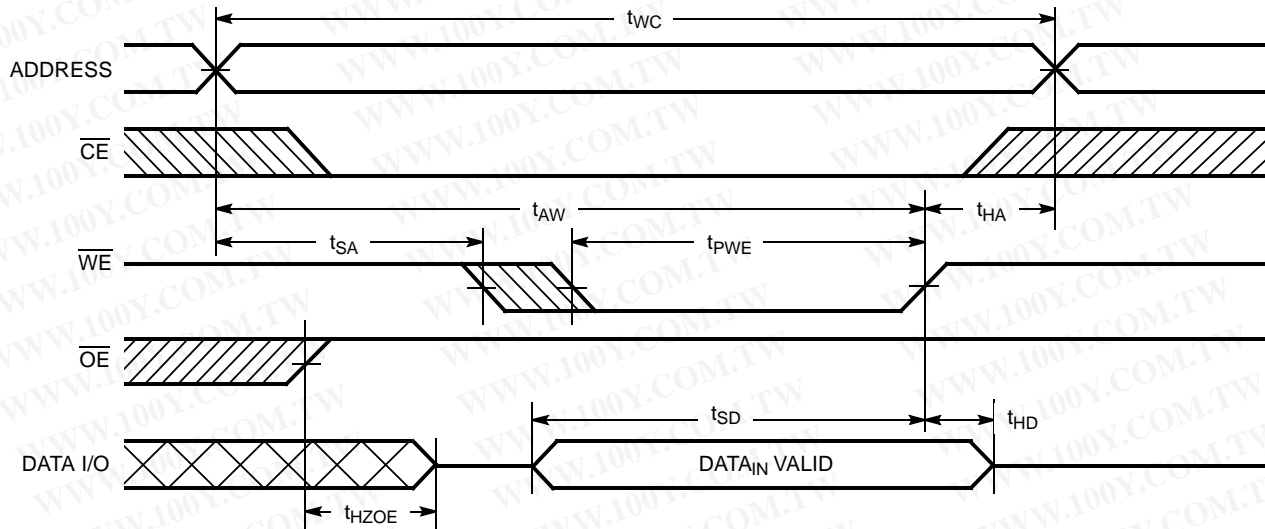


**Notes:**

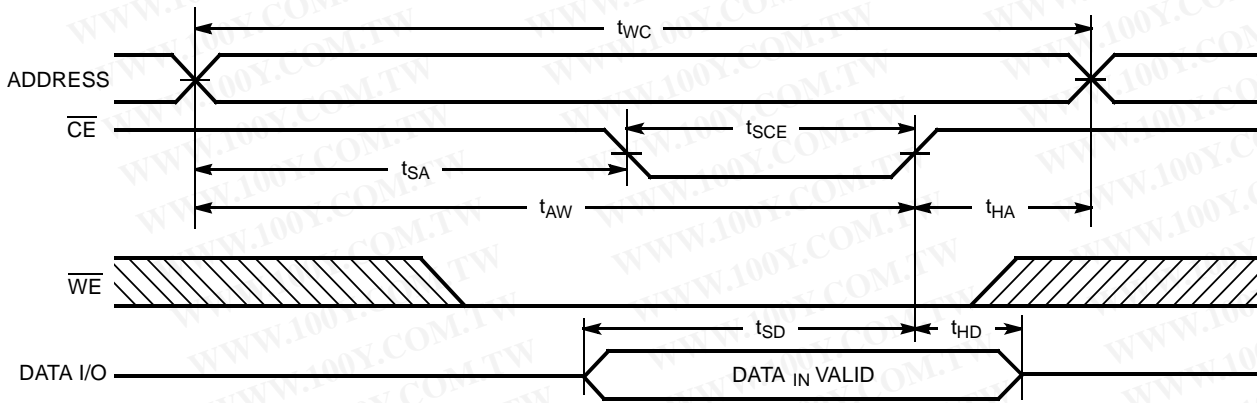
- 12. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
- 13. WE is HIGH for read cycle.
- 14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

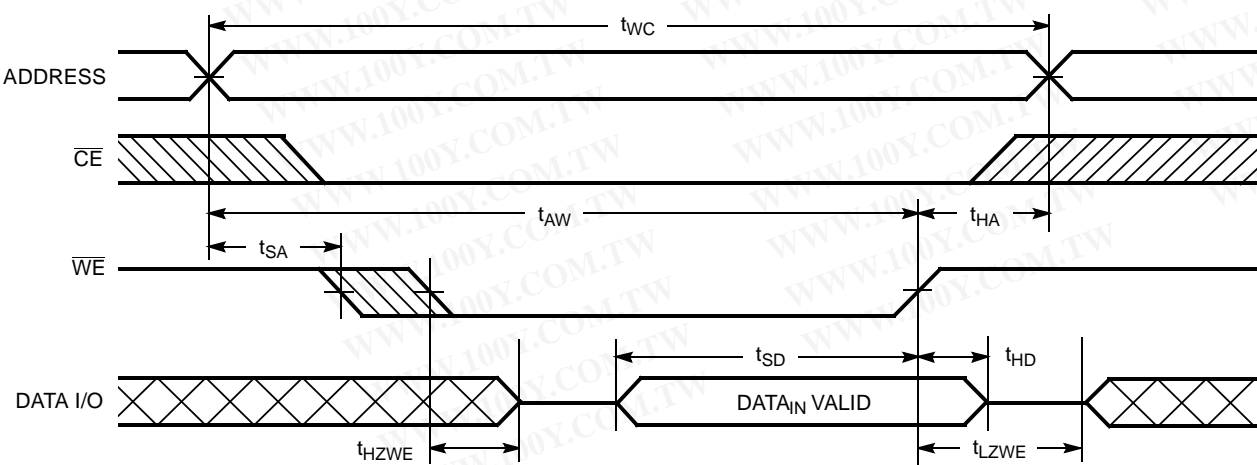
Write Cycle No. 1 (WE Controlled)<sup>[10, 15, 16]</sup>



Write Cycle No. 2 (CE Controlled)<sup>[10, 15, 16]</sup>



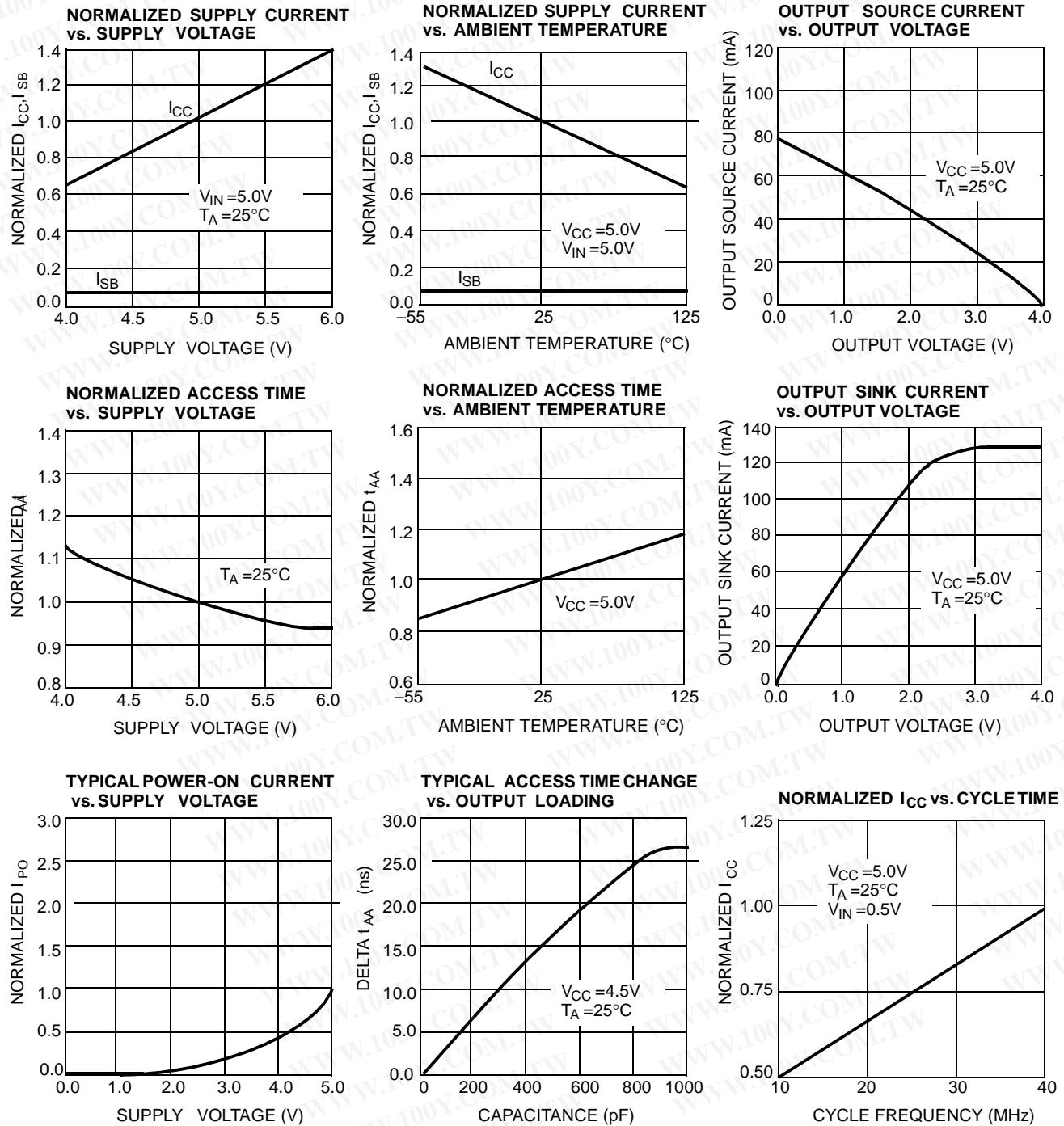
Write Cycle No. 3 (WE Controlled  $\overline{OE}$  LOW)<sup>[11, 16]</sup>



Notes:

15. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

### Typical DC and AC Characteristics



### Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output disabled	Active ( $I_{CC}$ )



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## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range	
8	CY7C199-8VC	V21	28-Lead Molded SOJ	Commercial	
	CY7C199-8ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-8VC	V21	28-Lead Molded SOJ		
	CY7C199L-8ZC	Z28	28-Lead Thin Small Outline Package		
10	CY7C199-10VC	V21	28-Lead Molded SOJ	Commercial	
	CY7C199-10ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-10VC	V21	28-Lead Molded SOJ		
	CY7C199L-10ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199-10VI	V21	28-Lead Molded SOJ	Industrial	
	CY7C199-10ZI	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-10VI	V21	28-Lead Molded SOJ		
	CY7C199L-10ZI	Z28	28-Lead Thin Small Outline Package		
12	CY7C199-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial	
	CY7C199-12VC	V21	28-Lead Molded SOJ		
	CY7C199-12ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-12PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199L-12VC	V21	28-Lead Molded SOJ	Industrial	
	CY7C199L-12ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199-12VI	V21	28-Lead Molded SOJ		
	CY7C199-12ZI	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-12VI	V21	28-Lead Molded SOJ		
	CY7C199L-12ZI	Z28	28-Lead Thin Small Outline Package		
15	CY7C199-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial	
	CY7C199-15VC	V21	28-Lead Molded SOJ		
	CY7C199-15ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-15PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199L-15VC	V21	28-Lead Molded SOJ	Industrial	
	CY7C199L-15ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199-15VI	V21	28-Lead Molded SOJ		
	CY7C199-15ZI	Z28	28-Lead Thin Small Outline Package		
	CY7C199-15DMB	D22	28-Lead (300-Mil) CerDIP		Military
	CY7C199-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier		
20	CY7C199L-15DMB	D22	28-Lead (300-Mil) CerDIP	Military	
	CY7C199L-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier		
	CY7C199-20PC	P21	28-Lead (300-Mil) Molded DIP		Commercial
	CY7C199-20VC	V21	28-Lead Molded SOJ		
	CY7C199-20ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199L-20PC	P21	28-Lead (300-Mil) Molded DIP		
	CY7C199L-20VC	V21	28-Lead Molded SOJ	Industrial	
	CY7C199L-20ZC	Z28	28-Lead Thin Small Outline Package		
	CY7C199-20VI	V21	28-Lead Molded SOJ		
	CY7C199-20ZI	Z28	28-Lead Thin Small Outline Package		
	CY7C199-20DMB	D22	28-Lead (300-Mil) CerDIP	Military	
	CY7C199-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier		
CY7C199L-20DMB	D22	28-Lead (300-Mil) CerDIP			
CY7C199L-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier			

Shaded area contains advance information. Contact your Cypress sales representative for availability



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 勝特力电子(深圳) 86-755-83298787  
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# CY7C199

## Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C199-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-25SC	S21	28-Lead Molded SOIC	
	CY7C199-25VC	V21	28-Lead Molded SOJ	
	CY7C199-25ZC	Z28	28-Lead Thin Small Outline Package	Industrial
	CY7C199-25SI	S21	28-Lead Molded SOIC	
	CY7C199-25VI	V21	28-Lead Molded SOJ	
	CY7C199-25ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C199-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-35SC	S21	28-Lead Molded SOIC	
	CY7C199-35VC	V21	28-Lead Molded SOJ	
	CY7C199-35ZC	Z28	28-Lead Thin Small Outline Package	Industrial
	CY7C199-35SI	S21	28-Lead Molded SOIC	
	CY7C199-35VI	V21	28-Lead Molded SOJ	
	CY7C199-35ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C199-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advance information. Contact your Cypress sales representative for availability

## MILITARY SPECIFICATIONS Group A Subgroup Testing

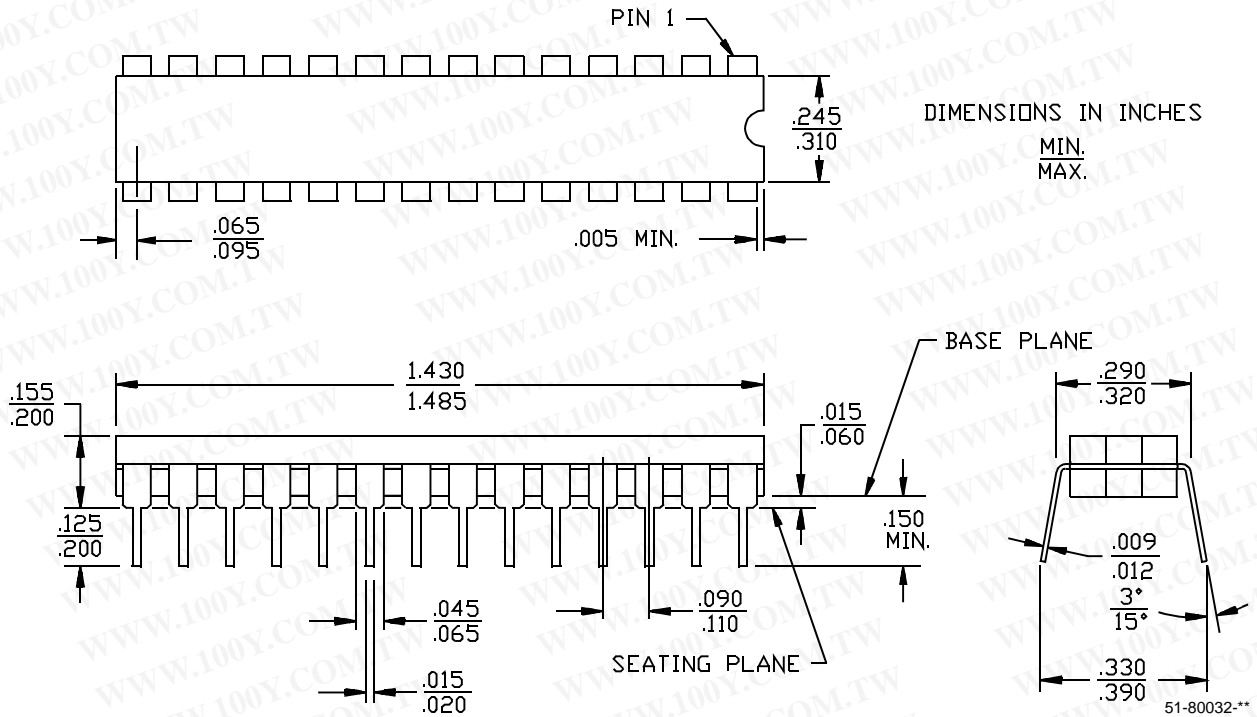
### DC Characteristics

Parameter	Subgroups
$V_{OH}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{IH}$	1, 2, 3
$V_{IL Max.}$	1, 2, 3
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{CC}$	1, 2, 3
$I_{SB1}$	1, 2, 3
$I_{SB2}$	1, 2, 3

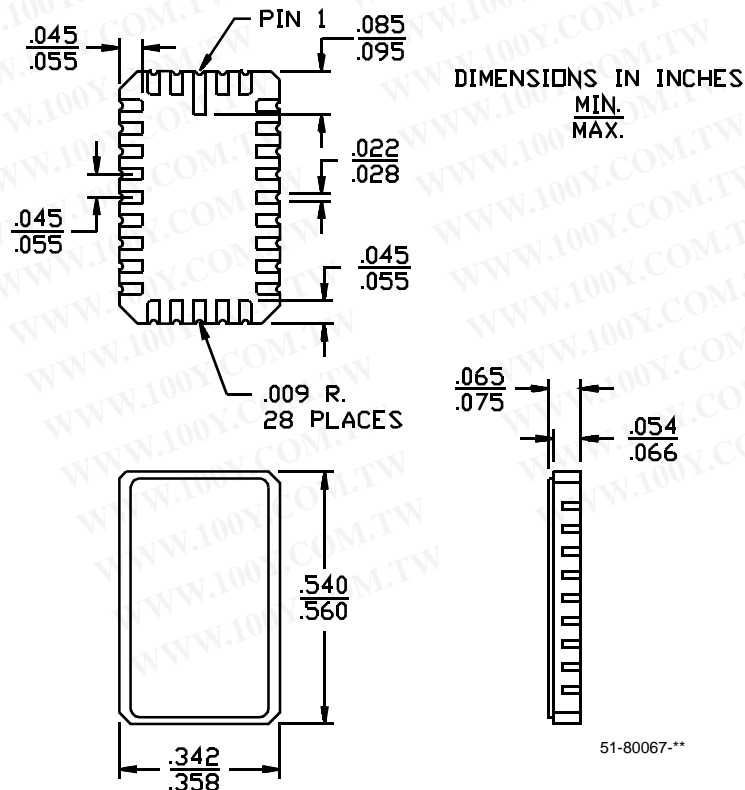
### Switching Characteristics

Parameter	Subgroups
<b>Read Cycle</b>	
$t_{RC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{OHA}$	7, 8, 9, 10, 11
$t_{ACE}$	7, 8, 9, 10, 11
$t_{DOE}$	7, 8, 9, 10, 11
<b>Write Cycle</b>	
$t_{WC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{AW}$	7, 8, 9, 10, 11
$t_{HA}$	7, 8, 9, 10, 11
$t_{SA}$	7, 8, 9, 10, 11
$t_{PWE}$	7, 8, 9, 10, 11
$t_{SD}$	7, 8, 9, 10, 11
$t_{HD}$	7, 8, 9, 10, 11

**28-pin (300-Mil) CerDIP D22**  
 MIL-STD-1835 D-15 Config. A

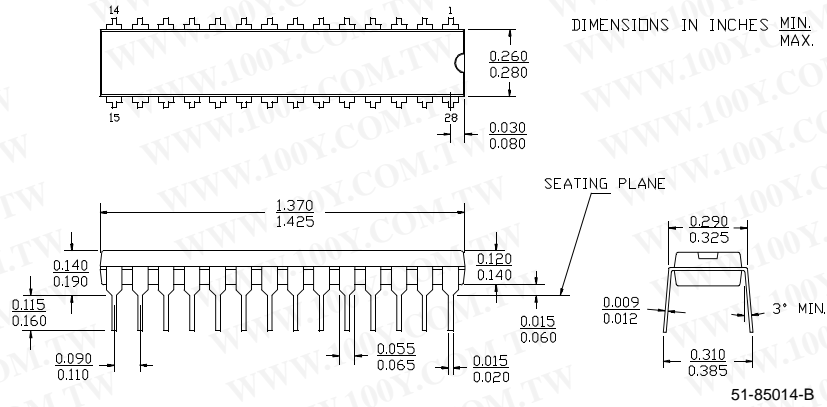


**28-pin Rectangular Leadless Chip Carrier L54**  
 MIL-STD-1835-11A

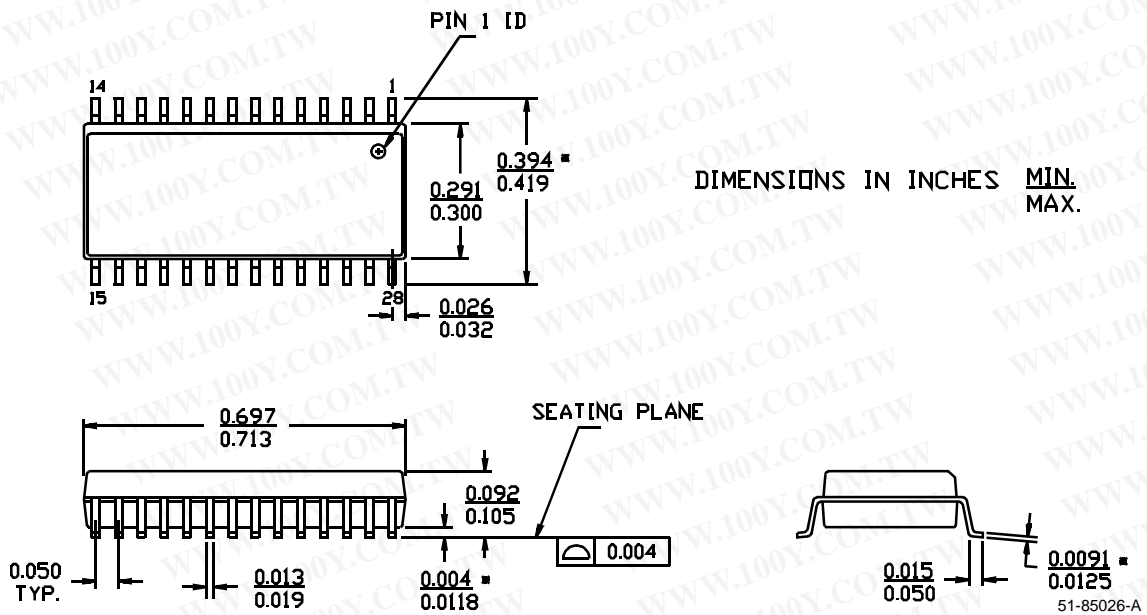


Package Diagrams (continued)

28-pin (300-Mil) Molded DIP P21

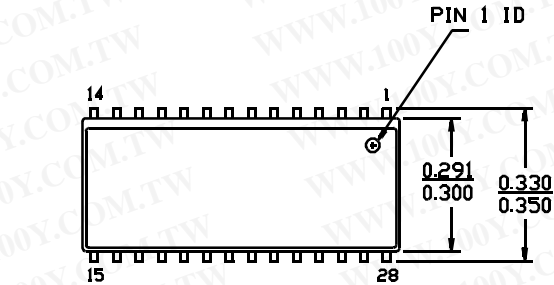


28-pin (300-Mil) Molded SOIC S21

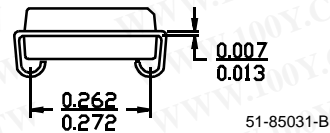
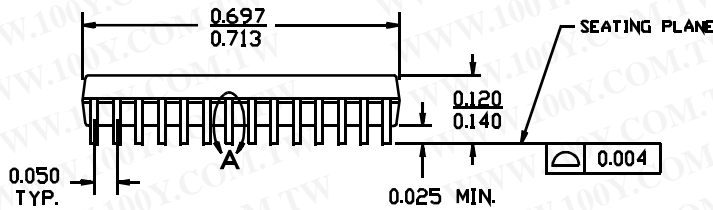
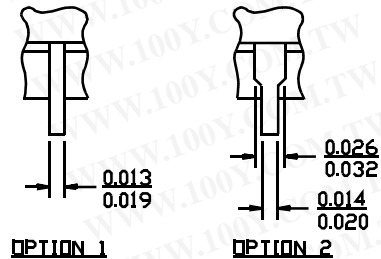


Package Diagrams (continued)

28-pin (300-Mil) Molded SOJ V21  
 DIMENSIONS IN INCHES MIN. MAX.

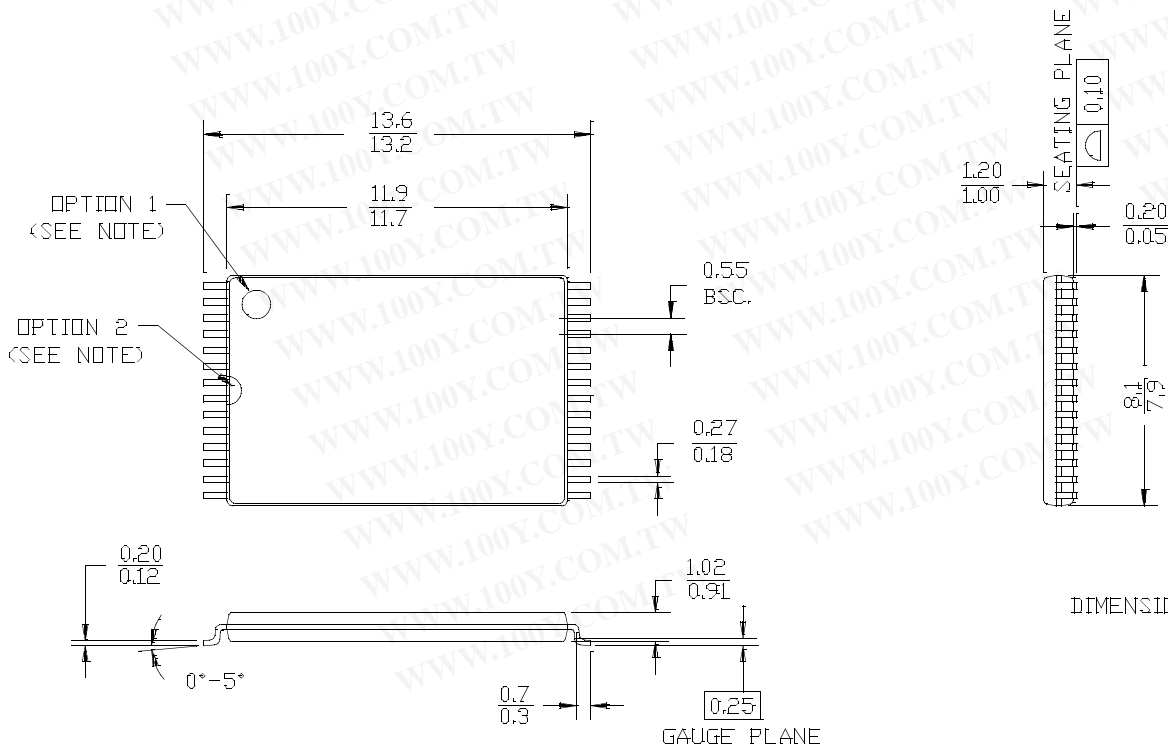


DETAIL A  
 EXTERNAL LEAD DESIGN



28-Lead Thin Small Outline Package Type 1 (8x13.4 mm) Z28

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



DIMENSION IN MM  
 MAX.  
 MIN.

51-85071-G

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## Document History Page

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**CY7C199**

**Document Title: CY7C199 32K x 8 Static RAM**  
**Document Number: 38-05160**

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109971	10/28/01	SZV	Change from Spec number: 38-00239 to 38-05160
*A	121730	01/09/02	DFP	Updated Product Offering table.