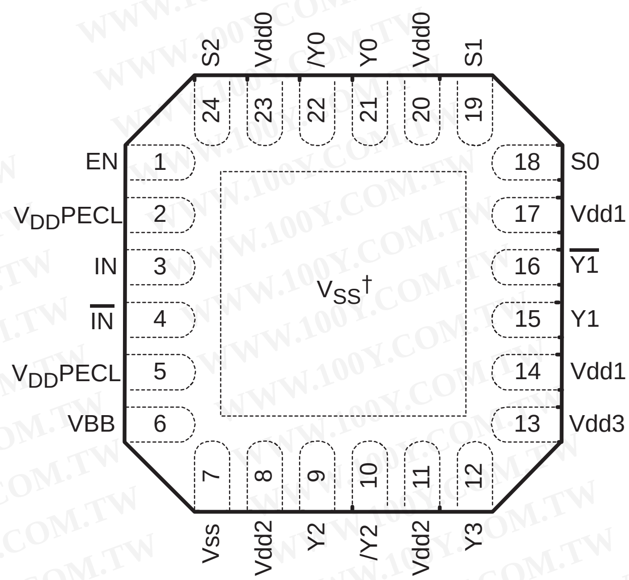
- **Distributes One Differential Clock Input to Three LVPECL Differential Clock Outputs and One LVCMOS Single-Ended Output**
- **Programmable Output Divider for Two LVPECL Output and LVCMOS Output**
- **Low-Output Skew 15 ps (Typical) for Clock-Distribution Applications for LVPECL Outputs; 1.6-ns Output Skew Between LVCMOS and LVPECL Transitions Minimizing Noise**
- **V_{CC} Range 3 V−3.6 V**
- **Signaling Rate Up to 800-MHz LVPECL and 200-MHz LVCMOS**
- **Differential Input Stage for Wide Common-Mode Range**
- **Provides VBB Bias Voltage Output for Single-Ended Input Signals**
- **Receiver Input Threshold ±75 mV**
- **24-Pin MLF Package (4 mm x 4 mm)**
- **Accepts Any Differential Signaling: LVDS, HSTL, CML, VML, SSTL-2, and Single-Ended: LVTTL/LVCMOS**

MLF PACKAGE
(TOP VIEW)



† PowerPad must be connected to V_{SS}.

description

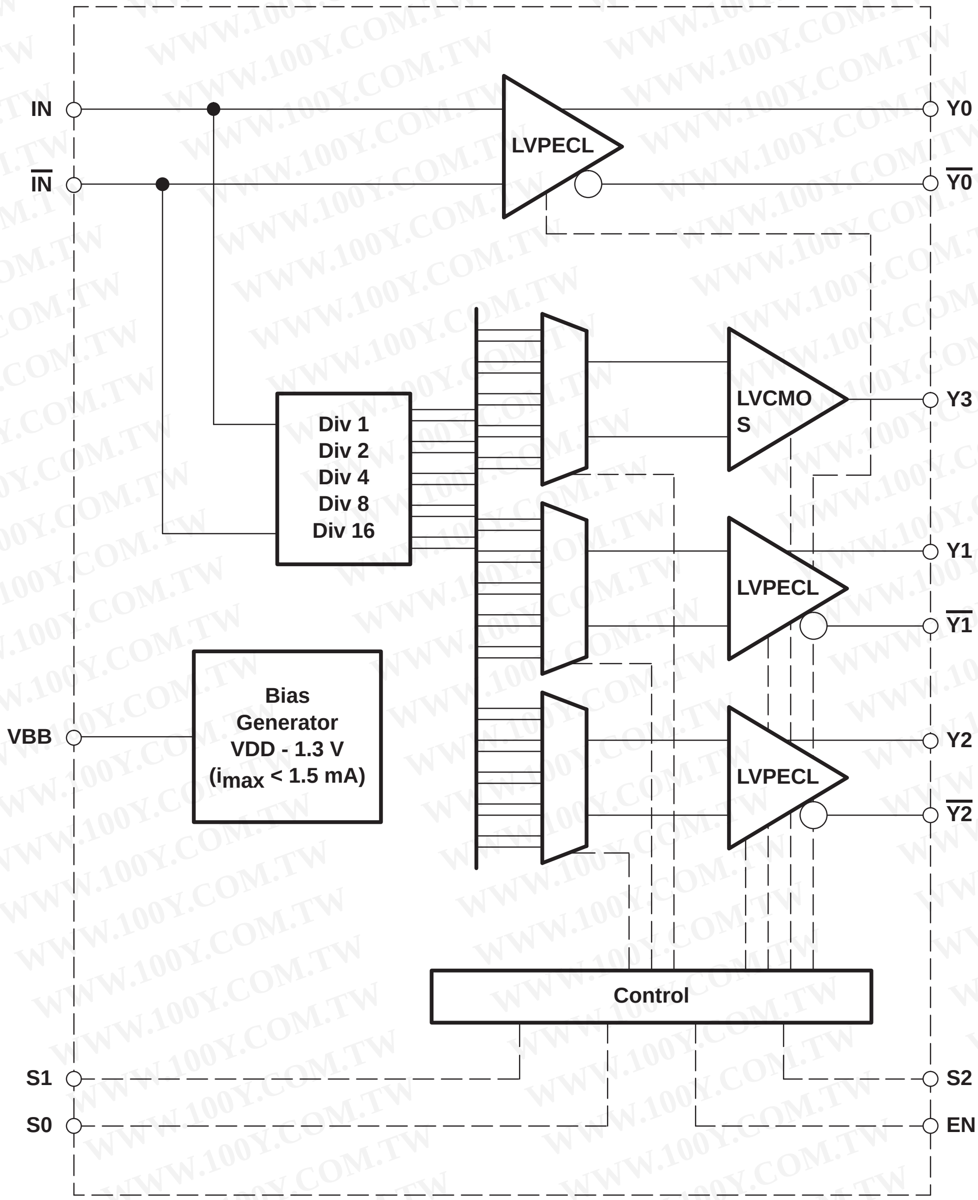
The CDCM1804 clock driver distributes one pair of differential clock inputs to three pairs of LVPECL differential clock outputs Y[2:0] and $\overline{\text{Y[2:0]}}$, with minimum skew for clock distribution. The CDCM1804 is specifically designed for driving 50-Ω transmission lines. Additionally, the CDCM1804 offers a single-ended LVCMOS output Y3. This output is delayed by 1.6 ns over the three LVPECL output stages to minimize noise impact during signal transitions.

The CDCM1804 has three control pins, S0, S1, and S2 to select different output mode settings. The S[2:0] pins are 3-level inputs and therefore allow up to 3^3=27 combinations. Additionally, an enable pin (EN) is provided to disable or enable all outputs simultaneously. The EN pin is a 3-level input as well and extends the number of settings to 2x27=54. See Table 1 for details.

The CDCM1804 is characterized for operation from −40°C to 85°C.

For use in single-ended driver applications, the CDCM1804 also provides a VBB output pin that can be directly connected to the unused input as a common-mode voltage reference.

functional block diagram



Terminal Functions

NAME	NO.	I/O	DESCRIPTION
EN	1	I (with 60-kΩ pullup)	ENABLE: Enables or disables all outputs simultaneously. The EN pin offers three different configurations: tight to GND (logic 0), external 60-kΩ pulldown resistor (pull to $V_{DD}/2$), or left floating (logic 1); EN=1: outputs on according to S0, S1, and S2 setting EN=$V_{DD}/2$: outputs on according to S[0:2] setting EN=0:outputs Y[3:0] off (high impedance) See Table 1 for details.
IN, $\overline{\text{IN}}$	3, 4	I (differential)	Differential input clock: Input stage is sensitive and has a wide common-mode range. Therefore, almost any type of differential signal can drive this input (LVPECL, LVDS, CML, HSTL). Since the input is high impedance, it is recommended to terminate the PCB transmission line before the input (e.g. with 100-Ω across input). Input can also be driven by single ended signal if the complementary input is tight to VBB. A more advanced scheme for single-ended signal is given in the application section near the end of this document. The inputs deploy an ESD structure protecting the inputs in case of an input voltage exceeding the rails by more than ~0.7 V. Reverse biasing of the IC through these inputs is possible and must be prevented by limiting the input voltage < V_{DD}.
S0, S1, S2	18, 19, 24	I (with 60-kΩ pullup)	Select mode of operation: Defines the output configuration of Y[3:0]. Each pin offers three different configurations: tight to GND (logic 0), external 60-kΩ pulldown resistor (pull to $V_{DD}/2$) or left floating (logic 1); see Table 1 for details.
Y3	12	O	LVCMOS clock output: This output provides copy of IN or down divided copy of clock IN based on selected mode of operation S[2:0]; Also, this output can be disabled by when $V_{DD}3$ becomes tight to GND.
Y[2:0], $\overline{\text{Y[2:0]}}$	9, 10, 15, 16, 21, 22	O (LVPECL)	LVPECL clock outputs: These outputs provide low-skew copies of IN or down divided copies of clock IN based on selected mode of operation S[2:0]; If an output is unused, the output can simply be left open to safe power and minimize noise impact to the remaining outputs.
VBB	6	O	Bias voltage output to be used to bias unused complementary input $\overline{\text{IN}}$ for single ended input signals. The output voltage of VBB is V_{DD} − 1.3 V. When driving a load, the output current drive is limited to about 1.5 mA.
V_{SS}	7	Supply	Device ground
V_{DD}PECL	2, 5	Supply	Supply voltage LVPECL input + internal logic
V_{DD} [2−0]	8, 11, 14, 17, 20, 23	Supply	LVPECL output supply voltage for output Y[0−2]: Each output can be disabled by pulling the corresponding V_{DD}x to GND. **CAUTION:** In this mode, no voltage from outside may be forced, because internal diodes could be forced in forward direction; Thus, it is recommended to disconnect the output.
$V_{DD}3$	13	Supply	Supply voltage LVCMOS output: The LVCMOS output can be disabled by pulling $V_{DD}3$ to GND. **CAUTION**: In this mode, no voltage from outside may be forced because internal diodes could be forced in a forward direction. Thus, it is recommended to leave Y3 unconnected, tight to GND, or terminated into GND.

control pin settings

The CDCM1804 has three control pins (S0, S1, and S2) and an enable pin (EN) to select different output mode settings. All four inputs (S0, S1, S2, and EN) are 3-level inputs offering 54 different combinations. In addition, the EN input allows the disabling of all outputs and forcing them into a high-z (or 3-state) output state when pulled to GND.

Each control input incorporates a 60-kΩ pullup resistor. Thus, it is easy to choose the input setting by designing a resistor pad between the control input and GND. To choose a logic zero, the resistor value must be zero. Setting the input high requires leaving the resistor pad empty (no resistor installed). For setting the input to $V_{DD}/2$, the installed resistor needs a value of 60-kΩ pulldown to GND with a tolerance better or equal 10%.

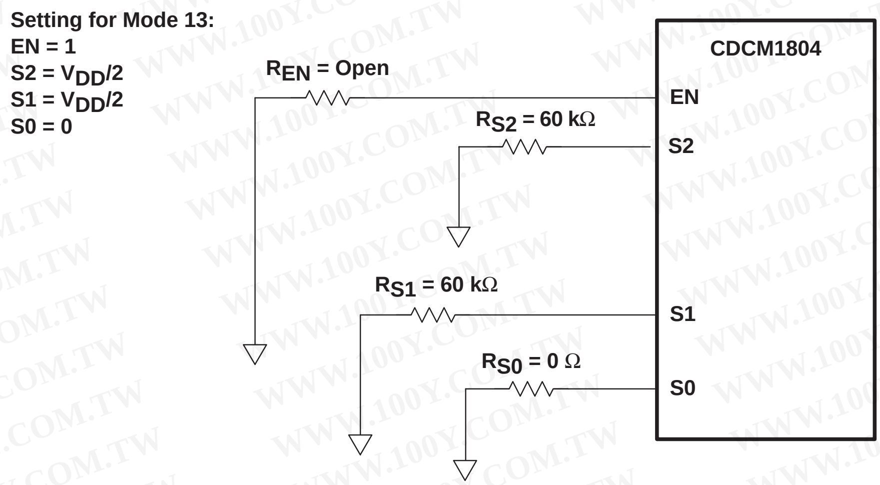


Figure 1. Control Pin Setting for Example

Table 1. Selection Mode Table

					LVPECL			LVCMOS
MODE	**EN**	**S2**	**S1**	**S0**	**Y0**	**Y1**	**Y2**	**Y3**
0	0	x	x	x	Off (high-z)			
1	1	0	0	0	÷ 1	÷ 1	÷ 1	Off (high-z)
2	1	0	0	$V_{DD}/2$	÷ 1	Off (high-z)	Off (high-z)	÷ 4
3	1	0	0	1	÷ 1	÷ 1	Off (high-z)	÷ 4
4	1	0	$V_{DD}/2$	0	÷ 1	÷ 2	Off (high-z)	÷ 4
5	1	0	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 4	Off (high-z)	÷ 4
6	1	0	$V_{DD}/2$	1	÷ 1	÷ 8	Off (high-z)	÷ 4
7	1	0	1	0	÷ 1	Off (high-z)	÷ 1	÷ 4
8	1	0	1	$V_{DD}/2$	÷ 1	÷ 1	÷ 1	÷ 4
9	1	0	1	1	÷ 1	÷ 2	÷ 1	÷ 4
10	1	$V_{DD}/2$	0	0	÷ 1	÷ 4	÷ 1	÷ 4
11	1	$V_{DD}/2$	0	$V_{DD}/2$	÷ 1	÷ 8	÷ 1	÷ 4
12	1	$V_{DD}/2$	0	1	÷ 1	Off (high-z)	÷ 2	÷ 4
13	1	$V_{DD}/2$	$V_{DD}/2$	0	÷ 1	÷ 1	÷ 2	÷ 4
14	1	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 2	÷ 2	÷ 4
15	1	$V_{DD}/2$	$V_{DD}/2$	1	÷ 1	÷ 4	÷ 2	÷ 4
16	1	$V_{DD}/2$	1	0	÷ 1	÷ 8	÷ 2	÷ 4
17	1	$V_{DD}/2$	1	$V_{DD}/2$	÷ 1	Off (high-z)	÷ 4	÷ 4
18	1	$V_{DD}/2$	1	1	÷ 1	÷ 1	÷ 4	÷ 4
19	1	1	0	0	÷ 1	÷ 2	÷ 4	÷ 4
20	1	1	0	$V_{DD}/2$	÷ 1	÷ 4	÷ 4	÷ 4
21	1	1	0	1	÷ 1	÷ 8	÷ 4	÷ 4
22	1	1	$V_{DD}/2$	0	÷ 1	Off (high-z)	÷ 8	÷ 4
23	1	1	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 1	÷ 8	÷ 4
24	1	1	$V_{DD}/2$	1	÷ 1	÷ 2	÷ 8	÷ 4
25	1	1	1	0	÷ 1	÷ 4	÷ 8	÷ 4
26	1	1	1	$V_{DD}/2$	÷ 1	÷ 8	÷ 8	÷ 4

27	1	1	1	1	÷ 1	Off (high-z)	÷ 16	÷ 4
28	$V_{DD}/2$	0	0	0	÷ 1	÷ 1	÷ 16	÷ 4
29	$V_{DD}/2$	0	0	$V_{DD}/2$	÷ 1	÷ 2	÷ 16	÷ 4
30	$V_{DD}/2$	0	0	1	÷ 1	÷ 4	÷ 16	÷ 4
31	$V_{DD}/2$	0	$V_{DD}/2$	0	÷ 1	÷ 8	÷ 16	÷ 4
32	$V_{DD}/2$	0	$V_{DD}/2$	$V_{DD}/2$	÷ 1	Off (high-z)	Off (high-z)	÷ 1
33	$V_{DD}/2$	0	$V_{DD}/2$	1	÷ 1	÷ 1	Off (high-z)	÷ 1
34	$V_{DD}/2$	0	1	0	÷ 1	÷ 2	Off (high-z)	÷ 1
35	$V_{DD}/2$	0	1	$V_{DD}/2$	÷ 1	÷ 1	Off (high-z)	÷ 2
36	$V_{DD}/2$	0	1	1	÷ 1	÷ 2	Off (high-z)	÷ 2
37	$V_{DD}/2$	$V_{DD}/2$	0	0	÷ 1	Off (high-z)	Off (high-z)	÷ 2
38	$V_{DD}/2$	$V_{DD}/2$	0	$V_{DD}/2$	÷ 1	÷ 1	÷ 1	÷ 2
39	$V_{DD}/2$	$V_{DD}/2$	0	1	÷ 1	÷ 2	÷ 8	÷ 2
40	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	0	÷ 1	÷ 2	÷ 8	÷ 8
41	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 4	Off (high-z)	÷ 1
42	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	1	÷ 1	÷ 8	Off (high-z)	÷ 1
43	$V_{DD}/2$	$V_{DD}/2$	1	0	÷ 1	÷ 4	Off (high-z)	÷ 2
44	$V_{DD}/2$	$V_{DD}/2$	1	$V_{DD}/2$	÷ 1	÷ 8	Off (high-z)	÷ 2
45	$V_{DD}/2$	$V_{DD}/2$	1	1	÷ 1	÷ 1	÷ 2	÷ 2
46	$V_{DD}/2$	1	0	0	÷ 1	Off (high-z)	Off (high-z)	÷ 8
47	$V_{DD}/2$	1	0	$V_{DD}/2$	÷ 1	÷ 4	Off (high-z)	÷ 8
48	$V_{DD}/2$	1	0	1	÷ 1	÷ 4	÷ 8	÷ 8
49	$V_{DD}/2$	1	$V_{DD}/2$	0	÷ 1	÷ 8	Off (high-z)	÷ 8
50	$V_{DD}/2$	1	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 2	÷ 8	÷ 16
Rsv	$V_{DD}/2$	1	$V_{DD}/2$	1	Reserved	Reserved	Reserved	Reserved
Rsv	$V_{DD}/2$	1	1	0	N/A	Low	Low	Low
53	$V_{DD}/2$	1	1	$V_{DD}/2$	÷ 1	÷ 1	÷ 1	÷ 1
54	$V_{DD}/2$	1	1	1	÷ 1	÷ 1	÷ 1	÷ 1

NOTE: The LVPECL outputs are open emitter stages. Thus, if you leave the unused LVPECL outputs Y0, Y1, or Y2 unconnected, then the current consumption is minimized and noise impact to remaining outputs is neglectable. Also, each output can be individually disabled by connecting the corresponding V_{DD} input to GND.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} . . . −0.3 V to 3.8 V
Input voltage, V_I . . . −0.2 V to (V_{DD} +0.2 V)
Output voltage, V_O . . . −0.2 V to (V_{DD} +0.2 V)
Differential short circuit current, Yn, $\overline{Yn}$, I_{OSD} . . . Continuous
Electrostatic discharge (HBM 1.5 kΩ, 100 pF), ESD . . . >2000 V
Moisture level 24-pin MLF package (solder reflow temperature of 235°C) MSL . . . 2
Storage temperature, T_{stg} . . . −65°C to 150°C
Maximum junction temperature, T_J . . . 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

LVPECL input IN, $\overline{IN}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Input frequency		0		800	MHz
V_{CM}	High-level input common mode		1		V_{DD}−0.3	V
V_{IN}	Input voltage swing between IN and $\overline{IN}$, see Note 1		500		1300	mV
V_{IN}	Input voltage swing between IN and $\overline{IN}$, see Note 2		150		1300	mV
I_{IN}	Input current	$V_I = V_{DD}$ or 0 V			±10	µA
R_{IN}	Input impedance		300			kΩ
C_I	Input capacitance at IN, $\overline{IN}$			1		pF

NOTES: 1. Is required to maintain ac specifications
2. Is required to maintain device functionality

LVPECL output driver Y[2:0], $\overline{Y[2:0]}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Output frequency, see Figure 4		0		800	MHz
V_{OH}	High-level output voltage	Termination with 50 Ω to V_{DD}−2 V	V_{DD}−1.18		V_{DD}−0.81	V
V_{OL}	Low-level output voltage	Termination with 50 Ω to V_{DD}−2 V	V_{DD}−1.98		V_{DD}−1.55	V
V_O	Output voltage swing between Y and $\overline{Y}$, see Figure 4	Termination with 50 Ω to V_{DD}−2 V	500			mV
I_{OZL}	Output 3-state	V_{DD} = 3.6 V, V_O = 0 V			5	µA
I_{OZH}	Output 3-state	V_{DD} = 3.6 V, $V_O = V_{DD}$ − 0.8 V			10	µA
t_r/t_f	Rise and fall time	20% to 80% of V_{OUTPP}, see Figure 9	200		350	ps
$t_{skpecl(o)}$	Output skew between any LVPECL output Y[2−0] and $\overline{Y[2-0]}$	See Note A in Figure 8		15	30	ps
t_{Duty}	Output duty cycle distortion, see Note 3	Crossing point-to-crossing point distortion	−50		50	ps
$t_{sk(pp)}$	Part-to-part skew	Any Y, See Note B in Figure 8		50		ps
C_O	Output capacitance	$V_O = V_{DD}$ or GND		1		pF
LOAD	Expected output load			50		Ω

NOTES: 3. For a 800-MHz signal, the 50-ps error would result into a duty cycle distortion of ±4% when driven by an ideal clock input signal.

LVPECL input-to-LVPECL output parameter

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(lh)}$	Propagation delay rising edge	VOX to VOX	320		600	ps
$t_{pd(hl)}$	Propagation delay falling edge	VOX to VOX	320		600	ps
$t_{sk(p)}$	LVPECL pulse skew	VOX to VOX, See Note C in Figure 8			100	ps

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

LVCMOS output parameter, Y3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clk}	OUTPUT frequency, see Note 1 and Figure 5			0		200	MHz
$t_{skLVCMOS(o)}$	Output skew between the LVCMOS output Y3 and LVPECL outputs Y[2−0]	VOX to V_{DD}/2, See Figure 8			1.6		ns
$t_{sk(pp)}$	Part-to-part skew	Y3, See Note B in Figure 8			300		ps
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = −100 µA	V_{DD}–0.1			V
		V_{DD} = 3 V,	I_{OH} = −6 mA	2.4			
		V_{DD} = 3 V,	I_{OH} = −12 mA	2			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL}=100 µA			0.1	V
		V_{DD} = 3 V,	I_{OL} = 6 mA			0.5	
		V_{DD} = 3 V,	I_{OL} = 12 mA			0.8	
I_{OH}	High-level output current	V_{DD} = 3.3 V,	V_O = 1.65 V		−29		mA
I_{OL}	Low-level output current	V_{DD} = 3.3 V,	V_O = 1.65 V		37		mA
I_{OZ}	High-impedance state output current	V_{DD} = 3.6 V,	V_O = V_{DD} or 0 V			±5	µA
C_O	Output capacitance	V_{DD} = 3.3 V			2		pF
t_{Duty}	Output duty cycle distortion, see Note 2	Measured at V_{DD}/2		−150		150	ps
$t_{pd(lh)}$	Propagation delay rising edge from IN to Y3	VOX to V_{DD}/2 load, see Figure 10		1.6		2.6	ns
$t_{pd(hl)}$	Propagation delay falling edge from IN to Y3	VOX to V_{DD}/2 load, see Figure 10		1.6		2.6	ns
t_r	Output rise slew rate	20% to 80% of swing see Figure 10		1.4	2.3		V/ns
t_f	Output fall slew rate	80% to 20% of swing see Figure 10		1.4	2.3		V/ns

NOTES: 1. Operating the CDCM1804 LVCMOS output above the maximum frequency will not cause a malfunction to the device, but the Y3 output signal swing will not achieve enough signal swing to meet the output spec. Therefore, the CDCM1804 can be operated at higher frequencies, while the LVCMOS output Y3 becomes unusable.
2. For a 200-MHz signal, the 150-ps error would result in a duty cycle distortion of ±3% when driven by an ideal clock input signal.

jitter characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{jitterLVPECL}$	Additive phase jitter from input to LVPECL output [Y2−0], see Figure 2	12 kHz to 20 MHz, f_{out} = 250 MHz to 800 MHz, divide by 1 mode			0.15	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz to 800 MHz, divide by 1 mode			0.25	ps rms
$t_{jitterLVCMOS}$	Additive phase jitter from input to LVCMOS output Y3 see Figure 3	12 kHz to 20 MHz, f_{out} = 250 MHz, divide by 1 mode			0.25	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz, divide by 1 mode			0.4	ps rms

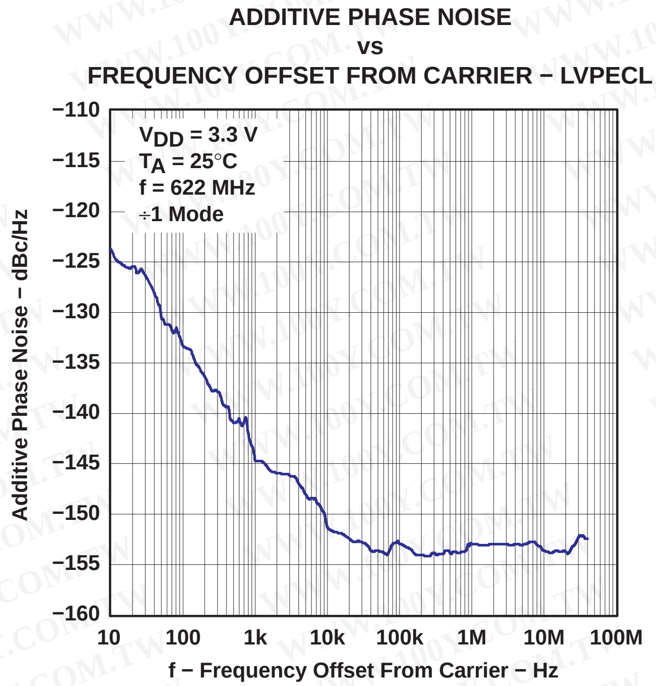


Figure 2.

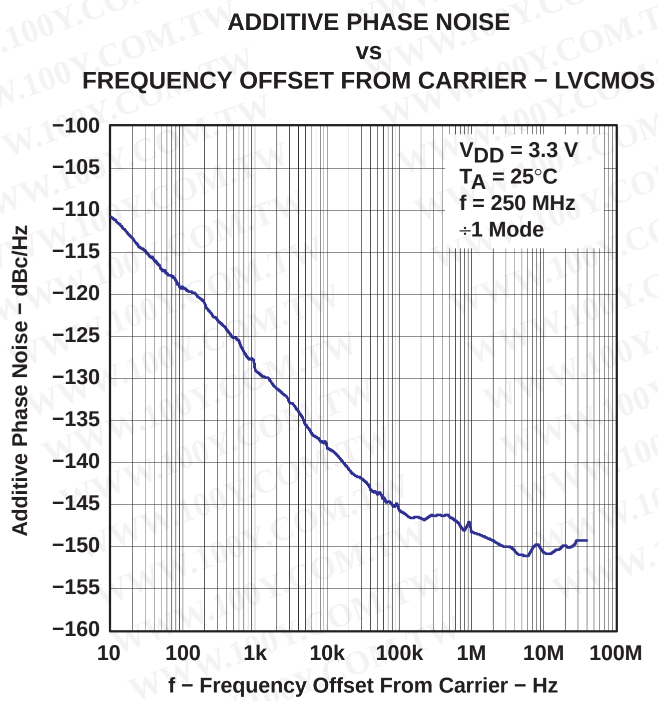


Figure 3.

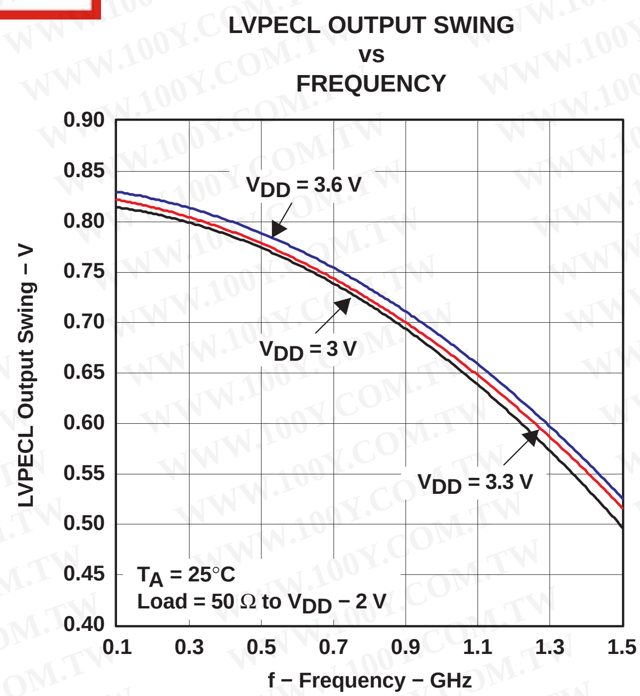


Figure 4.

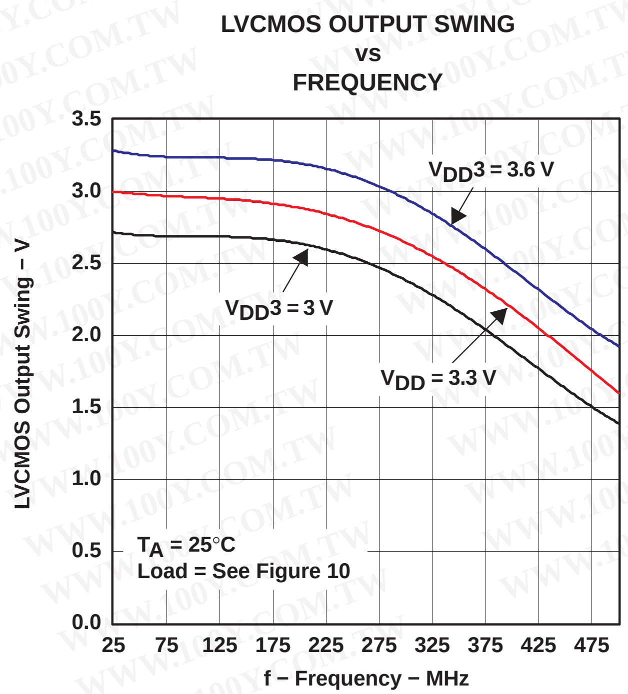


Figure 5.

supply current electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Supply current	Full load	All outputs enabled and terminated with 50 Ω to V_{DD} − 2 V on LVPECL outputs and 10 pF on LVCMOS output, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS V_{DD} = 3.3 V		160		mA
		No load	Outputs enabled, no output load, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS V_{DD} = 3.6 V			110	mA
I_{DD}	Supply current saving per LVPECL output stage disabled, no load		f = 800 MHz for LVPECL output, V_{DD} = 3.3 V		10		mA
I_{DDZ}	Supply current, tri-state		All outputs 3-state by control logic, f = 0 Hz, V_{DD} = 3.6 V			0.5	mA

SUPPLY CURRENT
vs
FREQUENCY

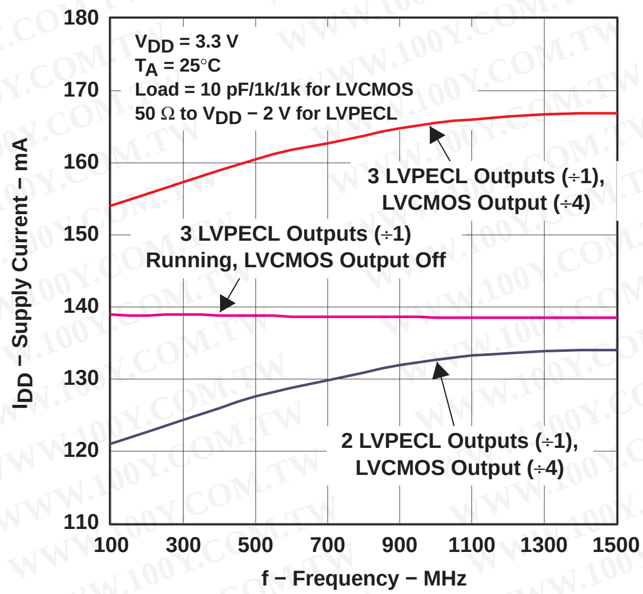


Figure 6.

package thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA-1}	MLF−24 package thermal resistance, See Note 1	4-layer JEDEC test board (JESD51−7), airflow = 0 ft/min		106.6		°C/W
θ_{JA-2}	MLF−24 package thermal resistance with thermal vias in PCB, See Note 1	4-layer JEDEC test board (JESD51−7) with four thermal vias of 22-mil diameter each, airflow = 0 ft/min		55.4		°C/W

NOTE 1: It is recommended to provide four thermal vias to connect the thermal pad of the package effectively with the PCB and ensure a good heat sink.

Example:

calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

$T_{Chassis}$ = 85°C (temperature of the chassis)

$P_{effective} = I_{max} \times V_{max}$ = 110 mA x 3.6 V = 396 mW (max power consumption inside the package)

$\theta T_{Junction} = \theta_{JA-2} \times P_{effective}$ = 55.45°C/W x 396 mW = 21.96°C

$T_{Junction} = \theta T_{Junction} + T_{Chassis}$ = 21.96°C + 85°C = 107°C (the maximum junction temperature of $T_{die-max}$ = 125°C is not violated)

control input characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{su}	Setup time, S0, S1, S2, and EN pin before clock IN		25			ns
t_h	Hold time, S0, S1, S2, and EN pin after clock IN		0			ns
$t_{(disable)}$	Time between latching the EN low transition and when all outputs are disabled (how much time is required until the outputs turn off)			10		ns
$t_{(enable)}$	Time between latching the EN low-to-high transition and when outputs are enabled based on control settings (how much time passes before the outputs carry valid signals)			1		µs
Rpullup	Internal pullup resistor on S[2:0] and EN input		42	60	78	kΩ
$V_{IH(H)}$	Three level input high, S0, S1, S2, and EN pin, see Note 1		$0.9xV_{DD}$			V
$V_{IM(M)}$	Three level input MID, S0, S1, S2, and EN pin		$0.3xV_{DD}$		$0.7xV_{DD}$	V
$V_{IL(L)}$	Three level low, S0, S1, S2, and EN pin				$0.1xV_{DD}$	V
I_{IH}	Input current, S0, S1, S2, and EN pin	$V_I = V_{DD}$			−5	µA
I_{IL}	Input current, S0, S1, S2, and EN pin	V_I = GND	38		85	µA

NOTES: 1. Leaving this pin floating automatically pulse the logic level high to V_{DD} through an internal pullup resistor of 60 kΩ.

bias voltage VBB over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
VBB	Output reference voltage	V_{DD} = 3 V − 3.6 V, I_{BB} = −0.2 mA	V_{DD} − 1.4		V_{DD} − 1.2	V

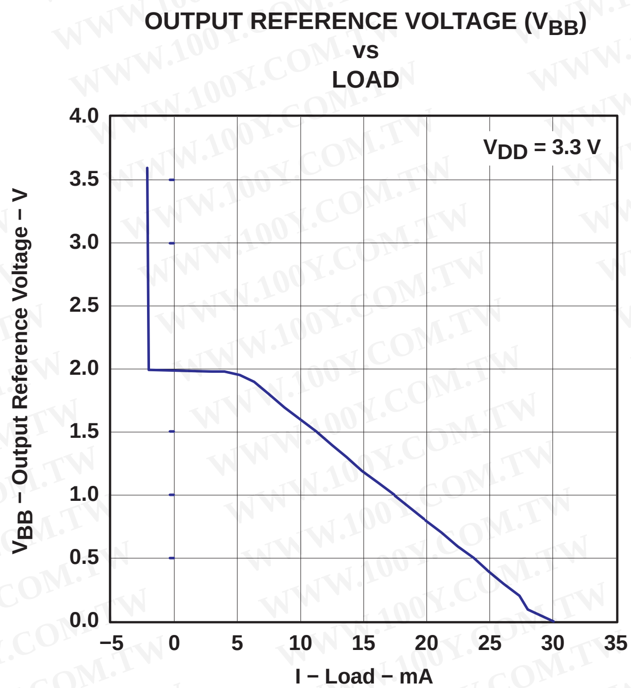
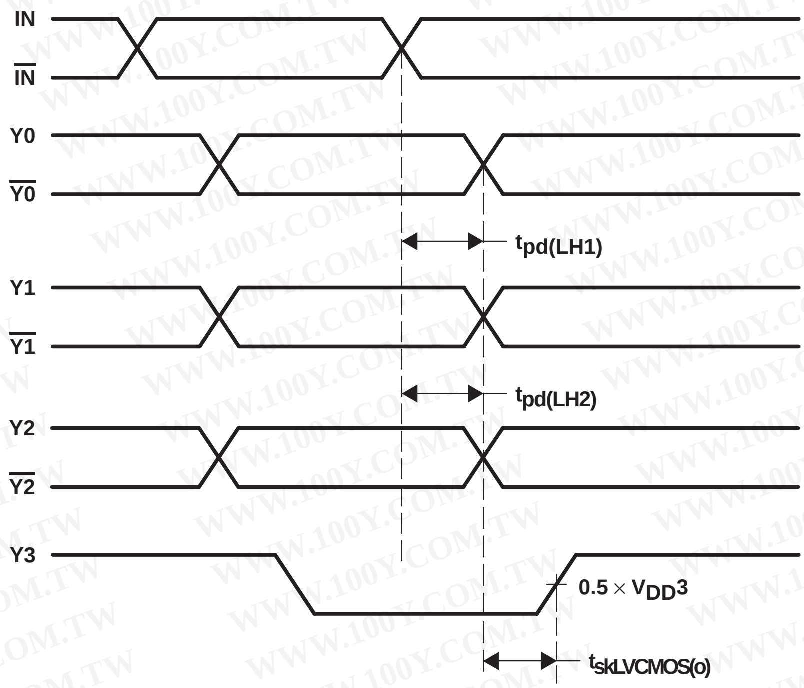

OUTPUT REFERENCE VOLTAGE (V_{BB})
vs
LOAD
V_{DD} = 3.3 V
V_{BB} − Output Reference Voltage − V
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
−5
0
5
10
15
20
25
30
35
I − Load − mA

Figure 7.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and the slowest $t_{pd(LH)n}$ (n = 0…2)
- The difference between the fastest and the slowest $t_{pd(HL)n}$ (n = 0…2)

B. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
- The difference between the fastest and the slowest $t_{pd(LH)n}$ (n = 0…2 for LVPECL, n = 3 for LVCMOS) across multiple devices
- The difference between the fastest and the slowest $t_{pd(HL)n}$ (n = 0…2 for LVPECL, n = 3 for LVCMOS) across multiple devices

C. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low ($t_{pd(HL)}$) and the low-to-high ($t_{pd(LH)}$) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)} = | t_{pd(HL)} - t_{pd(LH)} |$. Pulse skew is sometimes referred to as *pulse width distortion or duty cycle skew.*

Figure 8. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$

PARAMETER MEASUREMENT INFORMATION

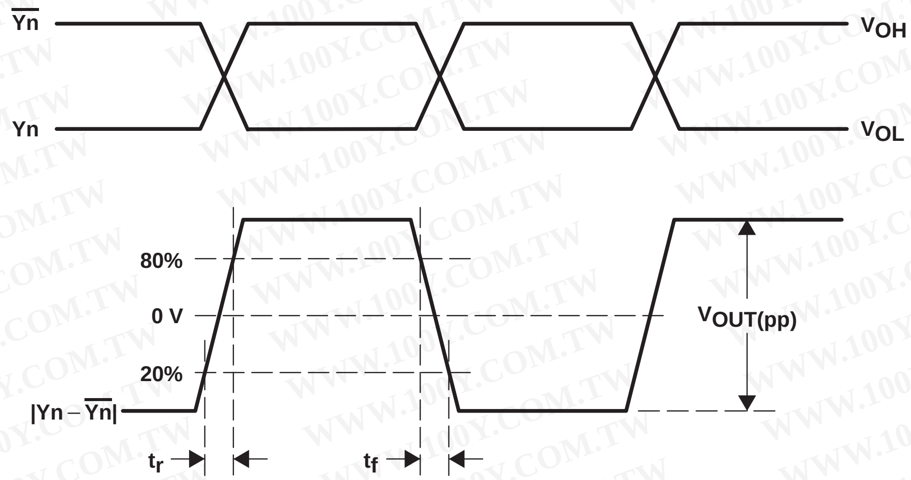


Figure 9. LVPECL Differential Output Voltage and Rise/Fall Time

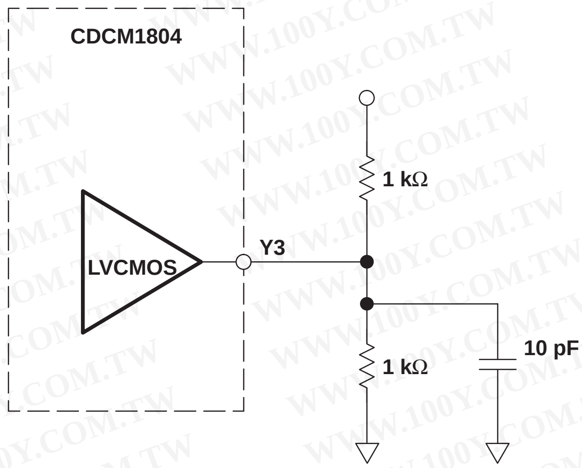


Figure 10. LVCMOS Output Loading During Device Test

PCB design for thermal functionality

It is recommended to take special care of the PCB design for good thermal flow from the MLF-24 pin package to the PCB.

Due to the three LVPECL outputs, the current consumption of the CDCM1804 is fixed.

JEDEC JESD51-7 specifies thermal conductivity for standard PCB boards.

Modeling the CDCM1804 with a standard 4-layer JEDEC board results into a 67.22°C max temperature with a θ_{JA} of 106.62°C/W for 25°C ambient temperature.

When deploying four thermal vias (one per quadrant), the thermal flow improves significantly, yielding 46.94°C max temperature with a θ_{JA} of 55.4°C/W for 25°C ambient temperature.

To ensure sufficient thermal flow, it is recommended to design with four thermal vias in applications enabling all four outputs at ones.

PARAMETER MEASUREMENT INFORMATION

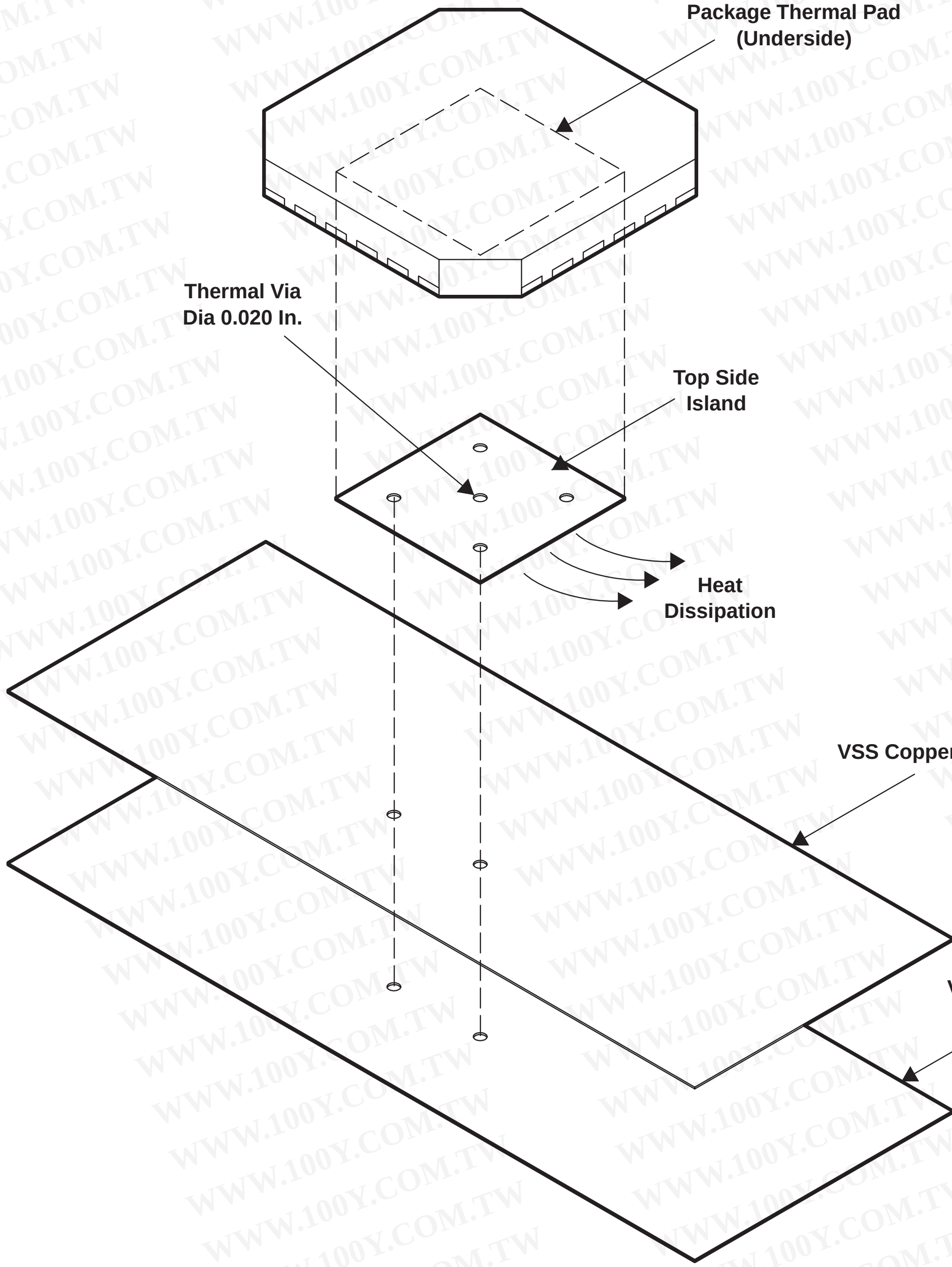


Figure 11. Recommended Thermal Via Placement

See the SCBA017 and the SLUA271 application notes for further package related information.

APPLICATION INFORMATION

LVPECL receiver input termination

The input of the CDCM1804 has a high impedance and comes with a large common-mode voltage range.

For optimized noise performance, it is recommended to properly terminate the PCB trace (transmission line). If a differential signal drives the CDCM1804, then a 100-Ω termination resistor is recommended to be placed as close as possible across the input pins. An even better approach is to install 2x 50 Ω, with the center tap connected to a capacitor (C) to terminate odd-mode noise and make up for transmission line mismatches. The VBB output can also be connected to the center tap to bias the input signal to (V_{DD} − 1.3 V) (see Figure 12).

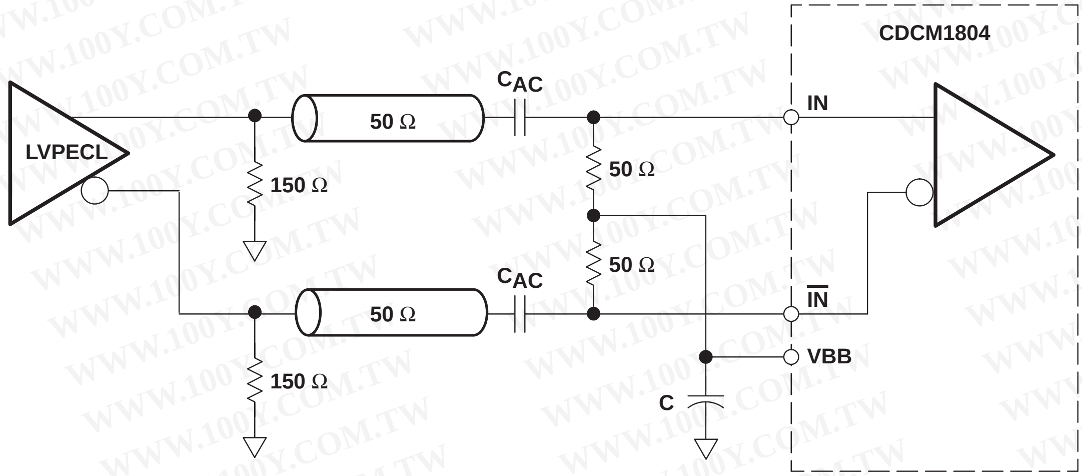


Figure 12. Recommended AC-Coupling LVPECL Receiver Input Termination

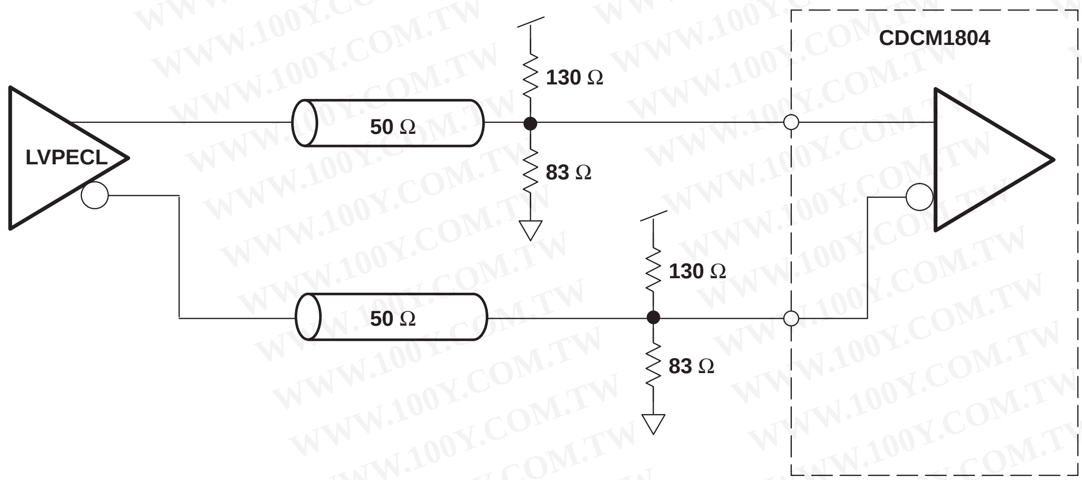
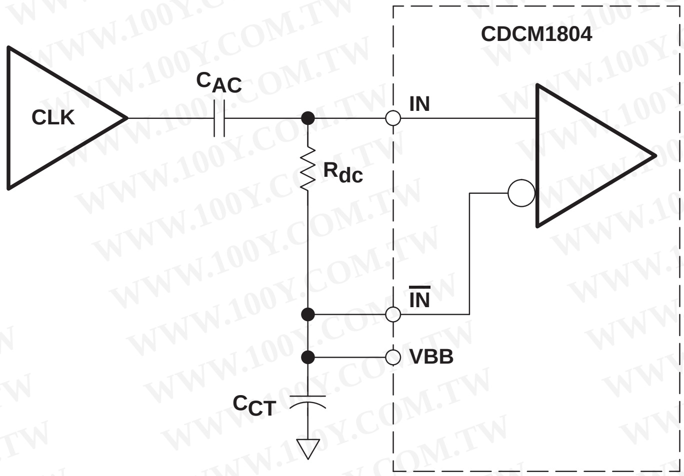


Figure 13. Recommended DC-Coupling LVPECL Receiver Input Termination

APPLICATION INFORMATION

The CDCM1804 can also be driven by single-ended signals. Typically, the input signal becomes connected to one input, while the complementary input must be properly biased to the center voltage of the incoming input signal. For LVCMOS signals, this would be $V_{CC}/2$, realized by a simple voltage divider (e.g. two 10-kΩ resistors). The best options (especially if the dc offset of the input signal might vary) are to ac-couple the input signal and then rebias the signal using the VBB reference output. See Figure 14.



NOTE: C_{AC} − AC-coupling capacitor (e.g., 10 nF)
C_{CT} − Capacitor keeps voltage at $\overline{IN}$ constant (e.g., 10 nF)
R_{dc} − Load and correct duty cycle (e.g., 50 Ω)
V_{BB} − Bias voltage output

Figure 14. Typical Application Setting for Single-Ended Input Signals Driving the CDCM1804

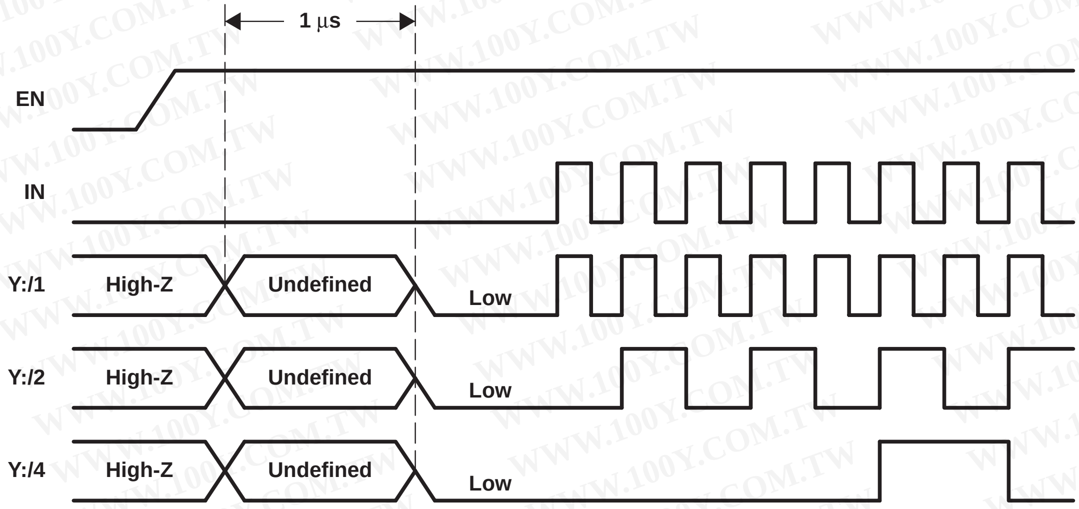
APPLICATION INFORMATION

device behavior during RESET and control pin switching

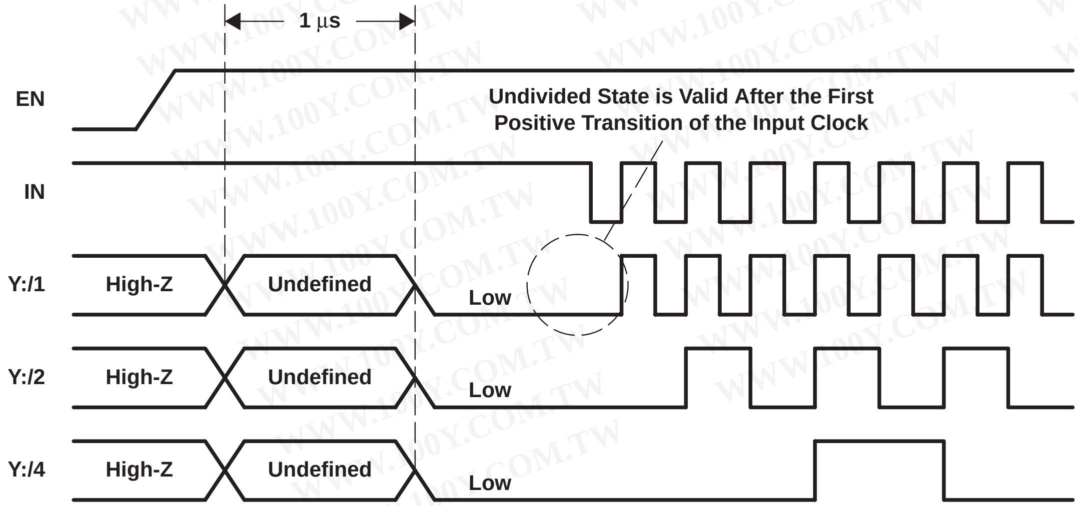
output behavior from enabling the device (EN=0 ⇒ 1)

In disable mode (EN=0), all output drivers are switched in high-Z mode. The S[0:2] control inputs are also switched off. In the same mode, all flip-flops are reset. The typical current consumption is below 500 µA.

When the device is enabled again, it takes typically 1 µs for the settling of the reference voltage and currents. During this time, the outputs Y[0:2] and $\overline{Y[0:2]}$ drive a high signal. Y3 is unknown (could be high or low). After the settle time, the outputs go into the low state. Due to the synchronization of each output driver signal with the input clock, the state of the waveforms after enabling the device looks like shown in Figure 15. The inverting input and output signal is not included. The Y:/1 waveform is the undivided output driver state.



Signal State After the Device is Enabled (IN = Low)



Signal State After the Device is Enabled (IN = High)

Figure 15. Waveforms

APPLICATION INFORMATION

enabling a single output stage

If a single output stage becomes enabled:

- Y[0:2] will either be low or high (undefined).
- $\overline{\text{Y[0:2]}}$ will be the inverted signal of Y[0:2].

With the first positive clock transition the undivided output becomes the input clock state. The divided output states are equal to the actual internal divider. The internal divider doesn't get reset while enabling single output drivers.

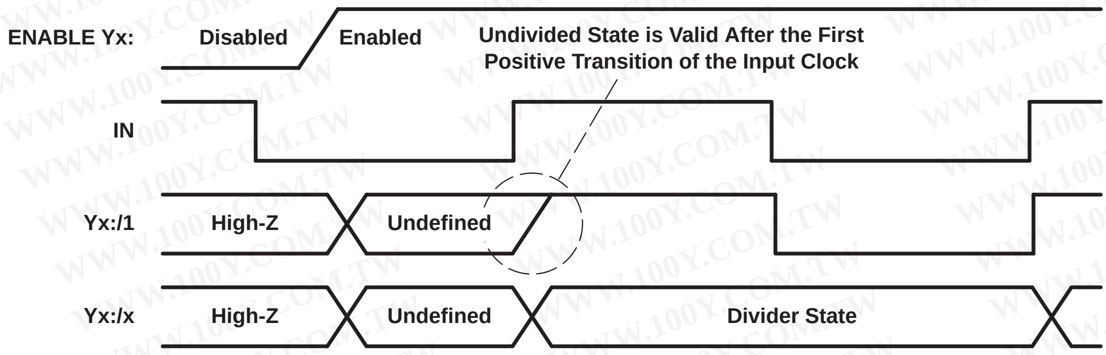


Figure 16. Signal State After an Output Driver Becomes Enabled While IN = 0

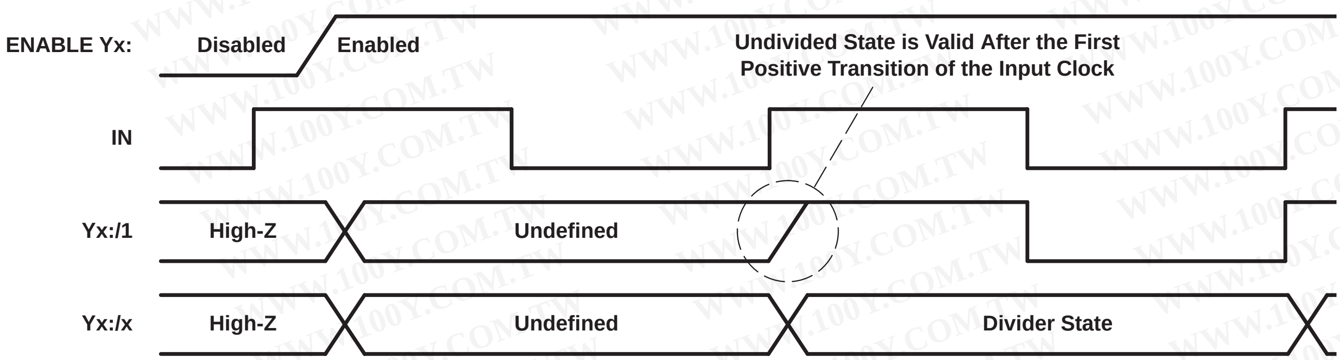
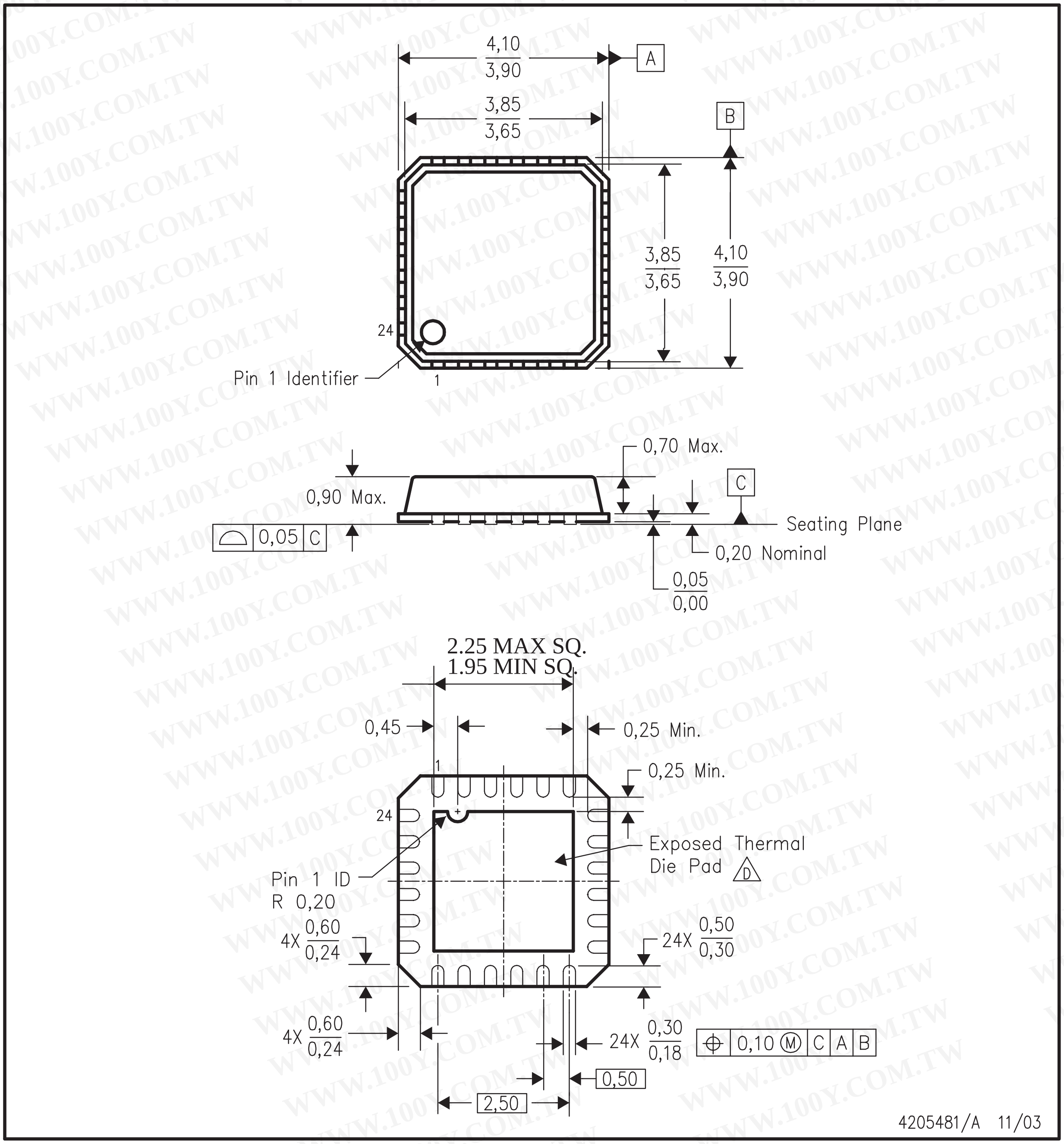


Figure 17. Signal State After an Output Driver Becomes Enabled While IN = 1

MECHANICAL DATA

RTH (S−PQFP−N24) **PLASTIC QUAD FLATPACK**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No−Lead) Package configuration.
D. The Package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad may be electrically connected to ground.