

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

CD74HC390, CD74HCT390

High Speed CMOS Logic Dual Decade Ripple Counter

Features

- Two BCD Decade or Bi-Quinary Counters
- One Package Can Be Configured to Divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two Master Reset Inputs to Clear Each Decade Counter Individually
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The Harris CD74HC390 and CD74HCT390 dual 4-bit decade ripple counters are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL). These devices are divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clock inputs (nCP0 and nCP1) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100. Each section is triggered by the High-to-Low transition of the input pulses (nCP0 and nCP1).

For BCD decade operation, the nQ0 output is connected to the nCP1 input of the divide-by-5 section. For bi-quinary decade operation, the nQ3 output is connected to the nCP0 input and nQ0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active-High asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A High level on the nMR input overrides the clock and sets the four outputs Low.

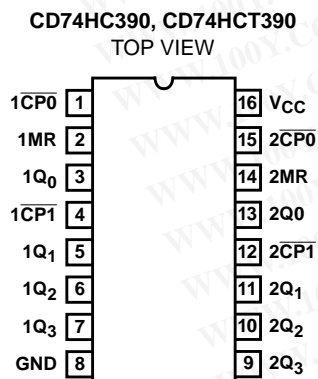
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC390E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT390E	-55 to 125	16 Ld PDIP	E16.3
CD74HC390M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT390M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

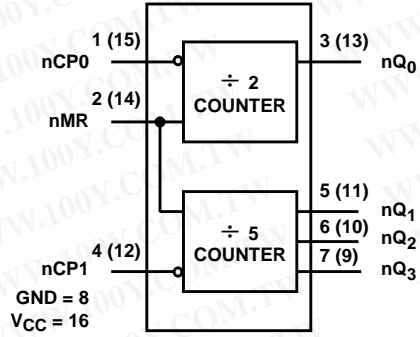
Pinout



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Functional Diagram



TRUTH TABLE

INPUTS		ACTION
CP	MR	
↑	L	No Change
↓	L	Count
X	H	All Qs Low

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care,
 ↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

BCD COUNT SEQUENCE FOR 1/2 THE 390

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output nQ0 connected to nCP1 with counter input on nCP0.

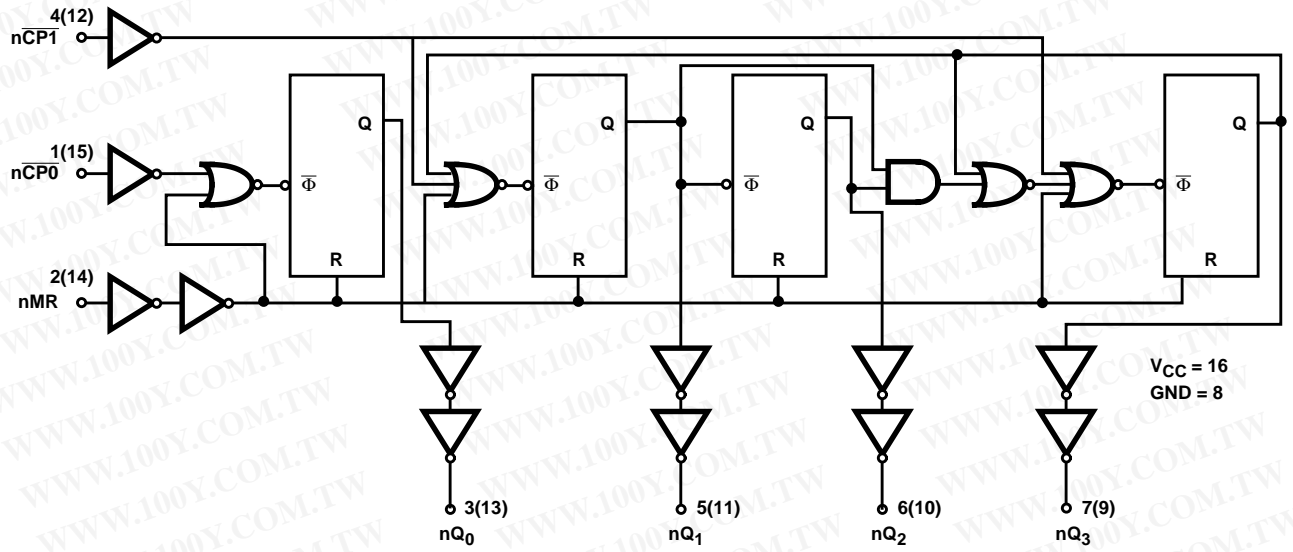
B-QUINARY COUNT SEQUENCE FOR 1/2 THE 390

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	H	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

NOTE: Output nQ3 connected to nCP0 with counter input on nCP1.

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Logic Diagram



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Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	90
SOIC Package	190
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A)	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

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CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA

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DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
nCP0	0.45
nCP1, MR	0.6

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NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Prerequisite for Switching Specifications

CHARACTERISTIC	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
Maximum Clock Frequency	f _{MAX}	2	6	-	-	5	-	4	-	MHz
		4.5	30	-	-	24	-	20	-	MHz
		6	35	-	-	28	-	24	-	MHz
Clock Pulse Width, nCP0, nCP1	t _w	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Reset Removal Time	t _{REM}	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns

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Prerequisite for Switching Specifications (Continued)

CHARACTERISTIC	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Reset Pulse Width	t _W	2	50	-	-	65	-	75	-	ns
		4.5	10	-	-	13	-	15	-	ns
		6	9	-	-	11	-	13	-	ns
HCT TYPES										
Maximum Clock Frequency	f _{MAX}	4.5	27	-	-	22	-	18	-	MHz
Clock Pulse Width, nCP0, nCP1	t _W	4.5	19	-	-	24	-	29	-	ns
Reset Removal Time	t _{REM}	4.5	15	-	-	19	-	22	-	ns
Reset Pulse Width	t _W	4.5	13	-	-	16	-	20	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay (Figure 1) nCP0 to nQ0	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	30	-	37	-	45	ns
nCP1 to nQ1	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
			6	-	-	31	-	39	-	48	ns
nCP1 to nQ2	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	245	-	305	-	370	ns
			4.5	-	-	49	-	61	-	74	ns
			6	-	-	42	-	52	-	63	ns
nCP1 to nQ3	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
			5	-	15	-	-	-	-	-	ns
			6	-	-	31	-	38	-	46	ns
nCP0 to nQ3 (nQ0 connected to nCP1)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	365	-	455	-	550	ns
			4.5	-	-	73	-	91	-	110	ns
			6	-	-	62	-	77	-	94	ns
MR to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	190	-	240	-	285	ns
			4.5	-	-	38	-	48	-	57	ns
		C _L = 15pF	5	-	16	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	32	-	41	-	48	ns
Output Transition Time (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	C _L = 15pF	5	-	28	-	-	-	-	-	pF

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Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES											
Propagation Delay (Figure 1) $n\overline{CP}0$ to nQ_0	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	40	-	50	-	60	ns
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	-	ns
$n\overline{CP}1$ to nQ_1	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	43	-	51	-	65	ns
$n\overline{CP}1$ to nQ_2	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
$n\overline{CP}1$ to nQ_3	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
$n\overline{CP}0$ to nQ_2 (nQ_0 connected to $n\overline{CP}1$)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	84	-	105	-	126	ns
MR to Q_n	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
Output Transition	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	$C_L = 15\text{pF}$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	$C_L = 15\text{pF}$	5	-	32	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per multiplexer.
5. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

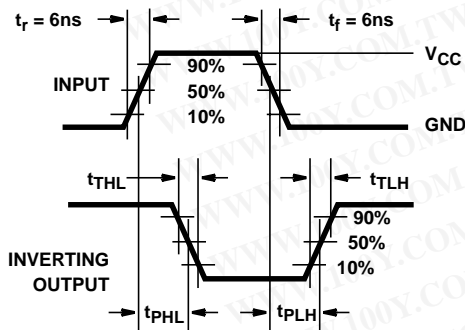


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

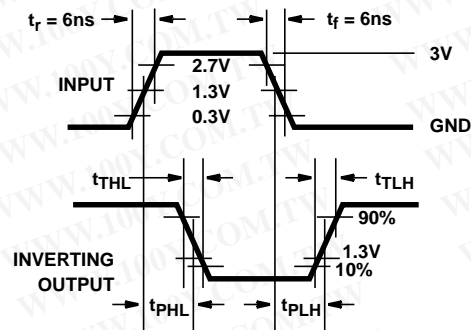


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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