

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
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**FAIRCHILD**  
 SEMICONDUCTOR™

October 1987  
 Revised May 1999

## CD4047BC Low Power Monostable/Astable Multivibrator

### General Description

The CD4047B is capable of operating in either the monostable or astable mode. It requires an external capacitor (between pins 1 and 3) and an external resistor (between pins 2 and 3) to determine the output pulse width in the monostable mode, and the output frequency in the astable mode.

Astable operation is enabled by a high level on the astable input or low level on the astable input. The output frequency (at 50% duty cycle) at Q and  $\bar{Q}$  outputs is determined by the timing components. A frequency twice that of Q is available at the Oscillator Output; a 50% duty cycle is not guaranteed.

Monostable operation is obtained when the device is triggered by LOW-to-HIGH transition at + trigger input or HIGH-to-LOW transition at - trigger input. The device can be retriggered by applying a simultaneous LOW-to-HIGH transition to both the + trigger and retrigger inputs.

A high level on Reset input resets the outputs Q to LOW,  $\bar{Q}$  to HIGH.

### Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity:  $0.45 V_{DD}$  (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS

#### SPECIAL FEATURES

- Low power consumption: special CMOS oscillator configuration
- Monostable (one-shot) or astable (free-running) operation

- True and complemented buffered outputs
- Only one external R and C required

#### MONOSTABLE MULTIVIBRATOR FEATURES

- Positive- or negative-edge trigger
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse width expansion
- Long pulse widths possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

#### ASTABLE MULTIVIBRATOR FEATURES

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available
- Good astable frequency stability  
 typical=  $\pm 2\% + 0.03\%/^{\circ}\text{C}$  @ 100 kHz  
 frequency=  $\pm 0.5\% + 0.015\%/^{\circ}\text{C}$  @ 10 kHz  
 deviation (circuits trimmed to frequency  $V_{DD} = 10\text{V}$   $\pm 10\%$ )

### Applications

- Frequency discriminators
- Timing circuits
- Time-delay applications
- Envelope detection
- Frequency multiplication
- Frequency division

### Ordering Code:

Order Number	Package Number	Package Description
CD4047BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
CD4047BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

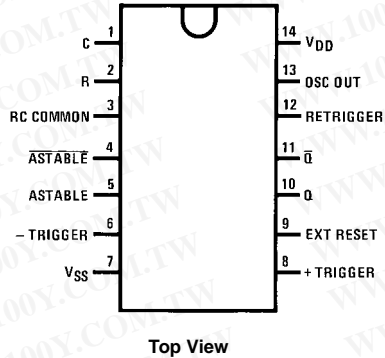
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## Connection Diagram

Pin Assignments for SOIC and DIP



## Function Table

Function	Terminal Connections			Output Pulse From	Typical Output Period or Pulse Width
	To V <sub>DD</sub>	To V <sub>SS</sub>	Input Pulse To		
Astable Multivibrator					
Free-Running	4, 5, 6, 14	7, 8, 9, 12		10, 11, 13	$t_A(10, 11) = 4.40 RC$
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	$t_A(13) = 2.20 RC$
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	$t_M(10, 11) = 2.48 RC$
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown (Note 1)	14	5, 6, 7, 8, 9, 12	Figure 1	Figure 1	Figure 1

Note 1: External resistor between terminals 2 and 3. External capacitor between terminals 1 and 3.

## Typical Implementation of External Countdown Option

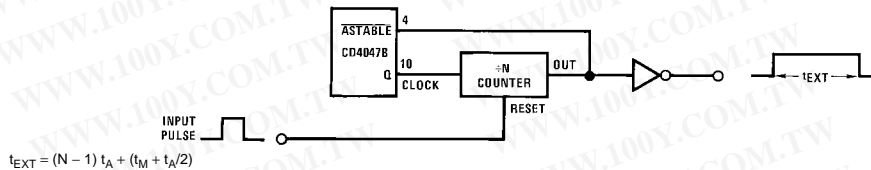
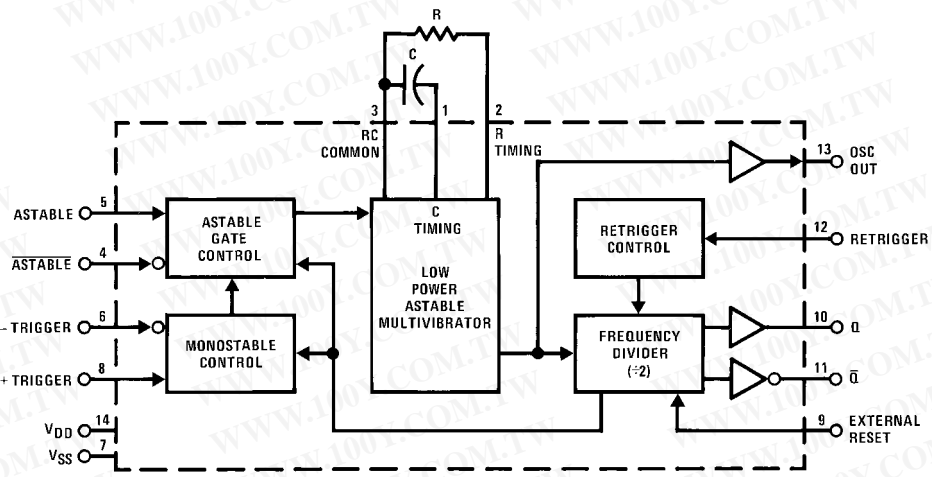


FIGURE 1.

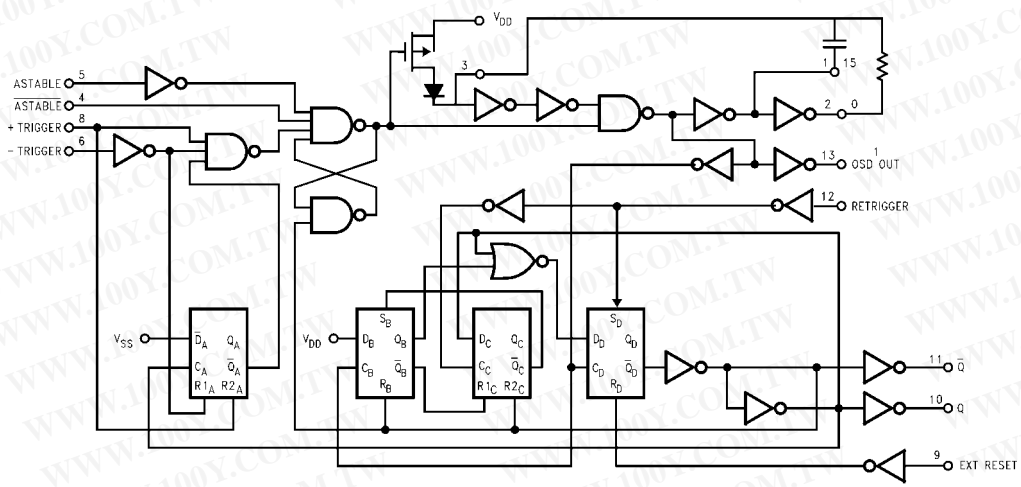
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**Block Diagram**



**Logic Diagram**



\*Special input protection circuit to permit larger input-voltage swings.

**Absolute Maximum Ratings** (Note 2)

(Note 3)

DC Supply Voltage ( $V_{DD}$ )	-0.5V to +18V <sub>DC</sub>
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{DD}$ +0.5V <sub>DC</sub>
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 3)

DC Supply Voltage ( $V_{DD}$ )	3V to 15V <sub>DC</sub>
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$ V <sub>DC</sub>
Operating Temperature Range ( $T_A$ )	-40°C to +85°C

**Note 2:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 3:**  $V_{SS} = 0V$  unless otherwise specified.

**DC Electrical Characteristics** (Note 3)

Symbol	Parameter	Conditions	-40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V$		20			20		150	$\mu A$
		$V_{DD} = 10V$		40			40		300	$\mu A$
		$V_{DD} = 15V$		80			80		600	$\mu A$
$V_{OL}$	LOW Level Output Voltage	$ I_O  < 1 \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
$V_{OH}$	HIGH Level Output Voltage	$ I_O  < 1 \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
$V_{IL}$	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or 9V		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0		6.75	4.0		4.0	V
$V_{IH}$	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1V$ or 9V	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0	8.25		11.0		V
$I_{OL}$	LOW Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
$I_{OH}$	HIGH Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 4.6V$	-0.52		-0.44	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	-8.8		-2.4		mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		$-10^{-5}$	-0.3		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		$10^{-5}$	0.3		1.0	$\mu A$

**Note 4:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

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<b>AC Electrical Characteristics</b> (Note 5)						
T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 200k, input t <sub>r</sub> = t <sub>f</sub> = 20 ns, unless otherwise specified.						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Time Astable, Astable to Osc Out	V <sub>DD</sub> = 5V		200	400	ns
		V <sub>DD</sub> = 10V		100	200	ns
		V <sub>DD</sub> = 15V		80	160	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Astable, Astable to Q, $\bar{Q}$	V <sub>DD</sub> = 5V		550	900	ns
		V <sub>DD</sub> = 10V		250	500	ns
		V <sub>DD</sub> = 15V		200	400	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	+ Trigger, - Trigger to $\bar{Q}$	V <sub>DD</sub> = 5V		700	1200	ns
		V <sub>DD</sub> = 10V		300	600	ns
		V <sub>DD</sub> = 15V		240	480	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	+ Trigger, Retrigger to $\bar{Q}$	V <sub>DD</sub> = 5V		300	600	ns
		V <sub>DD</sub> = 10V		175	300	ns
		V <sub>DD</sub> = 15V		150	250	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Reset to Q, $\bar{Q}$	V <sub>DD</sub> = 5V		300	600	ns
		V <sub>DD</sub> = 10V		125	250	ns
		V <sub>DD</sub> = 15V		100	200	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Transition Time Q, $\bar{Q}$ , Osc Out	V <sub>DD</sub> = 5V		100	200	ns
		V <sub>DD</sub> = 10V		50	100	ns
		V <sub>DD</sub> = 15V		40	80	ns
t <sub>WL</sub> , t <sub>WH</sub>	Minimum Input Pulse Duration	Any Input				
		V <sub>DD</sub> = 5V		500	1000	ns
		V <sub>DD</sub> = 10V		200	400	ns
t <sub>RCL</sub> , t <sub>FCL</sub>	+ Trigger, Retrigger, Rise and Fall Time	V <sub>DD</sub> = 5V			15	μs
		V <sub>DD</sub> = 10V			5	μs
		V <sub>DD</sub> = 15V			5	μs
C <sub>IN</sub>	Average Input Capacitance	Any Input		5	7.5	pF

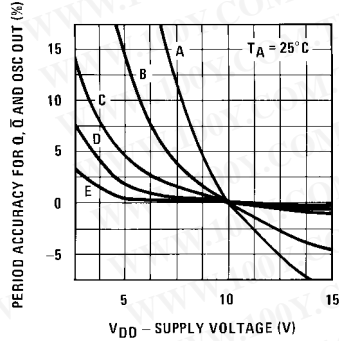
**Note 5:** AC Parameters are guaranteed by DC correlated testing.

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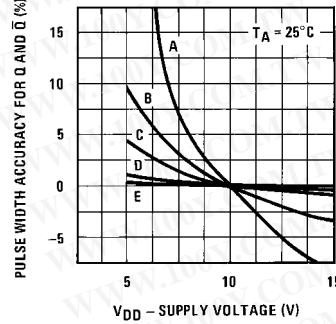
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## Typical Performance Characteristics

Typical Q,  $\bar{Q}$ , Osc Out Period Accuracy vs Supply Voltage (Astable Mode Operation)



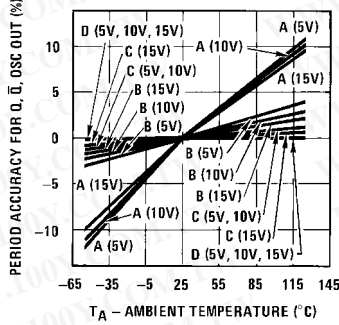
Typical Q,  $\bar{Q}$ , Pulse Width Accuracy vs Supply Voltage Monostable Mode Operation



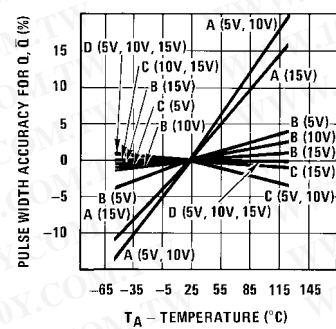
$f_{Q, \bar{Q}}$	R	C
A 1000 kHz	22k	10 pF
B 100 kHz	22k	100 pF
C 10 kHz	220k	100 pF
D 1 kHz	220k	1000 pF
E 100 Hz	2.2M	1000 pF

$t_M$	R	C
A 2 $\mu$ s	22k	10 pF
B 7 $\mu$ s	22k	100 pF
C 60 $\mu$ s	220k	100 pF
D 550 $\mu$ s	220k	1000 pF
E 5.5 ms	2.2M	1000 pF

Typical Q,  $\bar{Q}$  and Osc Out Period Accuracy vs Temperature Astable Mode Operation



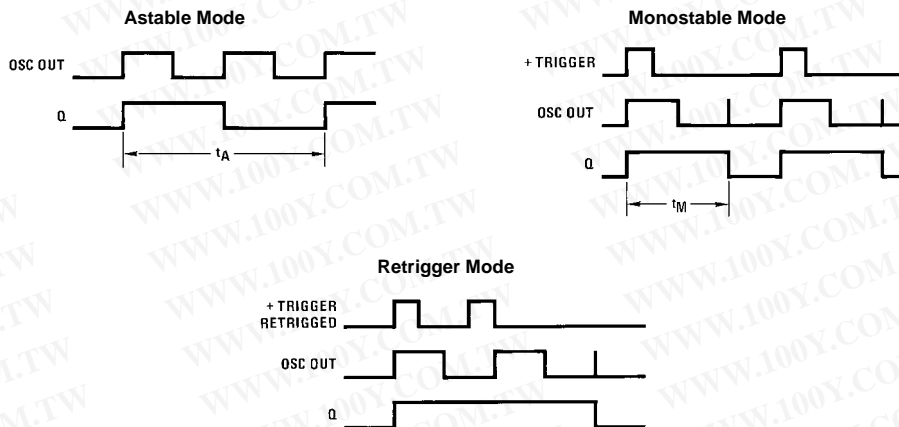
Typical Q and  $\bar{Q}$  Pulse Width Accuracy vs Temperature Monostable Mode Operation



$f_{Q, \bar{Q}}$	R	C
A 1000 kHz	22k	10 pF
B 100 kHz	22k	100 pF
C 10 kHz	220k	100 pF
D 1 kHz	220k	1000 pF

$t_M$	R	C
A 2 $\mu$ s	22k	10 pF
B 7 $\mu$ s	22k	100 pF
C 60 $\mu$ s	220k	100 pF
D 550 $\mu$ s	220k	1000 pF

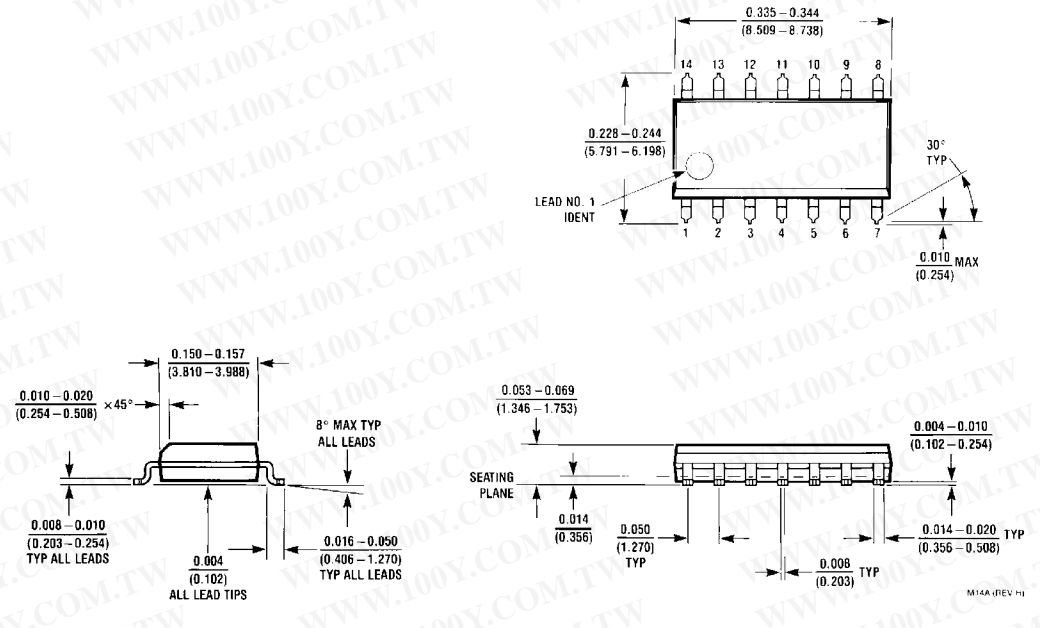
Timing Diagrams



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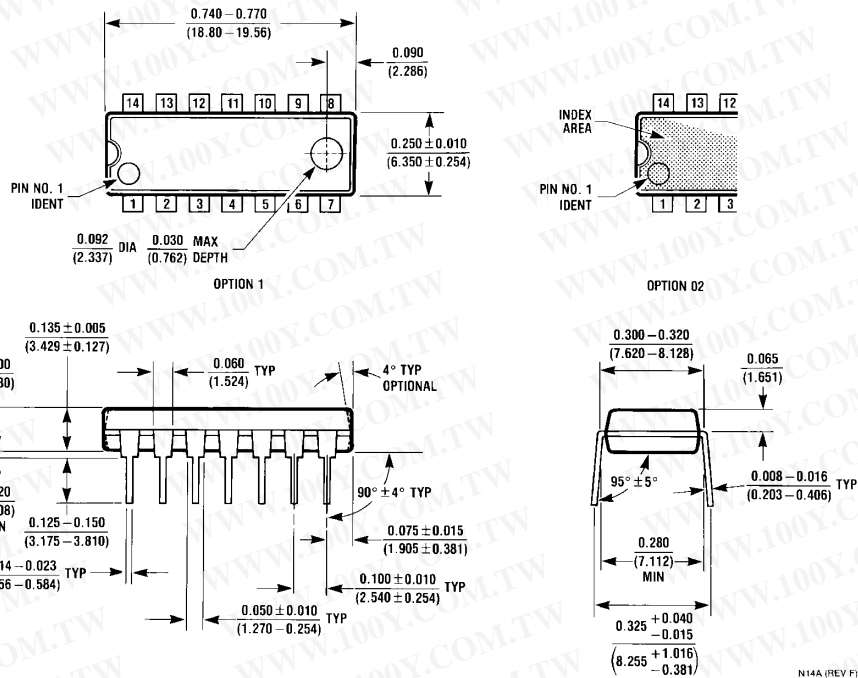
**Physical Dimensions** inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow  
Package Number M14A

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**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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