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Wideband, Low Distortion, Low Gain OPERATIONAL AMPLIFIER

OPA642

FEATURES

- **LOW DISTORTION: –95dBc at 5MHz**
- **GAIN OF +1 BANDWIDTH: 400MHz**
- **AVAILABLE IN SOT23-5 PACKAGE**
- **HIGH OPEN LOOP GAIN: 95dB**
- **HIGH COMMON-MODE REJECTION: 90dB**
- **FAST 12-BIT SETTLING: 13ns (0.01%)**
- **LOW NOISE: 2.7nV/√Hz**
- **HIGH OUTPUT CURRENT: ±60mA**
- **VERY LOW DIFF GAIN/PHASE ERROR: 0.007%/0.008°**

APPLICATIONS

- **ADC/DAC BUFFER AMPLIFIER**
- **LOW DISTORTION IF AMPLIFIER**
- **HIGH RESOLUTION IMAGING**
- **MEDICAL IMAGING**
- **LOW NOISE PREAMPLIFIER**
- **HIGH CMR DIFFERENCING AMPLIFIER**
- **TEST INSTRUMENTATION**
- **PROFESSIONAL AUDIO**

DESCRIPTION

The OPA642 provides a level of speed and dynamic range previously unattainable in a monolithic op amp. Using a unity gain stable voltage feedback architecture with two internal gain stages, the OPA642 achieves exceptionally low harmonic distortion over a wide frequency range. The "classic" differential input provides all the familiar benefits of precision op amps, such as bias current cancellation and very low inverting current noise compared with wideband current feedback op amps. Fast settling time, excellent differential gain/phase performance, low voltage noise and high output current drive make the OPA642 ideal for most high dynamic range applications.

Unity gain stability makes the OPA642 particularly suitable for low gain differential amplifiers, transimpedance amplifiers, gain of +2 video line drivers, wideband integrators and low distortion ADC buffers. Where higher gain or even lower harmonic distortion is required, consider the OPA643—a higher gain-bandwidth and lower noise version of the OPA642
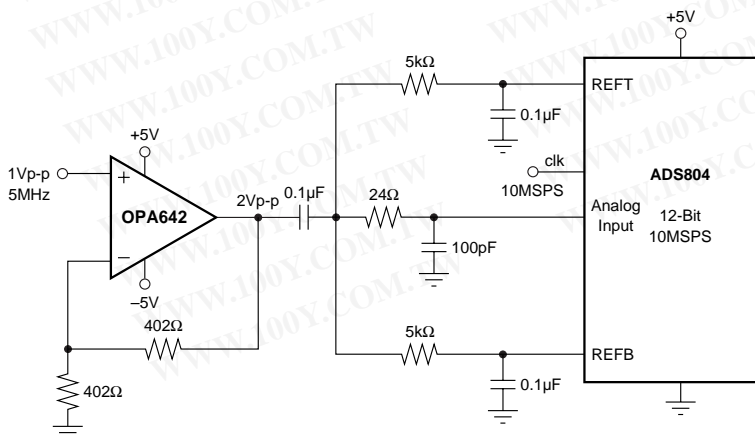
High Dynamic Range 10MSPS Digitizer

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, R_F = 402Ω, unless otherwise noted. R_F = 25Ω for a gain of +1.

PARAMETER	CONDITIONS	OPA642P, U, N			OPA642PB, UB, NB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			±1.5	±4		±0.5	±1.0	mV
Average Drift			4			2		µV/°C
Power Supply Rejection (PSR)	V_S = ±4.5 to ±5.5V	65	85		73	95		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		25	45	∗	∗		µA
Over Specified Temperature				70		∗	∗	µA
Input Offset Current	V_{CM} = 0V		0.1	2.0	∗	∗		µA
Over Specified Temperature				3.0			∗	µA
NOISE								
Input Voltage Noise								
Noise Density: f ≥ 1MHz			2.7			∗		nV/√Hz
Integrated Voltage Noise, BW = 100Hz to 100MHz			27			∗		µVrms
Input Bias Current Noise Density								
f ≥ 1MHz			2.8			∗		pA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.75	±3.0		∗	∗		V
Over Temperature		±2.5			∗			V
Common-Mode Rejection (CMR)	V_{CM} = ±0.5V	65	90		80	∗		dB
INPUT IMPEDANCE								
Differential			11 ‖ 1			∗		kΩ ‖ pF
Common-Mode			650 ‖ 1			∗		kΩ ‖ pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain (A_{OL})	V_O = ±2V, R_L = 100Ω	80	95		85	98		dB
Over Specified Temperature		80			∗			dB
FREQUENCY RESPONSE								
Closed-Loop Response	Gain = +1V/V		400			∗		MHz
	Gain = +2V/V		150			∗		MHz
	Gain = +5V/V		45			∗		MHz
	Gain = +10V/V		21			∗		MHz
Gain Bandwidth Product (GBP)			210			∗		MHz
Slew Rate[1]	G = +1, 2V Step		380			∗		V/µs
At Minimum Specified Temperature	G = +1, 2V Step		340			∗		V/µs
Settling Time: 0.01%	G = +1, 1V Step		13			∗		ns
0.1%	G = +1, 1V Step		11.5			∗		ns
1%	G = +1, 1V Step		3.5			∗		ns
Spurious Free Dynamic Range (SFDR)	G = +1, f = 5MHz		92			95		dBc
	V_O = 2Vp-p, R_L = 100Ω							
Diff. Gain Error at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.007			∗		%
Diff. Phase Error at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.008			∗		degrees
OUTPUT								
Voltage Output	No Load		±3.5			∗		V
Over Specified Temperature		±3.0			∗			V
Voltage Output	R_L = 100Ω		±2.75			∗		V
Over Specified Temperature		±2.5			∗	∗		V
Current Output, +25°C		±40	±60		±50	±65		mA
Over Specified Temperature		±35			±40			mA
Closed-Loop Output Resistance	0.1MHz, G = +1V/V		0.01			∗		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			∗		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	∗		∗	V
Quiescent Current			±20	±25	±16	∗	∗	mA
Over Specified Temperature				±26			∗	mA
TEMPERATURE RANGE								
Specification: P, U, N, PB, UB, NB	Ambient	−40		+85	∗		∗	°C
Thermal Resistance	θ_{JA}, Junction-to-Ambient							°C/W
P, PB 8-Pin DIP			100			∗		°C/W
U, UB 8-Pin SO-8			125			∗		°C/W
N, NB 5-Pin SOT23-5			150			∗		°C/W

∗ Indicates same specification as for OPA642P, U, N.

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

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ABSOLUTE MAXIMUM RATINGS

Supply .... ±6.0VDC
Internal Power Dissipation[1] .... See Thermal Analysis
Differential Input Voltage .... ±1.2V
Input Voltage Range .... ±V_S
Storage Temperature Range: P, PB, U, UB, N, NB..... –40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
　　　　　　　 (soldering, SO-8 3s) .... +260°C
Junction Temperature (T_J) .... +175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

⚠ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION

Top View　　　　　　　　　　　　　　　　　　　**DIP/SO-8**

NC	1	8　$+V_{S2}$[1]
Inverting Input	2	7　$+V_{S1}$
Non-Inverting Input	3	6　Output
$-V_{S1}$	4	5　$-V_{S2}$[1]

SOT23-5

Output	1	5　$+V_S$
$-V_S$	2	
Non-Inverting Input	3	4　Inverting Input

NOTE: (1) Making use of all four power supply pins is recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the power supply impedance improving distortion.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	TEMPERATURE RANGE	PACKAGE MARKING[2]	ORDERING NUMBER[3]
OPA642U	SO-8 Surface Mount	182	–40°C to +85°C	OPA642U	OPA642U
OPA642UB	SO-8 Surface Mount	182	–40°C to +85°C	OPA642UB	OPA642UB
OPA642N	5-pin SOT23-5	331	–40°C to +85°C	A42	OPA642N-250
					OPA642N-3k
OPA642NB	5-pin SOT23-5	331	–40°C to +85°C	A42B	OPA642NB-250
					OPA642NB-3k
OPA642P	8-Pin Plastic DIP	006	–40°C to +85°C	OPA642P	OPA642P
OPA642PB	8-Pin Plastic DIP	006	–40°C to +85°C	OPA642PB	OPA642PB

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 and DIP packages will be marked with a "B" by pin 8. The "B" grade of the SOT23-5 will be marked with a "B" near pins 3 and 4. (3) The SOT23-5 is only available on a 7" tape and reel (e.g. ordering 250 pieces of "OPA642N-250" will get a single 250 piece tape and reel. Ordering 3000 pieces of "OPA642N-3k" will get a single 3000 piece tape and reel). Please refer to Appendix B of Burr-Brown IC Data Book for detailed Tape and Reel Mechanical information.
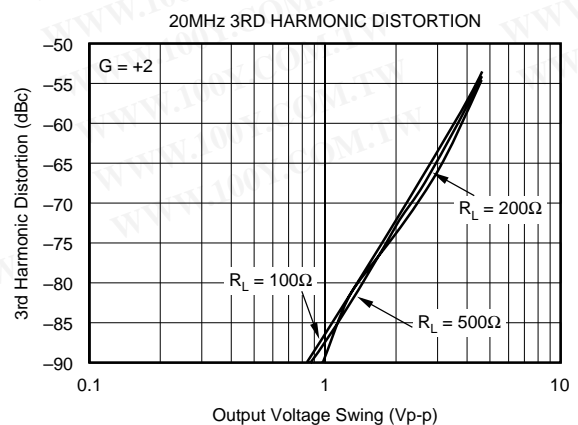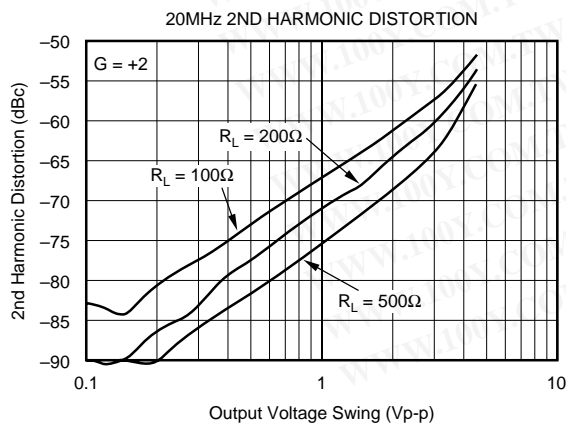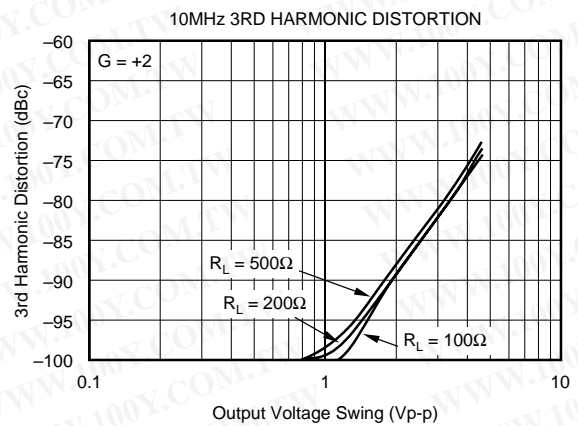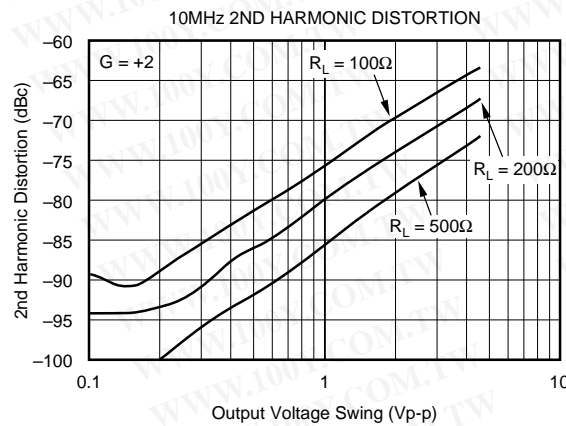
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TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, R_F = 402Ω, G = +2, unless otherwise noted. R_F = 25Ω for a gain of +1.

SMALL SIGNAL FREQUENCY RESPONSE

LARGE SIGNAL FREQUENCY RESPONSE

SMALL SIGNAL TRANSIENT RESPONSE
(G = +1, R_L = 100Ω)

LARGE SIGNAL TRANSIENT RESPONSE
(G = +1, R_L = 100Ω)

R_S vs CAPACITIVE LOAD

FREQUENCY RESPONSE vs CAPACITIVE LOAD

TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, R_F = 402Ω, G = +2, unless otherwise noted. R_F = 25Ω for a gain of +1.

5MHz 2ND HARMONIC DISTORTION

5MHz 3RD HARMONIC DISTORTION

10MHz 2ND HARMONIC DISTORTION

10MHz 3RD HARMONIC DISTORTION

20MHz 2ND HARMONIC DISTORTION

20MHz 3RD HARMONIC DISTORTION

OPA642

TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, R_F = 402Ω, G = +2, unless otherwise noted. R_F = 25Ω for a gain of +1.

2ND HARMONIC DISTORTION vs FREQUENCY

3RD HARMONIC DISTORTION vs FREQUENCY

INPUT VOLTAGE AND CURRENT NOISE DENSITY

TWO-TONE, THIRD ORDER INTERMODULATION INTERCEPT

OPEN-LOOP GAIN AND PHASE

TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, R_F = 402Ω, G = +2, unless otherwise noted. R_F = 25Ω for a gain of +1.

CMR AND PSR vs FREQUENCY

CLOSED-LOOP OUTPUT IMPEDANCE

DIFFERENTIAL AND COMMON-MODE
INPUT IMPEDANCE

COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE

A_{OL}, PSR AND CMR vs TEMPERATURE

OUTPUT AND QUIESCENT CURRENT
vs TEMPERATURE

7

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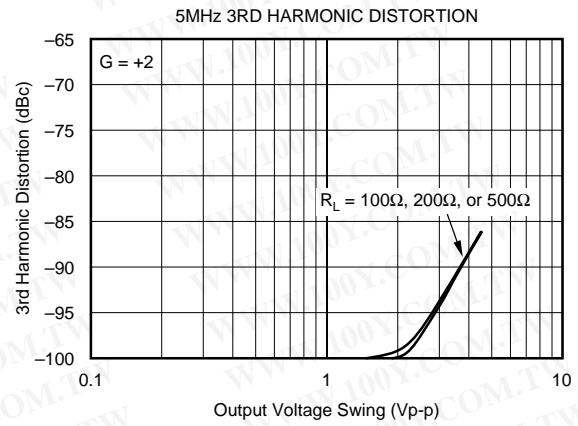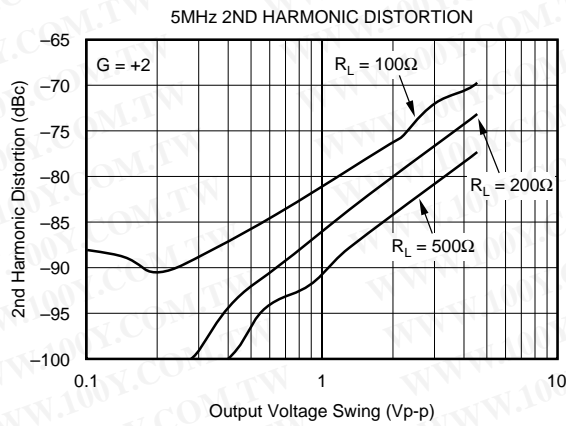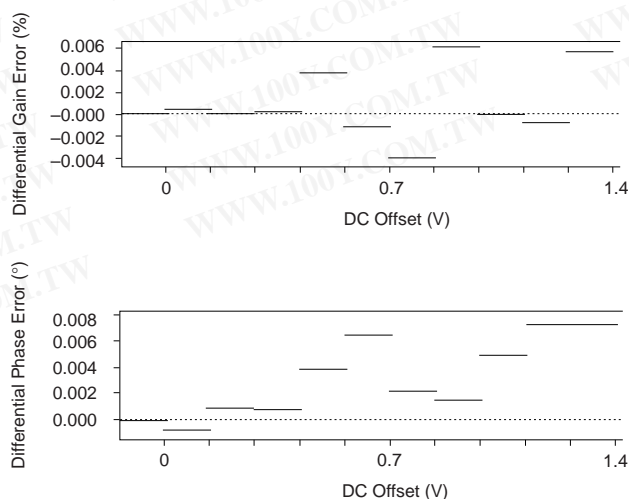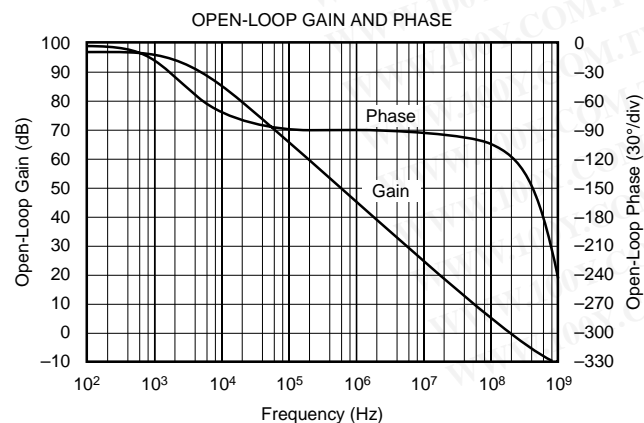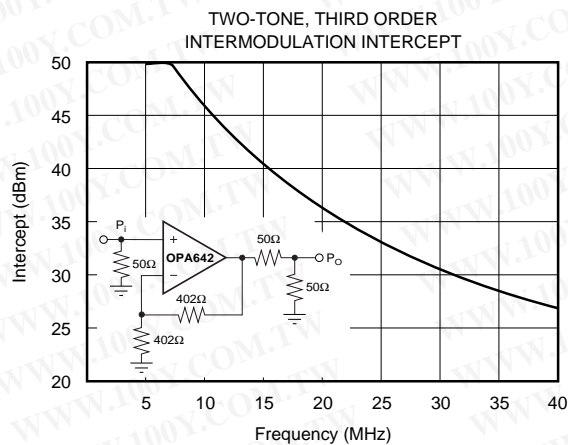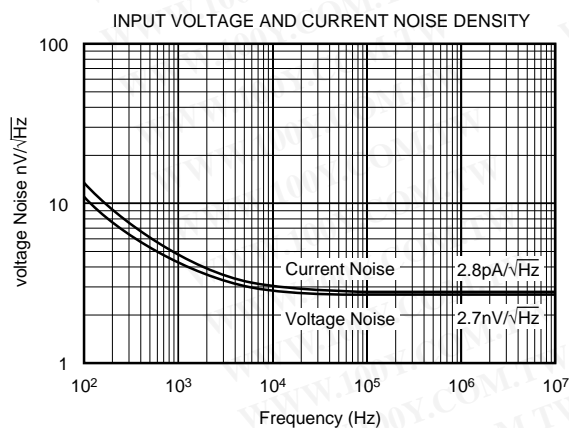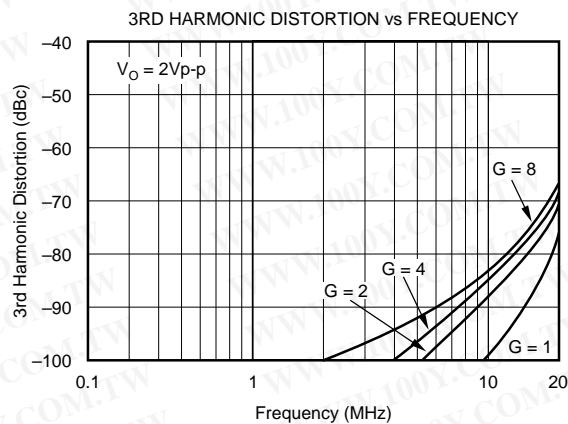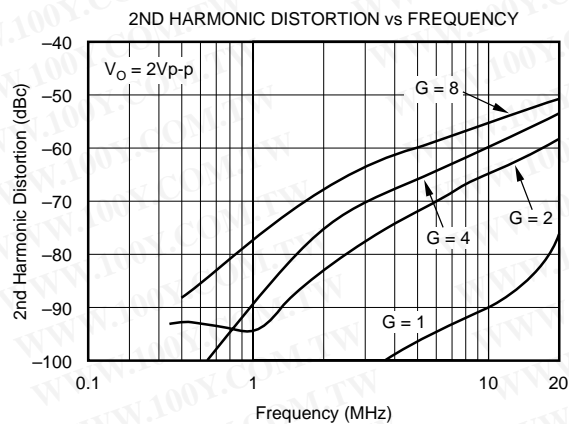
APPLICATIONS INFORMATION

WIDEBAND VOLTAGE FEEDBACK OPERATION

The OPA642's combination of speed and dynamic range is easily achieved in a wide variety of application circuits, providing that simple principles of good design practice are observed. For example, good power supply decoupling, as shown in Figure 1, is essential to achieve the lowest possible harmonic distortion and smooth frequency response. Proper PC board layout and careful component selection will maximize the performance of the OPA642 in all applications, as discussed in the remaining sections of this data sheet.

Figure 1 shows the gain of +2 configuration used as the basis for most of the Typical Performance Curves. Most of the curves were characterized using signal sources with 50Ω driving impedance, and with measurement equipment presenting 50Ω shunt load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet specifications refer to the voltage swing at the output pin (V_O in Figure 1). The 100Ω load from the series and shunt matching resistances, combined with the 804Ω total feedback network load, presents the OPA642 with an effective load of approximately 90Ω.
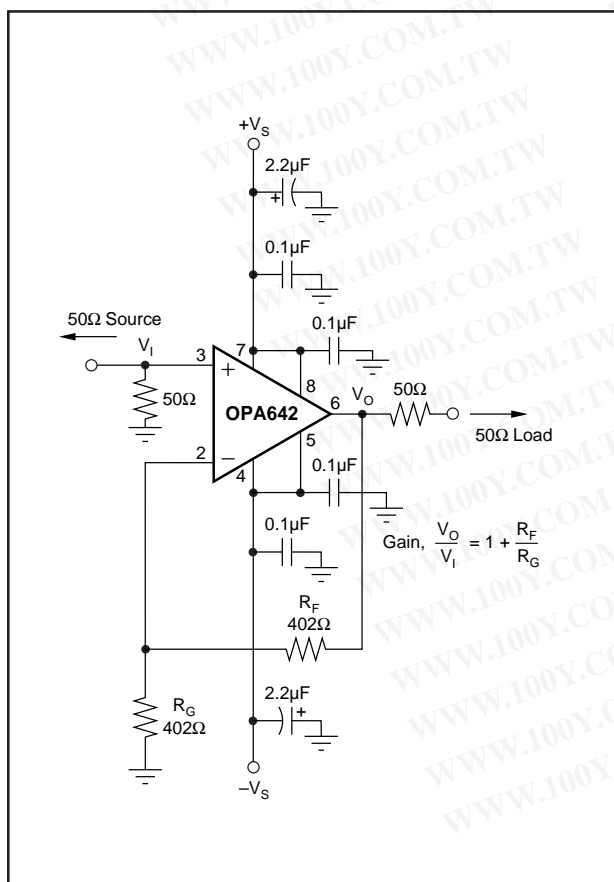

FIGURE 1. Gain of +2, High Frequency Application and Characterization Circuit [P or U Package].

BUFFERING HIGH PERFORMANCE ADC'S

To achieve full performance from a high dynamic range A/D converter, considerable care must be exercised in the design of the input amplifier interface circuit. The example circuit on the front page shows a typical AC-coupled interface to a very high dynamic range converter. The frequency domain application allows the OPA642 to be operated in its most linear region, using a signal range which swings symmetrically around ground (0V). The 2Vp-p swing is then level-shifted through the blocking capacitor to a DC reference level, which is created by a well-decoupled resistive divider off the converter's internal reference voltages. To have a negligible effect on the rated spurious-free dynamic range (SFDR) of the converter, the amplifier's SFDR should be at least 10dB greater. In the front page example, the insertion of the OPA642 has an immeasurable effect on the distortion of the ADS804, which achieves 80dB SFDR at 5MHz Nyquist input signal.

To achieve the lowest possible distortion in the 8-pin SO-8 or DIP package, the addition of 0.1μF decoupling capacitors on pins 5 and 8 is required. These are shown in Figure 1. Although pins 5 and 8 are internally connected to pins 4 and 7 respectively (the standard supply pins for 8-pin op amps), the additional capacitors help to decouple the package lead inductances and improve second harmonic suppression at 5MHz by approximately 4dB. The much shorter bond wires and supply leads of the SOT23-5 package give the best distortion performance while requiring only two power supply connections.

Successful application of the OPA642 for ADC buffering requires careful selection of the series resistor at the amplifier output, along with the additional shunt capacitor at the ADC input. To some extent, selection of this RC network will be determined empirically for each model of converter. Many high performance CMOS ADCs, like the ADS804, perform better with the shunt capacitor at the input pin. This capacitor provides a low source impedance for the transient currents produced by the sampling process. Improved SFDR is obtained by adding the capacitor, whose value is often recommended in the converter data sheet. The external capacitor, in combination with the built-in capacitance of the A/D input, presents a significant capacitive load to the OPA642. Without a series isolation resistor, the result could be undesirable peaking or loss of stability in the amplifier. Since the DC bias current of the CMOS A/D input is negligible, the resistor has no effect on overall gain or offset accuracy. Refer to the plot of "R_S vs Capacitive Load" in the Typical Performance Curves to obtain a good starting value for the series resistor. This will ensure flat frequency response to the ADC input. Increasing the external capacitor value will allow the series resistor to be reduced or, keeping this resistor fixed, will band-limit the signal and reduce high frequency noise to the input of the converter.

VIDEO LINE DRIVING

Most video distribution systems are designed with 75Ω series resistors to drive a matched 75Ω cable. In order to deliver a net gain of 1 to the 75Ω matched load, the amplifier

is typically set up for a voltage gain of +2, compensating for the 6dB attenuation of the voltage divider formed by the series and shunt 75Ω resistors at either end of the cable. The circuit of Figure 1 applies to this requirement if all references to 50Ω resistors are replaced by 75Ω values. Often, the amplifier gain is further increased to 2.2, which recovers the additional DC loss of a typical long cable run. This change would require the gain resistor (R_G) in Figure 1 to be reduced from 402Ω to 335Ω. In either case, both the gain flatness and the differential gain/phase performance of the OPA642 will provide exceptional results in video distribution applications. Differential Gain and Phase measure the change in overall small-signal gain and phase for the color subcarrier frequency (3.58MHz in NTSC systems) vs changes in the large-signal output level (which represents luminance information in a composite video signal). The OPA642, with the typical 150Ω load of a single matched video cable, shows less than 0.01%/0.01° differential gain/phase errors over the standard luminance range for a positive video (negative sync) signal. Similar performance would be observed for negative video signals. In practice, similar performance is achieved even with two video loads due to the linear high-frequency output impedance of the OPA642.

SINGLE OP-AMP DIFFERENTIAL AMPLIFIER

The voltage feedback architecture of the OPA642, with its high CMR, will provide exceptional performance in differential amplifier configurations. Figure 2 shows a typical configuration. The starting point for this design is the selection of the R_F value in the range of 200Ω to 2kΩ. Lower values reduce the required R_G increasing the load on the V_2 source and on the OPA642 output. Higher values increase output noise and exacerbate the effects of parasitic board and device capacitances. Following the selection of R_F, R_G must be set to achieve the desired inverting gain for V_2. Remember that the bandwidth will be set approximately by the gain bandwidth product (GBP) divided by the noise gain (1+ R_F/R_G). For accurate differential operation (i.e. good CMR), the ratio R_2/R_1 must be set equal to R_F/R_G. Usually, it is best to set the absolute values of R_2 and R_1 equal to R_F and R_G respectively; this equalizes the divider resistances and cancels the effect of input bias currents. However, it is sometimes useful to scale the values of R_2 and R_1 in order to adjust the loading on the driving source V_1. In most cases, the achievable low frequency CMR will be limited by the accuracy of the resistor values. The 90dB CMR of the OPA642 itself will not determine the overall circuit CMR unless the resistor ratios are matched to better than 0.003%. If it is necessary to trim the CMR, then R_2 is the suggested adjustment point.

THREE OP AMP DIFFERENCING
(Instrumentation Topology)

The primary drawback of the single op-amp differential amplifier is its relatively low input impedances. Where a high impedance is required at the differential input, a standard instrumentation amplifier (INA) topology may be built using the OPA642 as the differencing stage. Figure 3 shows an example of this, in which the two input amplifiers are

packaged together as a dual voltage feedback op-amp—the OPA2650. This approach saves board space, cost and power compared to using two additional OPA642 devices, and still achieves very good noise and distortion performance due to the moderate loading on the input amplifiers. In this circuit, the common mode gain to the output is always one due to the four matched 1kΩ resistors, while the differential gain is set by $(1 + 2R_{F1}/R_G)$—which is equal to 2 using the values in Figure 3. The differential to single-ended conversion is still performed by the OPA642 output stage. The high impedance inputs allow the V_1 and V_2 sources to be terminated or impedance matched as required without further loading by the differential amplifier. If the V_1 and V_2 inputs are already truly differential, such as the output from a signal transformer, then a single matching termination resistor may be used between them. Remember, however, that a defined DC signal path must always exist for the V_1 and V_2 inputs; for the transformer case, a center-tapped secondary connected to ground would provide an optimum DC operating point.
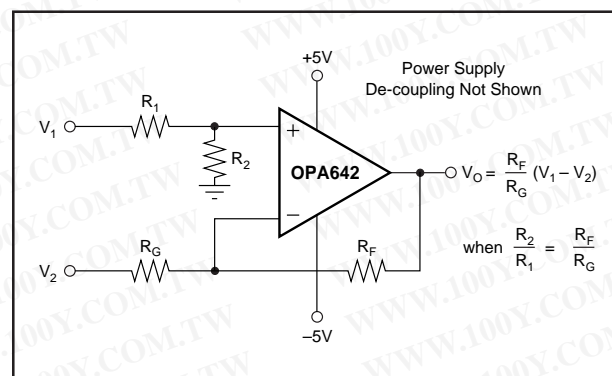

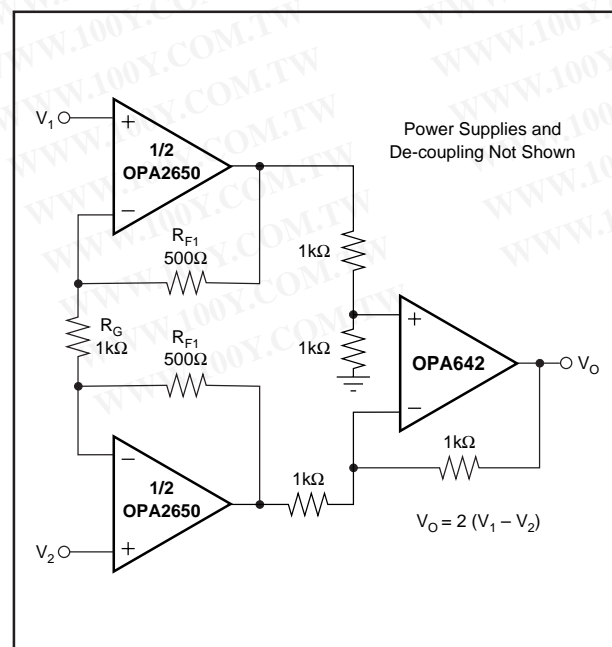FIGURE 2. High Speed, Single Amplifier Differential Amplifier.

FIGURE 3. Wideband 3-Op Amp Differencing Amplifier.

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DAC TRANSIMPEDANCE AMPLIFIER

High frequency DDC DACs require a low distortion output amplifier to retain their SFDR performance into real-world loads. A single-ended output drive implementation is shown in Figure 4. In this circuit, only one side of the complementary output drive signal is used. The diagram shows the signal output current connected into the virtual ground summing junction of the OPA642, which is set up as a transimpedance stage or "I-V converter". The unused current output of the DAC is connected to ground. If the DAC requires its outputs terminated to a compliance voltage other than ground for operation, then the appropriate voltage level may be applied to the non-inverting input of the OPA642. The DC gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance will produce a zero in the noise gain for the OPA642 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, this pole in the feedback network should be set to:

$$1 / 2\pi R_F C_F = \sqrt{GBP / \left(4\pi R_F C_D\right)}$$

which will give a corner frequency f_{-3dB} of approximately:

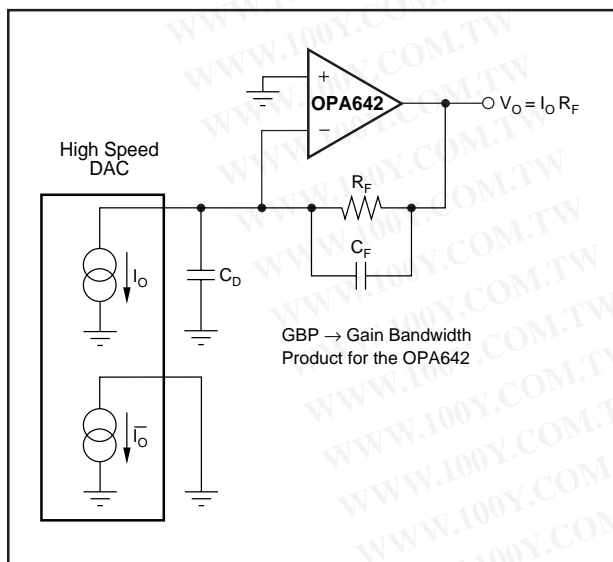$$f_{-3dB} = \sqrt{GBP / 2\pi R_F C_D}$$

FIGURE 4. Wideband, Low Distortion DAC Transimpedance Amplifier.

ACTIVE FILTERS

Most active filter topologies will deliver exceptional performance using the broad bandwidth and unity gain stability of the OPA642. Topologies employing capacitive feedback require a unity gain stable voltage feedback op amp. Sallen-Key filters simply use the op amp as a non-inverting gain stage inside an RC network. Either current or voltage feedback op amps may be used in Sallen-Key implementations.

Figure 5 shows an example Sallen-Key low pass filter, in which the OPA642 is set up to deliver a low frequency gain of +2. The filter component values have been selected to achieve a maximally flat Butterworth response with a 5MHz –3dB bandwidth. The resistor values have been slightly adjusted to compensate for the effects of the 150MHz bandwidth provided by the OPA642 in this configuration. This filter may be combined with the ADC driver suggestions to provide moderate (2-pole) Nyquist filtering, limiting noise and out of band components into the input of an ADC. This filter will deliver the exceptionally low harmonic distortion required by high SFDR A/D converters such as the ADS804 (12-bit, 10MSPS, 80dB SFDR).
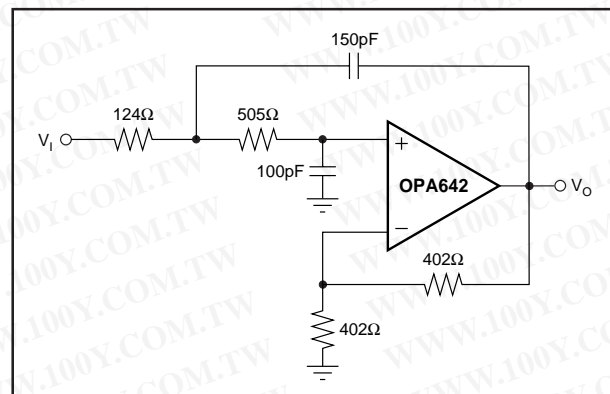

FIGURE 5. 5MHz Butterworth Low Pass Active Filter.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Since the OPA642 is a unity gain stable voltage feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a non-inverting unity gain follower application, the feedback connection should be made with a 25Ω resistor—not a direct short. This will isolate the inverting input capacitance from the output pin and improve the frequency response flatness. Usually, the feedback resistor value should be between 200Ω and 1kΩ. Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA642. Above 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band-limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (Figure 1) to be less than about 200Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G$ < 200Ω will keep this pole above 400MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G may be set equal to the required termination value. However, at low inverting gains the resultant feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50Ω input matching resistor (= R_G) would require a 100Ω feedback resistor, which would contribute to output loading in parallel with the external load. In such a case, it would be preferable to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground. The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

BANDWIDTH VS GAIN

Voltage feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the specifications. Ideally, dividing GBP by the non-inverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low signal gains, most amplifiers will exhibit a more complex response with lower phase margin. The OPA642 is optimized to give a maximally flat second order Butterworth response in a gain of 2. In this configuration, the OPA642 has approximately 60° of phase margin and will show a typical –3dB bandwidth of 150MHz. When the phase margin is 60°, the closed-loop bandwidth is approximately $\sqrt{2}$ greater than the value predicted by dividing GBP by the noise gain. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 21MHz bandwidth shown in the Typical Specifications agrees with that predicted using the simple formula and the typical GBP of 210MHz.

OUTPUT DRIVE CAPABILITY

The OPA642 has been optimized to drive the demanding load of a doubly terminated transmission line. When a 50Ω line is driven, a series 50Ω into the cable and a terminating 50Ω load at the end of the cable are used. Under these conditions, the cable's impedance will appear resistive over a wide frequency range, and the total effective load on the OPA642 is 100Ω in parallel with the resistance of the feedback network. The Specifications show a guaranteed ±2.5V swing into a such a load—which will then be reduced to a ±1.25V swing at the termination resistor. The guaranteed ±35mA output drive over temperature provides adequate current drive margin for this load. Higher voltage swings (and lower distortion) are achievable when driving higher impedance loads.

A single video load typically appears as a 150Ω load (using standard 75Ω cables) to the driving amplifier. The OPA642 provides adequate voltage and current drive to support up to 3 parallel video loads (50Ω total load) for an NTSC signal. With only one load, the OPA642 achieves an exceptionally low 0.007%/0.008° dG/dP error.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. A high speed, high open-loop gain, amplifier like the OPA642 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. In simple terms, the capacitive load reacts with the open-loop output resistance of the amplifier to introduce an additional pole into the loop and thereby decrease the phase margin. This issue has become a popular topic of application notes and articles, and several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Performance Curves show the recommended R_S vs Capacitive Load and the resulting frequency response at the load. The criterion for setting the recommended resistor is maximum bandwidth, flat frequency response at the load. Since there is now a passive low pass filter between the output pin and the load capacitance, the response at the output pin itself is typically somewhat peaked, and becomes flat after the rolloff action of the RC network. This is not a concern in most applications, but can cause clipping if the desired signal swing at the load is very close to the amplifier's swing limit. Such clipping would be most likely to occur in pulse response applications where the frequency peaking is manifested as an overshoot in the step response.

Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA642. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA642 output pin (see Board Layout Guidelines).

DISTORTION PERFORMANCE

The OPA642 is capable of delivering an exceptionally low distortion signal at high frequencies and low gains. The distortion plots in the Typical Performance Curves show the typical distortion under a wide variety of conditions. Most of these plots are limited to 100dB dynamic range. The OPA642's distortion does not rise above –100dBc until either the signal level exceeds 0.5V and/or the fundamental frequency exceeds 500kHz. **Distortion in the audio band is ≤ –120dBc.**

Generally, until the fundamental signal reaches very high frequencies or powers, the second harmonic will dominate the distortion with negligible third harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the non-inverting

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configuration this is sum of $R_F + R_G$, while in the inverting configuration this is just R_F (Figure 1). Increasing output voltage swing increases harmonic distortion directly. A 6dB increase in output swing will generally increase the second harmonic 12dB and the third harmonic 18dB. Increasing the signal gain will also increase the second harmonic distortion. Again a 6dB increase in gain will increase the second and third harmonic by 6dB even with a constant output power and frequency. And finally, the distortion increases as the fundamental frequency increases due to the rolloff in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open-loop pole at approximately 3kHz. Starting from the –90dBc second harmonic for 2Vp-p into 500Ω, G = +2 distortion at 1MHz (from the Typical Performance Curves), the second harmonic distortion at 20kHz should be approximately –90dB – 20log (1MHz/20kHz) = –124dBc.

The OPA642 has an extremely low third order harmonic distortion. This also gives an exceptionally good two-tone, third-order intermodulation intercept as shown in the Typical Performance Curves. This intercept curve is defined at the 50Ω load when driven through a 50Ω matching resistor to allow direct comparisons to RF MMIC devices. This network attenuates the voltage swing from the output pin to the load by 6dB. If the OPA642 drives directly into the input of a high impedance device, such as an ADC, this 6dB attenuation is not taken. Under these conditions, the intercept will increase by a minimum 6dBm. The intercept is used to predict the intermodulation spurious for two closely spaced frequencies. If the two test frequencies, f1 and f2, are specified in terms of average and delta frequency, $f_O = (f1 + f2)/2$ and $\Delta f = |f_2 - f_2|/2$, the two, third-order, close-in spurious tones will appear at $f_O \pm (3 \cdot \Delta f)$. The difference between two equal test tone power levels and these intermodulation spurious power levels is given by $2 \cdot (IM3 - P_O)$ where IM3 is the intercept taken from the Typical Performance Curve and P_O is the power level in dBm at the 50Ω load for one of the two closely spaced test frequencies. For instance, at 10MHz the OPA642 at a gain of +2 has an intercept of 46dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be 2Vp-p, this requires each tone to be 4dBm. The third-order intermodulation spurious tones will then be $2 \cdot (46 - 4) = 84$dBc below the test tone power level (–80dBm). If this same 2Vp-p two-tone envelope were delivered directly into the input of an ADC without the matching loss or loading of the 50Ω network, the intercept would increase to at least 52dBm. With the same signal and gain conditions but now driving directly into a light load, the spurious tones will then be at least $2 \cdot (52 - 4) = 96$dBc below the 1Vp-p test tone signal levels.

NOISE PERFORMANCE

The OPA642 complements its ultra-low harmonic distortion with low input noise terms. Both the input referred voltage noise, and the two input referred current noise terms combine to give a low output noise under a wide variety of operating conditions. Figure 6 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either $nV/\sqrt{Hz}$ or $pA/\sqrt{Hz}$.

The total output spot noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 1 shows the general form for this output noise voltage using the terms shown in Figure 6.

Eq. 1

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)G_N^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FG_N}$$
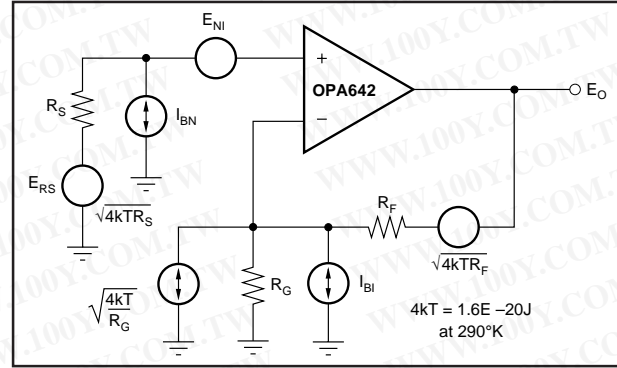

FIGURE 6. Op Amp Noise Analysis Model.

Dividing this expression by the noise gain ($G_N = 1 + R_F/R_G$) will give the equivalent input referred spot noise voltage at the non-inverting input as shown in Equation 2.

Eq. 2

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{G_N}\right)^2 + \frac{4kTR_F}{G_N}}$$

Evaluating these two equations for the OPA642 circuit shown in Figure 1 will give a total output spot noise voltage of $6.7nV/\sqrt{Hz}$ and an equivalent input spot noise voltage of $3.35nV/\sqrt{Hz}$.

Narrowband communications systems are more commonly concerned with the noise figure for the amplifier. The total input referred voltage noise expression (Eq. 2), may be used to calculate the noise figure. Equation 3 shows this noise figure expression using the E_N of Eq. 2 for the non-inverting configuration where the input terminating resistor R_T has been set to match the source impedance (as shown in Figure 1).

$$NF = 10\log\left[2 + \frac{E_N^2}{kTR_S}\right]$$

Eq. 3

Evaluating Equation 3 for the circuit of Figure 1 gives a Noise Figure = 17.6dB. Input transformer coupling can be used to reduce this noise figure. A broadband pulse transformer can provide both a noiseless voltage gain and a more optimum source impedance to minimize the noise figure. Figure 7 shows an example built from the circuit of Figure 1, in which the transformer turns ratio has been set to the

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closest integer for minimum noise figure. This optimum turns ratio is calculated by

Eq. 4

$$N_{OPT} = \text{Nearest Integer} \left(\sqrt{E_N / (I_{BN} \bullet (R_S / 2))} \right)$$

This optimum will depend strongly on the amplifier and configuration selected.
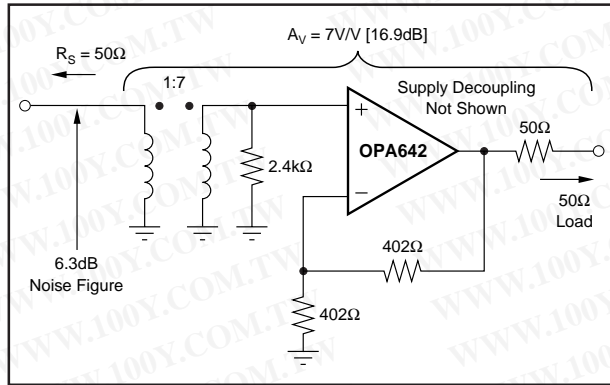

FIGURE 7. Reduced Noise Figure Circuit.

DC OFFSET CONTROL

The OPA642 can provide excellent DC signal accuracy due to its high open-loop gain, high common-mode rejection, high power supply rejection, and low input offset voltage and bias current offset errors. The high grade (B) version of any package type provides less than 1mV input offset voltage. To take full advantage of this low input offset voltage, a careful attention to input bias current cancellation is also required. The high speed input stage for the OPA642 has a relatively high input bias current ($25\mu A$ typ into the pins) but with a very close match between the two input currents—typically 100nA input offset current. The total output offset voltage may be considerably reduced by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 would be to insert a 175Ω series resistor into the non-inverting input from the 50Ω terminating resistor. When the 50Ω source resistor is DC coupled, this will increase the source impedance for the non-inverting input bias current to 200Ω. Since this is now equal to the impedance looking out of the inverting input ($R_F \| R_G$), the circuit will cancel the gains for the bias currents to the output leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using a 402Ω feedback resistor, this output error will now be less than $3\mu A \bullet 402\Omega = 1.2mV$.

A fine scale output offset null, or DC operating point adjustment, is sometimes required. Numerous techniques are available for introducing a DC offset control into an op amp circuit. Most of these techniques eventually reduce to setting up a DC current through the feedback resistor. One key consideration to selecting a technique is to insure that it has a minimal impact on the desired signal path frequency response. If the signal path is intended to be non-inverting,

the offset control is best applied as an inverting summing signal. If the signal path is intended to be inverting, applying the offset control to the non-inverting input can be considered. For a DC coupled signal, the DC offset signal can, in some configurations, set up a DC current back into the source that must be considered. An adjustment placed on the inverting op amp input can also change the noise gain and frequency response flatness. Figure 8 shows one example of an offset adjustment for a DC coupled signal path that will have minimum impact on the signal frequency response. In this case, the input is brought in to an inverting gain resistor with the DC adjustment an additional current summed into the inverting node. The resistor network setting this current is much larger than the signal path resistors. This will insure that this adjustment has minimal impact on the loop gain and hence the frequency response.
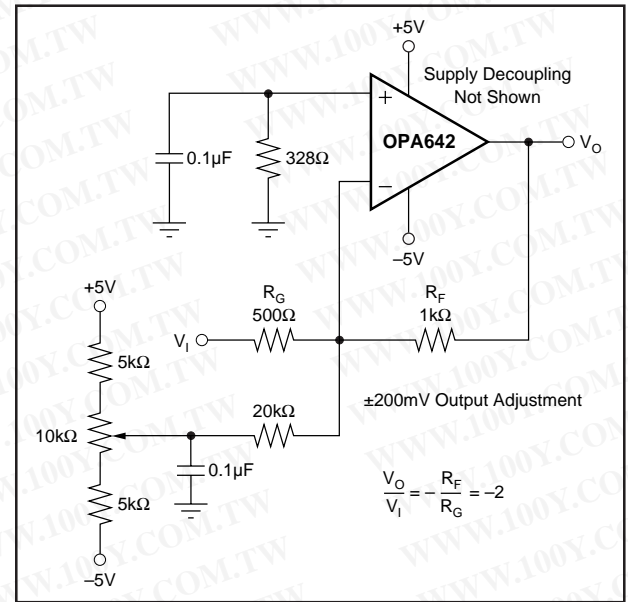

FIGURE 8. DC Coupled, Inverting Gain of –2, with Output Offset Adjustment.

THERMAL ANALYSIS

The OPA642 will not require heatsinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed $175°C$.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

13

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Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst case example, compute the maximum T_J using an OPA642N (SOT23-5 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C. $P_D = 10V \cdot 26mA + 5^2/(4 \cdot (100\Omega \| 804\Omega)) = 330mW$. Maximum $T_J = +85°C + 0.33W \cdot 150°C/W = 135°C$.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high frequency amplifier like the OPA642 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1uF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The primary power supply connections (on pins 4 and 7) should always be decoupled with these capacitors. Optional output stage power supply connections on pins 5 and 8 may be used to get a slight improvement in harmonic distortion and settling time (for the 8-pin packaged parts). Place additional 0.1μF decoupling capacitors very near to these pins to improve performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA642. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as non-inverting input termination resistors, should also be placed close to the package. Where double side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 402Ω feedback used in the typical performance specifications is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short is suggested for the unity gain follower application. This effectively isolates the inverting input capacitance from the output pin that would otherwise cause a slight peaking in the gain of +1 frequency response.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA642 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic cap. loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the Distortion vs Load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA642 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive load. This will not preserve signal integrity as well as a doubly terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high speed part like the OPA642 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA642 onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

INPUT AND ESD PROTECTION

The OPA642 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low due to these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Rating table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 9.
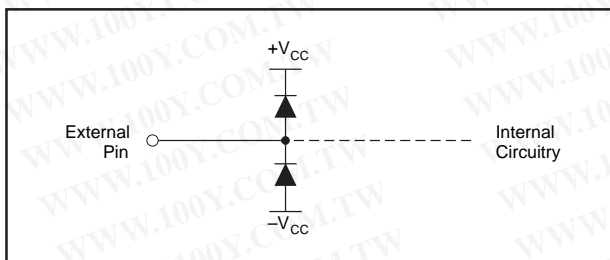

FIGURE 9. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g. in systems with ±15V supply parts driving into the OPA642), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

High input overdrive signals can also cause significant differential voltage between the + and – inputs. Where this voltage can exceed the maximum rated voltage of ±1.2V, external Schottky protection diodes should be added across the two inputs. Again, the capacitance added by these diodes can degrade the noise and AC performance and should be used only where necessary. Figure 9 shows a fully featured input protection circuit for the OPA642. This is the circuit of Figure 1 with additional limiting resistors into the inputs and Schottky clamp diodes across the inputs. These resistor values have been selected to limit the degradation in noise and frequency response, achieve DC bias current cancellation, and limit the current that will flow under overdrive conditions.
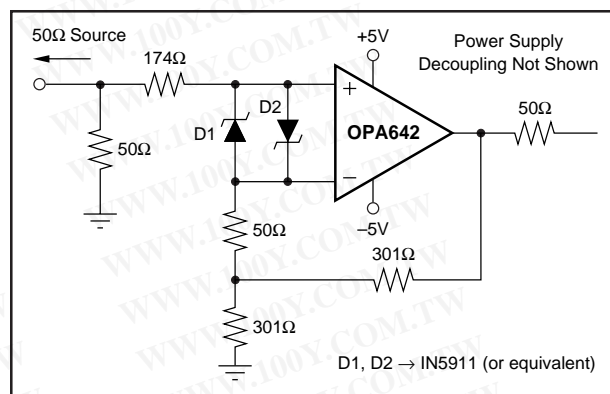

FIGURE 10. Gain of +2 with Input Protection.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Several PC boards are available in the initial evaluation of circuit performance using the OPA642 in its three package styles. Two partially assembled boards are available for sale to support the DIP (P suffix) and SO-8 (U-suffix) packages. These boards come partially assembled with power supply and I/O connectors but do not have the amplifier or resistor networks loaded. Both boards are configured for low distortion, non-inverting amplifier operation. Order these boards by the following part numbers from your local Burr-Brown distributor:

DEM-OPA64XP-N for the OPA642P and OPA642PB (8-pin DIP package)
DEM-OPA64XU-N for the OPA642U and OPA642UB (8-pin SO package)

The SOT23-5 package version of the OPA642 may be evaluated using a single unpopulated board used for numerous SOT23-5 packaged amplifiers available from Burr-Brown. This board is available from the Burr-Brown Literature department as an unpopulated board attached to a descriptive document. This board, the **DEM-OPA6xxN**, is available free by requesting literature number **MKT-348**.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA642 is available through either the Burr-Brown web page (http://www.burr-brown.com) or as a disk from the Burr-Brown Applications Department (1-800-548-6132). The application department is also available for design assistance at this number. These models do a good job of predicting small signal AC and transient performance under a wide variety of operating conditions. They do not do as good a job in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small signal AC performance.

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