

# Am29F016

## 16-Megabit (2,097,152 x 8-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

### DISTINCTIVE CHARACTERISTICS

- **5.0 Volt  $\pm$  10% for read and write operations**
  - Minimizes system level power requirements
- **Compatible with JEDEC-standards**
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection
- **48-pin TSOP**
- **44-pin SO**
- **Minimum 100,000 write/erase cycles guaranteed**
- **High performance**
  - 70 ns maximum access time
- **Sector erase architecture**
  - Uniform sectors of 64 Kbytes each
  - Any combination of sectors can be erased. Also supports full chip erase
- **Group sector protection**
  - Hardware method that disables any combination of sector groups from write or erase operations (a sector group consists of 4 adjacent sectors of 64 Kbytes each)
- **Embedded Erase Algorithms**
  - Automatically pre-programs and erases the chip or any sector
- **Embedded Program Algorithms**
  - Automatically programs and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/ $\overline{\text{Busy}}$  output ( $\text{RY}/\overline{\text{BY}}$ )**
  - Hardware method for detection of program or erase cycle completion
- **Erase Suspend/Resume**
  - Supports **reading or programming** data to a sector not being erased
- **Low power consumption**
  - 25 mA typical active read current
  - 30 mA typical program/erase current
- **Enhanced power management for standby mode**
  - $<1 \mu\text{A}$  typical standby current
  - Standard access time from standby mode
- **Hardware  $\overline{\text{RESET}}$  pin**
  - Resets internal state machine to the read mode

### GENERAL DESCRIPTION

The Am29F016 is a 16 Mbit, 5.0 Volt-only Flash memory organized as 2 Megabytes of 8 bits each. The 2 Mbytes of data is divided into 32 sectors of 64 Kbytes for flexible erase capability. The 8 bits of data appear on DQ0–DQ7. The Am29F016 is offered in 48-pin TSOP and 44-pin SO packages. This device is designed to be programmed in-system with the standard system 5.0 Volt  $V_{CC}$  supply. 12.0 Volt  $V_{PP}$  is not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard Am29F016 offers access times of 70 ns, 90 ns, 120 ns, and 150 ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention, the device has separate

chip enable ( $\overline{\text{CE}}$ ), write enable ( $\overline{\text{WE}}$ ), and output enable ( $\overline{\text{OE}}$ ) controls.

The Am29F016 is entirely command set compatible with the JEDEC single-power supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 Volt Flash or EPROM devices.

The Am29F016 is programmed by executing the program command sequence. This will invoke the Embed-

ded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This device also features a sector erase architecture. This allows for sectors of memory to be erased and re-programmed without affecting the data contents of other sectors. A sector is typically erased and verified within one second. The Am29F016 is erased when shipped from the factory.

The Am29F016 device also features hardware sector group protection. This feature will disable both program and erase operations in any combination of eight sector groups of memory. A sector group consists of four adjacent sectors grouped in the following pattern: sectors 0–3, 4–7, 8–11, 12–15, 16–19, 20–23, 24–27, and 28–31.

AMD has implemented an Erase Suspend feature that enables the user to put erase on hold for any period of time to read data from, or program data to, a sector that was not being erased. Thus, true background erase can be achieved.

The device features single 5.0 Volt power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V<sub>CC</sub> detector automatically inhibits write operations during power transitions. The end of program or erase is detected by the RY/BY pin, Data Polling of DQ7, or by the Toggle Bit I (DQ6). Once the end of a program or erase cycle has been completed, the device automatically resets to the read mode.

The Am29F016 also has a hardware RESET pin. When this pin is driven low, execution of any Embedded Program Algorithm or Embedded Erase Algorithm will be terminated. The internal state machine will then be reset into the read mode. The RESET pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during the Embedded Program Algorithm or Embedded Erase Algorithm, the device will be automatically reset to the read mode. This will enable the system's microprocessor to read the boot-up firmware from the Flash memory.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the

highest levels of quality, reliability and cost effectiveness. The Am29F016 memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

### Flexible Sector-Erase Architecture

- Thirty two 64 Kbyte sectors
- Eight sector groups each of which consists of 4 adjacent sectors in the following pattern: sectors 0–3, 4–7, 8–11, 12–15, 16–19, 20–23, 24–27, and 28–31.
- Individual-sector or multiple-sector erase capability
- Sector group protection is user-definable

|                  |          |           |                  |
|------------------|----------|-----------|------------------|
| SA31             | 64 Kbyte | 1FFFFFFh  | } Sector Group 7 |
| SA30             | 64 Kbyte | 1EFFFFFFh |                  |
| SA29             | 64 Kbyte | 1DFFFFFFh |                  |
| SA28             | 64 Kbyte | 1CFFFFFFh |                  |
| 32 Sectors Total |          | 1BFFFFFFh |                  |
|                  |          | 1AFFFFFFh |                  |
|                  |          | 19FFFFFFh |                  |
|                  |          | 18FFFFFFh |                  |
|                  |          | 17FFFFFFh |                  |
|                  |          | 16FFFFFFh |                  |
|                  |          | 15FFFFFFh |                  |
|                  |          | 14FFFFFFh |                  |
|                  |          | 13FFFFFFh |                  |
|                  |          | 12FFFFFFh |                  |
|                  |          | 11FFFFFFh |                  |
|                  |          | 10FFFFFFh |                  |
|                  |          | 1FFFFFFh  |                  |
|                  |          | 1EFFFFFFh |                  |
|                  |          | 1DFFFFFFh |                  |
|                  |          | 1CFFFFFFh |                  |
|                  |          | 1BFFFFFFh |                  |
|                  |          | 1AFFFFFFh |                  |
|                  |          | 09FFFFFFh |                  |
|                  |          | 08FFFFFFh |                  |
|                  |          | 07FFFFFFh |                  |
|                  |          | 06FFFFFFh |                  |
|                  |          | 05FFFFFFh |                  |
|                  |          | 04FFFFFFh |                  |
|                  |          | 03FFFFFFh |                  |
| SA3              | 64 Kbyte | 02FFFFFFh | } Sector Group 0 |
| SA2              | 64 Kbyte | 01FFFFFFh |                  |
| SA1              | 64 Kbyte | 00FFFFFFh |                  |
| SA0              | 64 Kbyte | 000000h   |                  |

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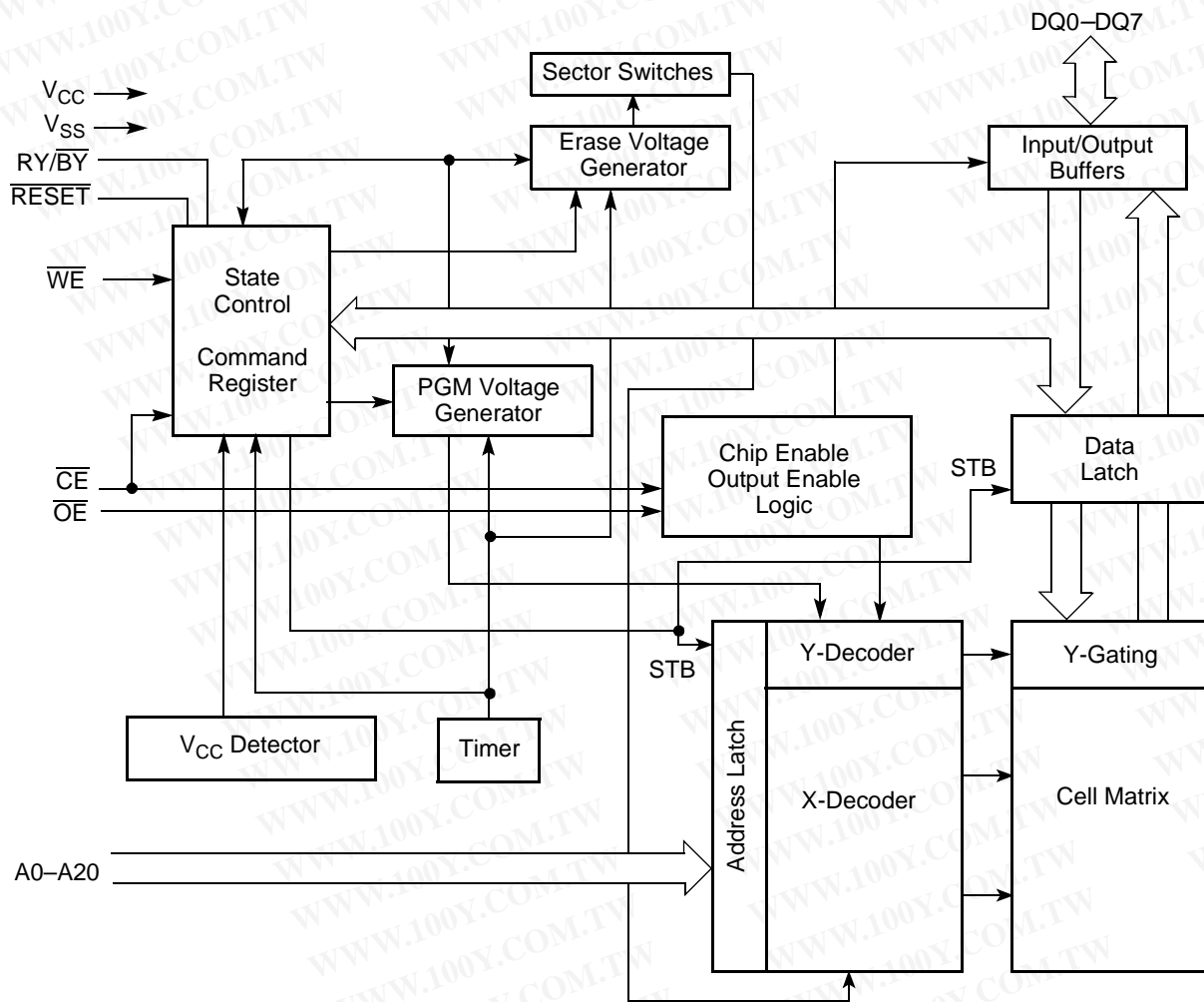
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## PRODUCT SELECTOR GUIDE

| Family Part No.   |            |            |             |             |
|---|------------|------------|-------------|-------------|
| Ordering Part No: $V_{CC} = 5.0 \text{ Volt} \pm 5\%$<br>$V_{CC} = 5.0 \text{ Volt} \pm 10\%$ | <b>-75</b> |            |             |             |
|   |            | <b>-90</b> | <b>-120</b> | <b>-150</b> |
| Max Access Time (ns)  | 70         | 90         | 120         | 150         |
| $\overline{CE}$ ( $\overline{E}$ ) Access (ns)  | 70         | 90         | 120         | 150         |
| $\overline{OE}$ ( $\overline{G}$ ) Access (ns)  | 40         | 40         | 50          | 75          |

## BLOCK DIAGRAM

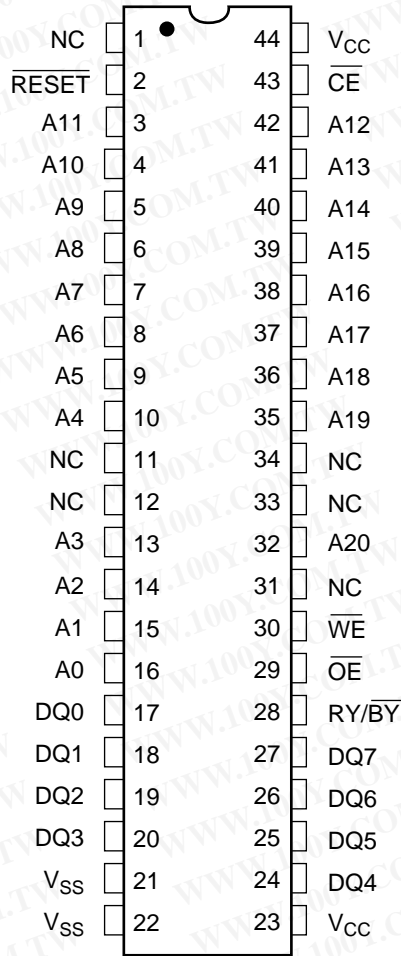


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SO



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CONNECTION DIAGRAMS



Standard TSOP

18805D-3



Reverse TSOP

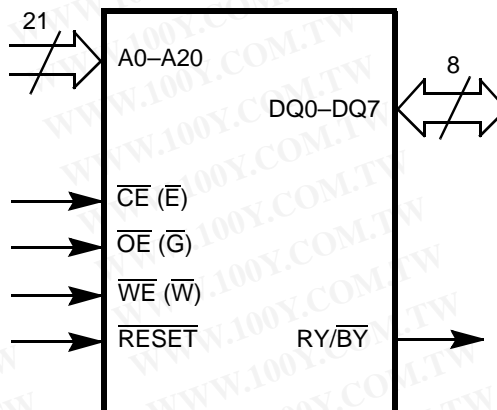
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**PIN CONFIGURATION**

- A0–A20 = 21 Addresses
- $\overline{CE}$  = Chip Enable
- DQ0–DQ7 = 8 Data Inputs/Outputs
- NC = Pin Not Connected Internally
- $\overline{OE}$  = Output Enable
- $\overline{RESET}$  = Hardware Reset Pin, Active Low
- RY/ $\overline{BY}$  = Ready/ $\overline{BUSY}$  Output
- V<sub>CC</sub> = +5.0 Volt Single-Power Supply  
(±10% for -90, -120, -150) or  
(±5% for -95)
- V<sub>SS</sub> = Device Ground
- $\overline{WE}$  = Write Enable

**LOGIC SYMBOL**



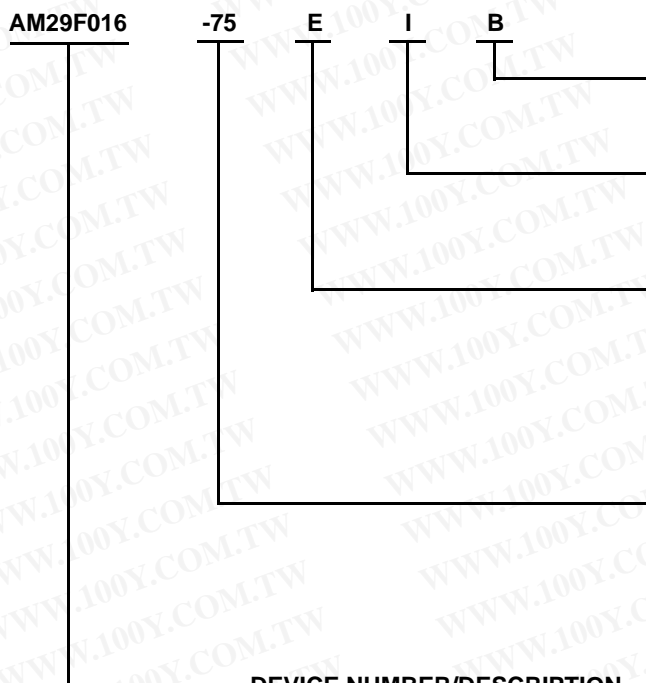
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## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



#### OPTIONAL PROCESSING

Blank = Standard Processing  
B = Burn-In

#### TEMPERATURE RANGE

C = Commercial (0°C to +70°C)  
I = Industrial (-40°C to +85°C)

#### PACKAGE TYPE

E = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 048)  
F = 48-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR048)  
S = 44-Pin Small Outline Package (SO 044)

#### SPEED OPTION

See Product Selector Guide and Valid Combinations

#### DEVICE NUMBER/DESCRIPTION

Am29F016  
16 Megabit (2M x 8-Bit) CMOS Flash Memory  
5.0 Volt-only Program and Erase

| Valid Combinations |  |
|--------------------|--|
| AM29F016-75        | EC, EI, FC, FI, SC, SI                                     |
| AM29F016-90        |  |
| AM29F016-120       | EC, ECB, EI, EIB,<br>FC, FCB, FI, FIB,<br>SC, SCB, SI, SIB |
| AM29F016-150       |  |

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

**Table 1. Am29F016 User Bus Operations**

| Operation                        | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | A0 | A1 | A6 | A9              | DQ0–DQ7          | $\overline{RESET}$ |
|----------------------------------|-----------------|-----------------|-----------------|----|----|----|-----------------|------------------|--------------------|
| Autoselect, AMD Manuf. Code (1)  | L               | L               | H               | L  | L  | L  | V <sub>ID</sub> | Code             | H                  |
| Autoselect Device Code (1)       | L               | L               | H               | H  | L  | L  | V <sub>ID</sub> | Code             | H                  |
| Read                             | L               | L               | X               | A0 | A1 | A6 | A9              | D <sub>OUT</sub> | H                  |
| Standby                          | H               | X               | X               | X  | X  | X  | X               | HIGH Z           | H                  |
| Output Disable                   | L               | H               | H               | X  | X  | X  | X               | HIGH Z           | H                  |
| Write                            | L               | H               | L               | A0 | A1 | A6 | A9              | D <sub>IN</sub>  | H                  |
| Enable Sector Group Protect (2)  | L               | V <sub>ID</sub> | L               | X  | X  | X  | V <sub>ID</sub> | X                | H                  |
| Verify Sector Group Protect (2)  | L               | L               | H               | L  | H  | L  | V <sub>ID</sub> | Code             | H                  |
| Temporary Sector Group Unprotect | X               | X               | X               | X  | X  | X  | X               | X                | V <sub>ID</sub>    |
| Hardware Reset/Standby           | X               | X               | X               | X  | X  | X  | X               | HIGH Z           | L                  |

**Legend:**

L = logic 0, H = logic 1, X = Don't Care. See DC Characteristics for voltage levels.

**Notes:**

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 5.
2. Refer to the section on Sector Group Protection.

## Read Mode

The Am29F016 has two control functions which must be satisfied in order to obtain data at the outputs.  $\overline{CE}$  is the power control and should be used for device selection.  $\overline{OE}$  is the output control and should be used to gate data to the output pins if the device is selected.

Address access time ( $t_{ACC}$ ) is equal to the delay from stable addresses to valid output data. The chip enable access time ( $t_{CE}$ ) is the delay from stable addresses and stable  $\overline{CE}$  to valid data at the output pins. The output enable access time is the delay from the falling edge of  $\overline{OE}$  to valid data at the output pins (assuming the addresses have been stable for at least  $t_{ACC}-t_{OE}$  time).

## Standby Mode

There are two ways to implement the standby mode on the Am29F016 device, one using both the  $\overline{CE}$  and  $\overline{RESET}$  pins; the other via the  $\overline{RESET}$  pin only.

When using both pins, a CMOS standby mode is achieved with  $\overline{CE}$  and  $\overline{RESET}$  inputs both held at  $V_{CC} \pm 0.3$  V. Under this condition the current is typically

reduced to less than 1  $\mu$ A. A TTL standby mode is achieved with  $\overline{CE}$  and  $\overline{RESET}$  pins held at  $V_{IH}$ . Under this condition the current is typically reduced to 200  $\mu$ A. *The device can be read with standard access time ( $t_{CE}$ ) from either of these standby modes.*

When using the  $\overline{RESET}$  pin only, a CMOS standby mode is achieved with  $\overline{RESET}$  input held at  $V_{SS} \pm 0.3$  V ( $\overline{CE}$  = don't care). Under this condition the current is typically reduced to less than 1  $\mu$ A. A TTL standby mode is achieved with  $\overline{RESET}$  pin held at  $V_{IL}$  ( $\overline{CE}$  = don't care). Under this condition the current is typically reduced to less than 200  $\mu$ A. Once the  $\overline{RESET}$  pin is taken high, the device requires 50 ns of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the  $\overline{OE}$  input.

## Output Disable

With the  $\overline{OE}$  input at a logic high level ( $V_{IH}$ ), output from the device is disabled. This will cause the output pins to be in a high impedance state.

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## Autoselect

The autoselect mode allows the reading of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force  $V_{ID}$  (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from  $V_{IL}$  to  $V_{IH}$ . All addresses are don't cares except A0, A1, and A6 (see Table 2).

The manufacturer and device codes may also be read via the command register, for instances when the Am29F016 is erased or programmed in a system without access to high voltage on the A9 pin. The command

sequence is illustrated in Table 5 (see Autoselect Command Sequence).

Byte 0 ( $A0 = V_{IL}$ ) represents the manufacturer's code ( $AMD = 01H$ ) and byte 1 ( $A0 = V_{IH}$ ) the device identifier code for Am29F016 = ADH. These two bytes are given in the table below. All identifiers for manufacturer and device will exhibit odd parity with DQ7 defined as the parity bit. In order to read the proper device codes when executing the Autoselect, A1 must be  $V_{IL}$  (see Table 2).

The autoselect mode also facilitates the determination of sector group protection in the system. By performing a read operation at the address location XX02H with the higher order address bits A18, A19, and A20 set to the desired sector group address, the device will return 01H for a protected sector group and 00H for a non-protected sector group.

**Table 2. Am29F016 Sector Protection Verify Autoselect Codes**

| Type                    | A18 to A20           |   |   | A6       | A1       | A0       | Code (HEX) | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |
|-------------------------|----------------------|---|---|----------|----------|----------|------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Manufacturer Code—AMD   | X                    | X | X | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | 01H        | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| Am29F016 Device         | X                    | X | X | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | ADH        | 1   | 0   | 1   | 0   | 1   | 1   | 0   | 1   |
| Sector Group Protection | Sector Group Address |   |   | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | 01H*       | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

\* Outputs 01H at protected sector addresses

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**Table 3. Sector Address Table**

|      | A20 | A19 | A18 | A17 | A16 | Address Range    |
|------|-----|-----|-----|-----|-----|------------------|
| SA0  | 0   | 0   | 0   | 0   | 0   | 000000h-00FFFFh  |
| SA1  | 0   | 0   | 0   | 0   | 1   | 010000h-01FFFFh  |
| SA2  | 0   | 0   | 0   | 1   | 0   | 020000h-02FFFFh  |
| SA3  | 0   | 0   | 0   | 1   | 1   | 030000h-03FFFFh  |
| SA4  | 0   | 0   | 1   | 0   | 0   | 040000h-04FFFFh  |
| SA5  | 0   | 0   | 1   | 0   | 1   | 050000h-05FFFFh  |
| SA6  | 0   | 0   | 1   | 1   | 0   | 060000h-06FFFFh  |
| SA7  | 0   | 0   | 1   | 1   | 1   | 070000h-07FFFFh  |
| SA8  | 0   | 1   | 0   | 0   | 0   | 080000h-08FFFFh  |
| SA9  | 0   | 1   | 0   | 0   | 1   | 090000h-09FFFFh  |
| SA10 | 0   | 1   | 0   | 1   | 0   | 0A0000h-0AFFFFFh |
| SA11 | 0   | 1   | 0   | 1   | 1   | 0B0000h-0BFFFFh  |
| SA12 | 0   | 1   | 1   | 0   | 0   | 0C0000h-0CFFFFh  |
| SA13 | 0   | 1   | 1   | 0   | 1   | 0D0000h-0DFFFFh  |
| SA14 | 0   | 1   | 1   | 1   | 0   | 0E0000h-0EFFFFh  |
| SA15 | 0   | 1   | 1   | 1   | 1   | 0F0000h-0FFFFFh  |
| SA16 | 1   | 0   | 0   | 0   | 0   | 100000h-10FFFFh  |
| SA17 | 1   | 0   | 0   | 0   | 1   | 110000h-11FFFFh  |
| SA18 | 1   | 0   | 0   | 1   | 0   | 120000h-12FFFFh  |
| SA19 | 1   | 0   | 0   | 1   | 1   | 130000h-13FFFFh  |
| SA20 | 1   | 0   | 1   | 0   | 0   | 140000h-14FFFFh  |
| SA21 | 1   | 0   | 1   | 0   | 1   | 150000h-15FFFFh  |
| SA22 | 1   | 0   | 1   | 1   | 0   | 160000h-16FFFFh  |
| SA23 | 1   | 0   | 1   | 1   | 1   | 170000h-17FFFFh  |
| SA24 | 1   | 1   | 0   | 0   | 0   | 180000h-18FFFFh  |
| SA25 | 1   | 1   | 0   | 0   | 1   | 190000h-19FFFFh  |
| SA26 | 1   | 1   | 0   | 1   | 0   | 1A0000h-1AFFFFFh |
| SA27 | 1   | 1   | 0   | 1   | 1   | 1B0000h-1BFFFFh  |
| SA28 | 1   | 1   | 1   | 0   | 0   | 1C0000h-1CFFFFh  |
| SA29 | 1   | 1   | 1   | 0   | 1   | 1D0000h-1DFFFFh  |
| SA30 | 1   | 1   | 1   | 1   | 0   | 1E0000h-1EFFFFh  |
| SA31 | 1   | 1   | 1   | 1   | 1   | 1F0000h-1FFFFFFh |

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Table 4. Sector Group Addresses

|      | A20 | A19 | A18 | Sectors   |
|------|-----|-----|-----|-----------|
| SGA0 | 0   | 0   | 0   | SA0–SA3   |
| SGA1 | 0   | 0   | 1   | SA4–SA7   |
| SGA2 | 0   | 1   | 0   | SA8–SA11  |
| SGA3 | 0   | 1   | 1   | SA12–SA15 |
| SGA4 | 1   | 0   | 0   | SA16–SA19 |
| SGA5 | 1   | 0   | 1   | SA20–SA23 |
| SGA6 | 1   | 1   | 0   | SA24–SA27 |
| SGA7 | 1   | 1   | 1   | SA28–SA31 |

## Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written to by bringing  $\overline{WE}$  to  $V_{IL}$ , while  $\overline{CE}$  is at  $V_{IL}$  and  $\overline{OE}$  is at  $V_{IH}$ . Addresses are latched on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever happens later; while data is latched on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

## Sector Group Protection

The Am29F016 features hardware sector group protection. This feature will disable both program and erase operations in any combination of eight sector groups of memory. Each sector group consists of four adjacent sectors grouped in the following pattern: sectors 0–3, 4–7, 8–11, 12–15, 16–19, 20–23, 24–27, and 28–31 (see Table 4). The sector group protect feature is enabled using programming equipment at the user's site. The device is shipped with all sector groups unprotected. Alternatively, AMD may program and protect sector groups in the factory prior to shipping the device (AMD's ExpressFlash™ Service).

It is possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order address bits A18, A19, and A20 is the desired sector group address, will produce a logical "1" at DQ0 for a protected sector group. See Table 2 for Autoselect codes.

## Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups of the Am29F016 device in order to change data in-system. The Sector Group Unprotect mode is activated by setting the  $\overline{RESET}$  pin to high voltage (12V). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the 12 V is taken away from the  $\overline{RESET}$  pin, all the previously protected sector groups will be protected again. Refer to Figures 15 and 16.

## Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. **Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode.** Table 5 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Moreover, both Reset/Read commands are functionally equivalent, resetting the device to the read mode.

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Table 5. Am29F016 Command Definitions

| Command Sequence Read/Reset | Bus Write Cycles Req'd | First Bus Write Cycle |      | Second Bus Write Cycle |      | Third Bus Write Cycle |      | Fourth Bus Read/Write Cycle |      | Fifth Bus Write Cycle |      | Sixth Bus Write Cycle |      |
|-----------------------------|------------------------|-----------------------|------|------------------------|------|-----------------------|------|-----------------------------|------|-----------------------|------|-----------------------|------|
|                             |                        | Addr                  | Data | Addr                   | Data | Addr                  | Data | Addr                        | Data | Addr                  | Data | Addr                  | Data |
| Reset/Read                  | 1                      | XXXXH                 | F0H  |                        |      |                       |      |                             |      |                       |      |                       |      |
| Reset/Read                  | 3                      | 5555H                 | AAH  | 2AAAH                  | 55H  | 5555H                 | F0H  | RA                          | RD   |                       |      |                       |      |
| Autoselect                  | 3                      | 5555H                 | AAH  | 2AAAH                  | 55H  | 5555H                 | 90H  |                             |      |                       |      |                       |      |
| Byte Program                | 4                      | 5555H                 | AAH  | 2AAAH                  | 55H  | 5555H                 | A0H  | PA                          | Data |                       |      |                       |      |
| Chip Erase                  | 6                      | 5555H                 | AAH  | 2AAAH                  | 55H  | 5555H                 | 80H  | 5555H                       | AAH  | 2AAAH                 | 55H  | 5555H                 | 10H  |
| Sector Erase                | 6                      | 5555H                 | AAH  | 2AAAH                  | 55H  | 5555H                 | 80H  | 5555H                       | AAH  | 2AAAH                 | 55H  | SA                    | 30H  |
| Erase Suspend               | 1                      | XXXXH                 | B0H  |                        |      |                       |      |                             |      |                       |      |                       |      |
| Erase Resume                | 1                      | XXXXH                 | 30H  |                        |      |                       |      |                             |      |                       |      |                       |      |

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**Notes:**

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.  
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the  $\overline{WE}$  pulse.  
SA = Address of the sector to be erased. The combination of A20, A19, A18, A17, and A16 will uniquely select any sector.
3. RD = Data read from location RA during read operation.  
PD = Data to be programmed at location PA. Data is latched on the rising edge of  $\overline{WE}$ .
4. Read and Byte program functions to non-erasing sectors are allowed in the Erase Suspend mode.
5. Address bits A15, A14, A13, A12 and A11 = X, X = don't care.

**Read/Reset Command**

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

**Autoselect Command**

Flash memories are intended for use in applications where the local CPU can alter memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desirable system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming

methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacturer code of 01H. A read cycle from address XX01H returns the device code ADH (see Table 2).

All manufacturer and device codes will exhibit odd parity with DQ7 defined as the parity bit.

Furthermore, the write protect status of sectors can be read in this mode. Scanning the sector group addresses (A18, A19, and A20) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector group.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

**Byte Programming**

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever happens later and the data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever happens first. The rising edge of  $\overline{CE}$  or  $\overline{WE}$  (whichever happens first) begins programming using the Embedded Program Algo-

rithm. Upon executing the algorithm, the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

This automatic programming operation is completed when the data on DQ7 (also used as  $\overline{\text{Data}}$  Polling) is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see Table 6, Write Operation Status). Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time for  $\overline{\text{Data}}$  Polling operations.  $\overline{\text{Data}}$  Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored. If a hardware reset occurs during the programming operation, the data at that particular location will be corrupted.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

## Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last  $\overline{\text{WE}}$  pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

## Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are

then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of  $\overline{\text{WE}}$ , while the command (30H) is latched on the rising edge of  $\overline{\text{WE}}$ . After a time-out of 50  $\mu\text{s}$  from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased sequentially by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50  $\mu\text{s}$  otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50  $\mu\text{s}$  from the rising edge of the last  $\overline{\text{WE}}$  will initiate the execution of the Sector Erase command(s). If another falling edge of the  $\overline{\text{WE}}$  occurs within the 50  $\mu\text{s}$  time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this period will reset the device to the read mode, ignoring the previous command string. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for DQ3, Sector Erase Timer, operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 31).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 50  $\mu\text{s}$  time out from the rising edge of the  $\overline{\text{WE}}$  pulse for the last sector erase command pulse and terminates when the data on DQ7,  $\overline{\text{Data}}$  Polling, is "1" (see Write Operation Status section) at which time the device returns to the read mode.  $\overline{\text{Data}}$  Polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

## Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded

Program Algorithm. Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are “don't-cares” when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 15  $\mu$ s to suspend the erase operation. When the device has entered the erase-suspended mode, the RY/ $\overline{\text{BY}}$  output pin and the DQ7 bit will be at logic '1', and DQ6 will stop toggling. The user must use the address of the erasing sector for reading DQ6 and DQ7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-sus-

pended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ2 to toggle. (See the section on DQ2).

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Byte Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Byte Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause DQ2 to toggle. The end of the erase-suspended program operation is detected by the RY/ $\overline{\text{BY}}$  output pin,  $\overline{\text{Data}}$  Polling of DQ7, or by the Toggle Bit I (DQ6) which is the same as the regular Byte Program operation. Note that DQ7 must be read from the byte program address while DQ6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

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## Write Operation Status

Table 6. Write Operation Status

|                      |   | Status  | DQ7                     | DQ6             | DQ5  | DQ3  | DQ2             |
|----------------------|---|---|-------------------------|-----------------|------|------|-----------------|
| In Progress          | Byte Program in Embedded Program Algorithm          |   | $\overline{\text{DQ7}}$ | Toggle          | 0    | 0    | 1               |
|                      | Embedded Program Algorithm                          |   | 0                       | Toggle          | 0    | 1    | Toggle          |
|                      | Erase Suspended Mode                                | Erase Suspended Read (Erase Suspended Sector)     | 1                       | 1               | 0    | 1    | Toggle (Note 1) |
|                      |   | Erase Suspended Read (Non-Erase Suspended Sector) | Data                    | Data            | Data | Data | Data            |
|                      |   | Erase Suspended Read (Non-Erase Suspended Sector) | $\overline{\text{DQ7}}$ | Toggle (Note 2) | 0    | 1    | 1 (Note 3)      |
| Exceeded Time Limits | Byte Program in Embedded Program Algorithm          |   | $\overline{\text{DQ7}}$ | Toggle          | 1    | 0    | 1               |
|                      | Program/Erase Program in Embedded Program Algorithm |   | 0                       | Toggle          | 1    | 1    | N/A             |
|                      | Erase Suspended Mode                                | Erase Suspended Read (non-Erase Suspended Sector) | $\overline{\text{DQ7}}$ | Toggle          | 1    | 1    | N/A             |

**Notes:**

1. Performing successive read operations from the erase-suspended sector will cause DQ2 to toggle.
2. Performing successive read operations from any address will cause DQ6 to toggle.
3. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic '1' at the DQ2 bit. However, successive reads from the erase-suspended sector will cause DQ2 to toggle.

**DQ7****Data Polling**

The Am29F016 device features  $\overline{\text{Data}}$  Polling as a method to indicate to the host that the embedded algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for  $\overline{\text{Data}}$  Polling (DQ7) is shown in Figure 3.

$\overline{\text{Data}}$  Polling will also flag the entry into Erase Suspend. DQ7 will switch "0" to "1" at the start of the Erase Suspend mode. Please note that the address of an erasing sector must be applied in order to observe DQ7 in the Erase Suspend Mode.

During Program in Erase Suspend,  $\overline{\text{Data}}$  Polling will perform the same as in regular program execution outside of the suspend mode.

For chip erase, the  $\overline{\text{Data}}$  Polling is valid after the rising edge of the sixth  $\overline{\text{WE}}$  pulse in the six write pulse

sequence. For sector erase, the  $\overline{\text{Data}}$  Polling is valid after the last rising edge of the sector erase  $\overline{\text{WE}}$  pulse.  $\overline{\text{Data}}$  Polling must be performed at sector addresses within any of the sectors being erased and **not** a sector that is within a protected sector group. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operations DQ7 may change asynchronously while the output enable ( $\overline{\text{OE}}$ ) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0–DQ7 can be read on the successive read attempts.

The  $\overline{\text{Data}}$  Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend, erase-suspend-program mode, or sector erase time-out (see Table 6).

See Figure 11 for the  $\overline{\text{Data}}$  Polling timing specifications and diagrams.

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**DQ6**

**Toggle Bit I**

The Am29F016 also features the “Toggle Bit I” as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ( $\overline{OE}$  toggling) data from the device *at any address* will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth  $\overline{WE}$  pulse in the four write pulse sequence. For chip erase, the Toggle Bit I is valid after the rising edge of the sixth  $\overline{WE}$  pulse in the six write pulse sequence. For Sector Erase, the Toggle Bit I is valid after the last rising edge of the sector erase  $\overline{WE}$  pulse. The Toggle Bit I is active during the sector erase time out.

Either  $\overline{CE}$  or  $\overline{OE}$  toggling will cause the DQ6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ6 to toggle. See Figure 12 for the Toggle Bit I timing specifications and diagrams.

**DQ5**

**Exceeded Timing Limits**

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The  $\overline{CE}$  circuit will partially power down the device under these conditions (to approximately 2 mA). The  $\overline{OE}$  and  $\overline{WE}$  pins will control the output disable functions as described in Table 1.

The DQ5 failure condition will also appear if a user tries to program a “1” to a location that is previously programmed to “0”. In this case the device locks out and never completes the Embedded Program Algorithm. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a “1.” Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device.

**DQ3**

**Sector Erase Timer**

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. Data Polling and Toggle Bit I are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high (“1”) the internally controlled erase cycle has begun; attempts to write subsequent commands (other than Erase Suspend) to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit I. If DQ3 is low (“0”), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 6: Write Operation Status.

**DQ2**

**Toggle Bit II**

This toggle bit, along with DQ6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspend sector will cause DQ2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic ‘1’ at the DQ2 bit.

DQ6 is different from DQ2 in that DQ6 toggles only when the standard Program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ7, is summarized as follows:

| Mode   | DQ7                  | DQ6     | DQ2     |
|--|----------------------|---------|---------|
| Program  | $\overline{DQ7}$     | toggles | 1       |
| Erase  | 0                    | toggles | toggles |
| Erase Suspend Read (1)<br>(Erase-Suspended Sector) | 1                    | 1       | toggles |
| Erase Suspend Program                              | $\overline{DQ7}$ (2) | toggles | 1 (2)   |

**Notes:**

1. These status flags apply when outputs are read from a sector that has been erase-suspended.
2. These status flags apply when outputs are read from the byte address of the non-erase suspended sector.

For example, DQ2 and DQ6 can be used together to determine the erase-suspend-read mode (DQ2 toggles while DQ6 does not). See also Table 6 and Figure 17.

Furthermore, DQ2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ2 toggles if this bit is read from the erasing sector.

## **$\overline{\text{RY}}/\overline{\text{BY}}$**

### **Ready/Busy**

The Am29F016 provides a  $\overline{\text{RY}}/\overline{\text{BY}}$  open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the  $\overline{\text{RY}}/\overline{\text{BY}}$  pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the Am29F016 is placed in an Erase Suspend mode, the  $\overline{\text{RY}}/\overline{\text{BY}}$  output will be high.

During programming, the  $\overline{\text{RY}}/\overline{\text{BY}}$  pin is driven low after the rising edge of the fourth  $\overline{\text{WE}}$  pulse. During an erase operation, the  $\overline{\text{RY}}/\overline{\text{BY}}$  pin is driven low after the rising edge of the sixth  $\overline{\text{WE}}$  pulse. The  $\overline{\text{RY}}/\overline{\text{BY}}$  pin will indicate a busy condition during the  $\overline{\text{RESET}}$  pulse. Refer to Figure 13 for a detailed timing diagram. The  $\overline{\text{RY}}/\overline{\text{BY}}$  pin is pulled high in standby mode.

Since this is an open-drain output, several  $\overline{\text{RY}}/\overline{\text{BY}}$  pins can be tied together in parallel with a pull-up resistor to  $V_{\text{CC}}$ .

## **$\overline{\text{RESET}}$**

### **Hardware Reset**

The Am29F016 device may be reset by driving the  $\overline{\text{RESET}}$  pin to  $V_{\text{IL}}$ . The  $\overline{\text{RESET}}$  pin must be kept low ( $V_{\text{IL}}$ ) for at least 500 ns. Any operation in progress will be terminated and the internal state machine will be reset to the read mode 20  $\mu\text{s}$  after the  $\overline{\text{RESET}}$  pin is driven low. If a hardware reset occurs during a program operation, the data at that particular location will be indeterminate.

When the  $\overline{\text{RESET}}$  pin is low and the internal reset is complete, the device goes to standby mode and cannot be accessed. Also, note that all the data output pins are tri-stated for the duration of the  $\overline{\text{RESET}}$  pulse. Once the  $\overline{\text{RESET}}$  pin is taken high, the device requires 500 ns of wake up time until outputs are valid for read access.

The  $\overline{\text{RESET}}$  pin may be tied to the system reset input. Therefore, if a system reset occurs during the Embedded Program or Erase Algorithm, the device will be automatically reset to read mode and this will enable the system's microprocessor to read the boot-up firmware from the Flash memory.

## **Data Protection**

The Am29F016 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from  $V_{\text{CC}}$  power-up and power-down transitions or system noise.

### **Low $V_{\text{CC}}$ Write Inhibit**

To avoid initiation of a write cycle during  $V_{\text{CC}}$  power-up and power-down, a write cycle is locked out for  $V_{\text{CC}}$  less than 3.2 V (typically 3.7 V). If  $V_{\text{CC}} < V_{\text{LKO}}$ , the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the  $V_{\text{CC}}$  level is greater than  $V_{\text{LKO}}$ . It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when  $V_{\text{CC}}$  is above 3.2 V.

### **Write Pulse "Glitch" Protection**

Noise pulses of less than 5 ns (typical) on  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  will not initiate a write cycle.

### **Logical Inhibit**

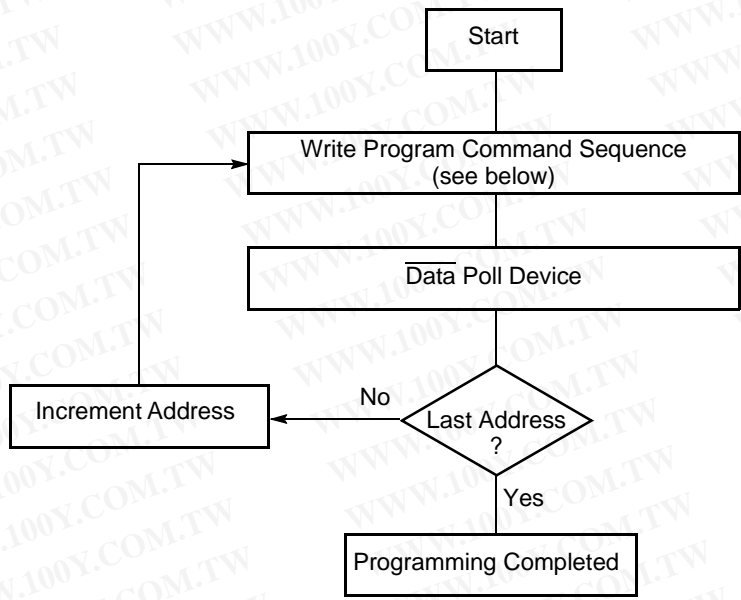
Writing is inhibited by holding any one of  $\overline{\text{OE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IH}}$  or  $\overline{\text{WE}} = V_{\text{IH}}$ . To initiate a write cycle  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be a logical zero while  $\overline{\text{OE}}$  is a logical one.

### **Power-Up Write Inhibit**

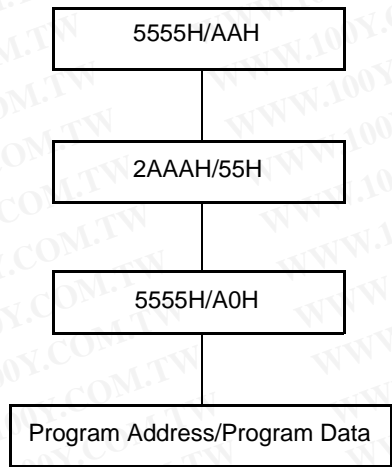
Power-up of the device with  $\overline{\text{WE}} = \overline{\text{CE}} = V_{\text{IL}}$  and  $\overline{\text{OE}} = V_{\text{IH}}$  will not accept commands on the rising edge of  $\overline{\text{WE}}$ . The internal state machine is automatically reset to the read mode on power-up.

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**Program Command Sequence (Address/Command):**

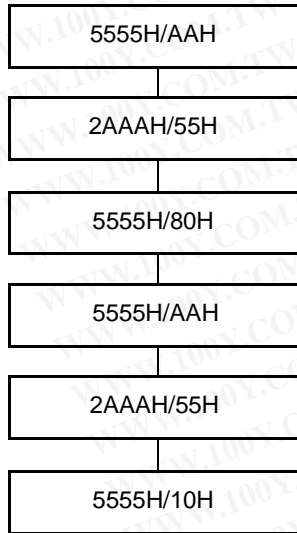


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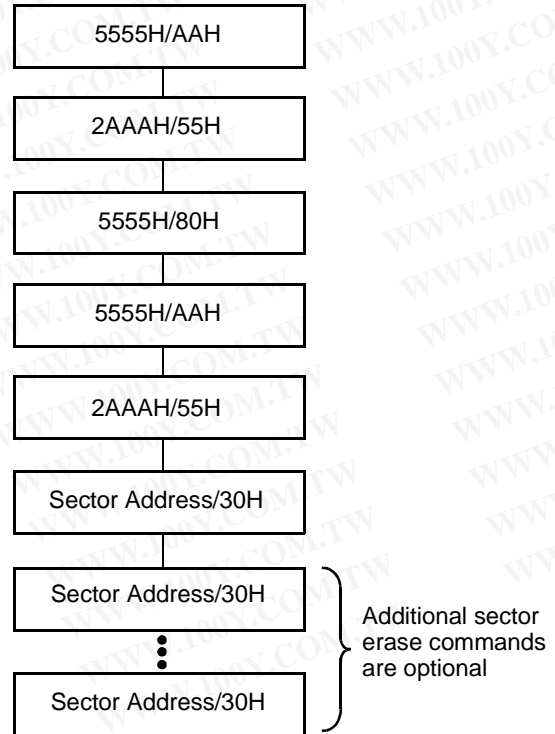
**Figure 1. Embedded Programming Algorithm**



**Chip Erase Command Sequence  
(Address/Command):**



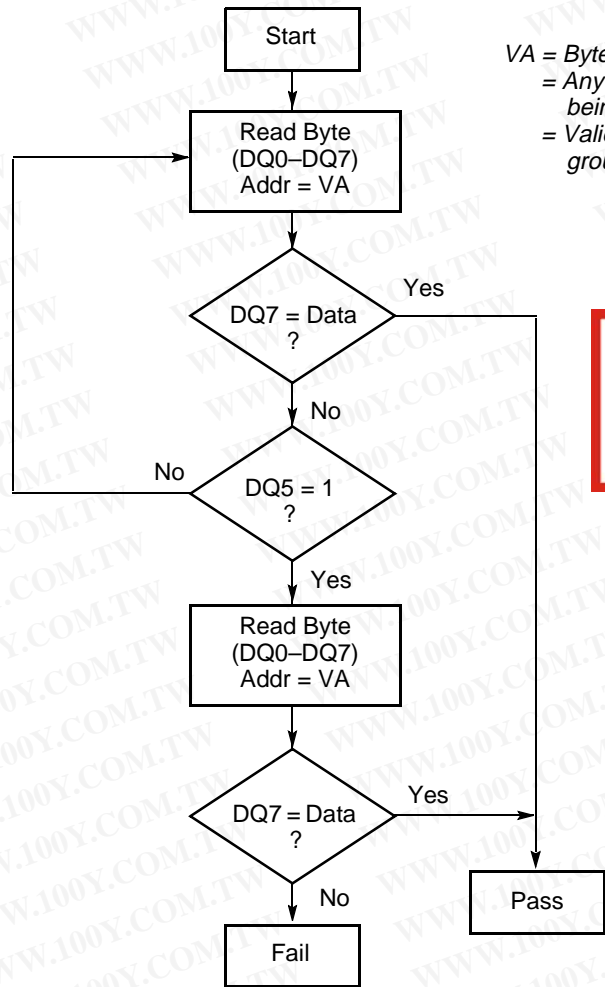
**Individual Sector/Multiple Sector  
Erase Command Sequence  
(Address/Command):**



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To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Figure 2. Embedded Erase Algorithm



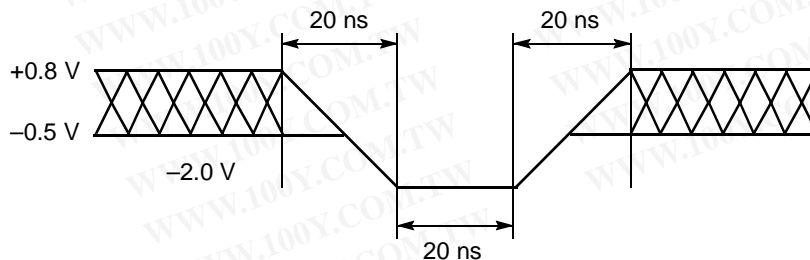
VA = Byte address for programming  
 = Any of the sector addresses within the sector being erased during sector erase operation  
 = Valid address equals any non-protected sector group address during chip erase

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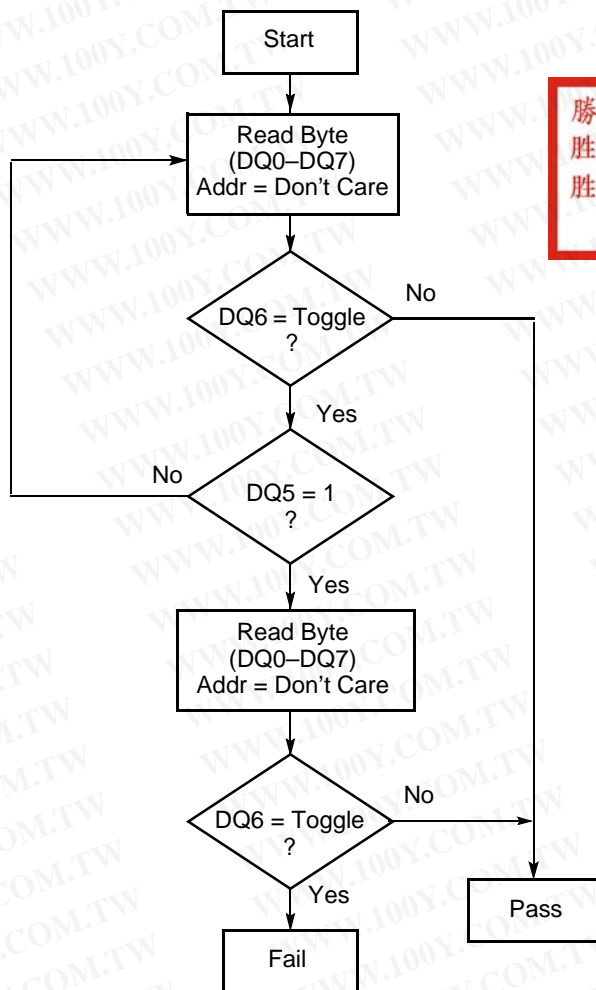
DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure 3. Data Polling Algorithm



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Figure 5. Maximum Negative Overshoot Waveform

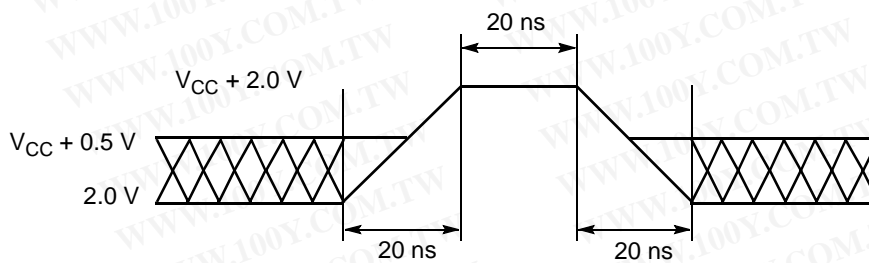


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*DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".*

18805D-9

**Figure 4. Toggle Bit I Algorithm**



18805D-11

**Figure 6. Maximum Positive Overshoot Waveform**

## ABSOLUTE MAXIMUM RATINGS

|   |                   |
|---|-------------------|
| Storage Temperature   |                   |
| Plastic Packages . . . . .                                  | -65°C to +125°C   |
| Ambient Temperature   |                   |
| with Power Applied. . . . .                                 | -55°C to +125°C   |
| Voltage with Respect to Ground                              |                   |
| All pins except A9 (Note 1). . . . .                        | -2.0 V to +7.0 V  |
| V <sub>CC</sub> (Note 1). . . . .                           | -2.0 V to +7.0 V  |
| A9, $\overline{OE}$ , $\overline{RESET}$ (Note 2) . . . . . | -2.0 V to +13.5 V |
| Output Short Circuit Current (Note 3) . . . . .             | 200 mA            |

### Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, inputs may overshoot V<sub>SS</sub> to -2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V<sub>CC</sub> + 0.5 V. During voltage transitions, outputs may overshoot to V<sub>CC</sub> + 2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on A9,  $\overline{OE}$ ,  $\overline{RESET}$  pins is -0.5V. During voltage transitions, A9,  $\overline{OE}$ ,  $\overline{RESET}$  pins may overshoot V<sub>SS</sub> to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the de-

vice to absolute maximum rating conditions for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Case Temperature (T<sub>C</sub>). . . . . 0°C to +70°C

### Industrial (I) Devices

Case Temperature (T<sub>C</sub>). . . . . -40°C to +85°C

### V<sub>CC</sub> Supply Voltages

V<sub>CC</sub> for Am29F016-75 . . . . . +4.75 V to +5.25 V

V<sub>CC</sub> for Am29F016-90, 120, 150. . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

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## DC CHARACTERISTICS

### TTL/NMOS Compatible

| Parameter Symbol | Parameter Description                     | Test Description  | Min  | Max            | Unit    |
|------------------|---|---|------|----------------|---------|
| $I_{LI}$         | Input Load Current                        | $V_{IN} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC}$ Max                         |      | $\pm 1.0$      | $\mu A$ |
| $I_{LIT}$        | A9 Input Load Current                     | $V_{CC} = V_{CC}$ Max, A9 = 12.0 Volt   |      | 50             | $\mu A$ |
| $I_{LO}$         | Output Leakage Current                    | $V_{OUT} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC}$ Max                        |      | $\pm 1.0$      | $\mu A$ |
| $I_{CC1}$        | $V_{CC}$ Active Current (Note 1)          | $\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$                           |      | 40             | mA      |
| $I_{CC2}$        | $V_{CC}$ Active Current (Notes 2, 3)      | $\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$                           |      | 60             | mA      |
| $I_{CC3}$        | $V_{CC}$ Standby Current                  | $V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}$ , $\overline{RESET} = V_{IH}$ |      | 1.0            | mA      |
| $I_{CC4}$        | $V_{CC}$ Standby Current (Reset)          | $V_{CC} = V_{CC}$ Max, $\overline{RESET} = V_{IL}$                            |      | 1.0            | mA      |
| $V_{IL}$         | Input Low Level                           |   | -0.5 | 0.8            | V       |
| $V_{IH}$         | Input High Level                          |   | 2.0  | $V_{CC} + 0.5$ | V       |
| $V_{ID}$         | Voltage for Autoselect and Sector Protect | $V_{CC} = 5.0$ Volt   | 11.5 | 12.5           | V       |
| $V_{OL}$         | Output Low Voltage                        | $I_{OL} = 12$ mA, $V_{CC} = V_{CC}$ Min                                       |      | 0.45           | V       |
| $V_{OH}$         | Output High Level                         | $I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ Min                                      | 2.4  |                | V       |
| $V_{LKO}$        | Low $V_{CC}$ Lock-out Voltage             |   | 3.2  | 4.2            | V       |

#### Notes:

- The  $I_{CC}$  current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 1 mA/MHz, with  $\overline{OE}$  at  $V_{IH}$ .
- $I_{CC}$  active while Embedded Program or Erase Algorithm is in progress.
- Not 100% tested.

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## DC CHARACTERISTICS (continued)

### CMOS Compatible

| Parameter Symbol | Parameter Description                     | Test Description  | Min                 | Typ | Max            | Unit    |
|------------------|---|---|---------------------|-----|----------------|---------|
| $I_{LI}$         | Input Load Current                        | $V_{IN} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC}$ Max   |                     |     | $\pm 1.0$      | $\mu A$ |
| $I_{LIT}$        | A9 Input Load Current                     | $V_{CC} = V_{CC}$ Max, A9 = 12.0 Volt   |                     |     | 50             | $\mu A$ |
| $I_{LO}$         | Output Leakage Current                    | $V_{OUT} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC}$ Max  |                     |     | $\pm 1.0$      | $\mu A$ |
| $I_{CC1}$        | $V_{CC}$ Active Current (Note 1)          | $\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$   |                     | 25  | 40             | mA      |
| $I_{CC2}$        | $V_{CC}$ Active Current (Notes 2, 3)      | $\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$   |                     | 30  | 40             | mA      |
| $I_{CC3}$        | $V_{CC}$ Standby Current                  | $V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.3$ V,<br>$\overline{RESET} = V_{CC} \pm 0.3$ V |                     | 1   | 5              | $\mu A$ |
| $I_{CC4}$        | $V_{CC}$ Standby Current (Reset)          | $V_{CC} = V_{CC}$ Max,<br>$\overline{RESET} = V_{SS} \pm 0.3$ V                                     |                     | 1   | 5              | $\mu A$ |
| $V_{IL}$         | Input Low Level                           |   | -0.5                |     | 0.8            | V       |
| $V_{IH}$         | Input High Level                          |   | $0.7 \times V_{CC}$ |     | $V_{CC} + 0.3$ | V       |
| $V_{ID}$         | Voltage for Autoselect and Sector Protect | $V_{CC} = 5.0$ Volt   | 11.5                |     | 12.5           | V       |
| $V_{OL}$         | Output Low Voltage                        | $I_{OL} = 12$ mA, $V_{CC} = V_{CC}$ Min   |                     |     | 0.45           | V       |
| $V_{OH1}$        | Output High Voltage                       | $I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min   | $0.85 V_{CC}$       |     |                | V       |
| $V_{OH2}$        |   | $I_{OH} = -100$ $\mu A$ , $V_{CC} = V_{CC}$ Min   | $V_{CC} - 0.4$      |     |                | V       |
| $V_{LKO}$        | Low $V_{CC}$ Lock-out Voltage             |   | 3.2                 |     | 4.2            | V       |

#### Notes:

- The  $I_{CC}$  current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 1 mA/MHz, with  $\overline{OE}$  at  $V_{IH}$ .
- $I_{CC}$  active while Embedded Program or Erase Algorithm is in progress.
- Not 100% tested.

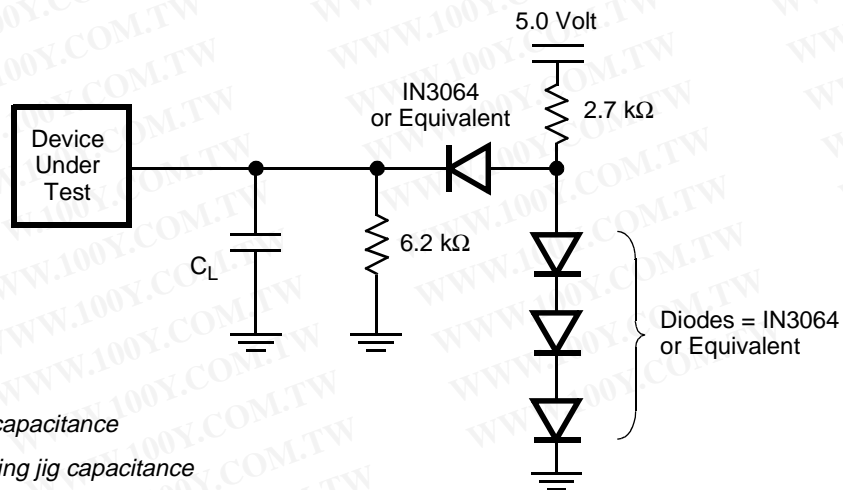
## AC CHARACTERISTICS

### Read-only Operations Characteristics

| Parameter Symbol |             | Parameter Description   | Test Setup   | Speed Options (Notes 1 and 2) |     |      |      | Unit    |
|------------------|-------------|---|--|-------------------------------|-----|------|------|---------|
| JEDEC            | Standard    |   |  | -75                           | -90 | -120 | -150 |         |
| $t_{AVAV}$       | $t_{RC}$    | Read Cycle Time 4   | Min  | 70                            | 90  | 120  | 150  | ns      |
| $t_{AVQV}$       | $t_{ACC}$   | Address to Output Delay   | $\overline{CE} = V_{IL}$<br>$\overline{OE} = V_{IL}$ Max | 70                            | 90  | 120  | 150  | ns      |
| $t_{ELQV}$       | $t_{CE}$    | Chip Enable to Output Delay   | $\overline{OE} = V_{IL}$ Max                             | 70                            | 90  | 120  | 150  | ns      |
| $t_{GLQV}$       | $t_{OE}$    | Output Enable to Output Delay   | Max  | 40                            | 40  | 50   | 55   | ns      |
| $t_{EHQZ}$       | $t_{DF}$    | Chip Enable to Output High Z (Notes 3, 4)   | Max  | 20                            | 20  | 30   | 35   | ns      |
| $t_{GHQZ}$       | $t_{DF}$    | Output Enable to Output High Z (Notes 3, 4)   | Max  | 20                            | 20  | 30   | 35   | ns      |
| $t_{AXQX}$       | $t_{OH}$    | Output Hold Time From Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurs First | Min  | 0                             | 0   | 0    | 0    | ns      |
|                  | $t_{Ready}$ | $\overline{RESET}$ Pin Low to Read Mode 4   | Max  | 20                            | 20  | 20   | 20   | $\mu$ s |

#### Notes:

1. Test Conditions (for -75):  
 Output Load: 1 TTL gate and 30 pF  
 Input rise and fall times: 5 ns  
 Input pulse levels: 0.0 V to 3.0 V  
 Timing measurement reference level: 1.5 V input and output
2. Test Conditions (for all others):  
 Output Load: 1 TTL gate and 100 pF  
 Input rise and fall times: 20 ns  
 Input pulse levels: 0.45 V to 2.4 V  
 Timing measurement reference level: 0.8 V and 2.0 V input and output
3. Output driver disable time.
4. Not 100% tested.



#### Note:

- $C_L$  (for -75) = 30 pF including jig capacitance  
 $C_L$  (for all others) = 100 pF including jig capacitance

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Figure 7. Test Conditions

## AC CHARACTERISTICS




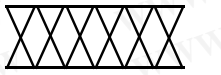
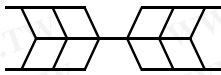
### Write/Erase/Program Operations

| Parameter Symbol |             | Parameter Description  |     | Speed Options (Notes 1 and 2) |     |      |      | Unit    |
|------------------|-------------|--|-----|-------------------------------|-----|------|------|---------|
| JEDEC            | Standard    |  |     | -75                           | -90 | -120 | -150 |         |
| $t_{AVAV}$       | $t_{WC}$    | Write Cycle Time   | Min | 70                            | 90  | 120  | 150  | ns      |
| $t_{AVWL}$       | $t_{AS}$    | Address Setup Time   | Min | 0                             | 0   | 0    | 0    | ns      |
| $t_{WLAX}$       | $t_{AH}$    | Address Hold Time  | Min | 40                            | 45  | 50   | 50   | ns      |
| $t_{DVWH}$       | $t_{DS}$    | Data Setup Time  | Min | 40                            | 45  | 50   | 50   | ns      |
| $t_{WHDX}$       | $t_{DH}$    | Data Hold Time   | Min | 0                             | 0   | 0    | 0    | ns      |
|                  | $t_{OEH}$   | Output Enable Hold Time  | Min | 0                             | 0   | 0    | 0    | ns      |
|                  |             | Read 2<br>Toggle Bit 1 and Data Polling 2  | Min | 10                            | 10  | 10   | 10   | ns      |
| $t_{GHWL}$       | $t_{GHWL}$  | Read Recover Time Before Write<br>( $\overline{OE}$ high to $\overline{WE}$ low) | Min | 0                             | 0   | 0    | 0    | ns      |
| $t_{ELWL}$       | $t_{CS}$    | $\overline{CE}$ Setup Time   | Min | 0                             | 0   | 0    | 0    | ns      |
| $t_{WHEH}$       | $t_{CH}$    | $\overline{CE}$ Hold Time  | Min | 0                             | 0   | 0    | 0    | ns      |
| $t_{WLWH}$       | $t_{WP}$    | Write Pulse Width  | Min | 40                            | 45  | 50   | 50   | ns      |
| $t_{WHWL}$       | $t_{WPH}$   | Write Pulse Width High   | Min | 20                            | 20  | 20   | 20   | ns      |
| $t_{WHWH1}$      | $t_{WHWH1}$ | Byte Programming Operation   | Typ | 7                             | 7   | 7    | 7    | $\mu$ s |
| $t_{WHWH2}$      | $t_{WHWH2}$ | Sector Erase Operation 1   | Typ | 1                             | 1   | 1    | 1    | sec     |
|                  |             |  | Max | 8                             | 8   | 8    | 8    | sec     |
|                  | $t_{VCS}$   | $V_{CC}$ Set Up Time 2   | Min | 50                            | 50  | 50   | 50   | $\mu$ s |
|                  | $t_{VIDR}$  | Rise Time to $V_{ID}$ (Notes 2, 3)   | Min | 500                           | 500 | 500  | 500  | ns      |
|                  | $t_{VLHT}$  | Voltage Transition Time (Notes 2, 3)   | Min | 4                             | 4   | 4    | 4    | $\mu$ s |
|                  | $t_{OESP}$  | $\overline{OE}$ Setup Time to $\overline{WE}$ Active (Notes 2, 3)                | Min | 4                             | 4   | 4    | 4    | $\mu$ s |
|                  | $t_{RP}$    | RESET Pulse Width  | Min | 500                           | 500 | 500  | 500  | ns      |
|                  | $t_{BUSY}$  | Program/Erase Valid to $RY/\overline{BY}$ Delay                                  | Min | 40                            | 40  | 50   | 60   | ns      |

**Notes:**

1. This does not include the preprogramming time.
2. Not 100% tested.
3. These timings are for Temporary Sector Group Unprotect operation.

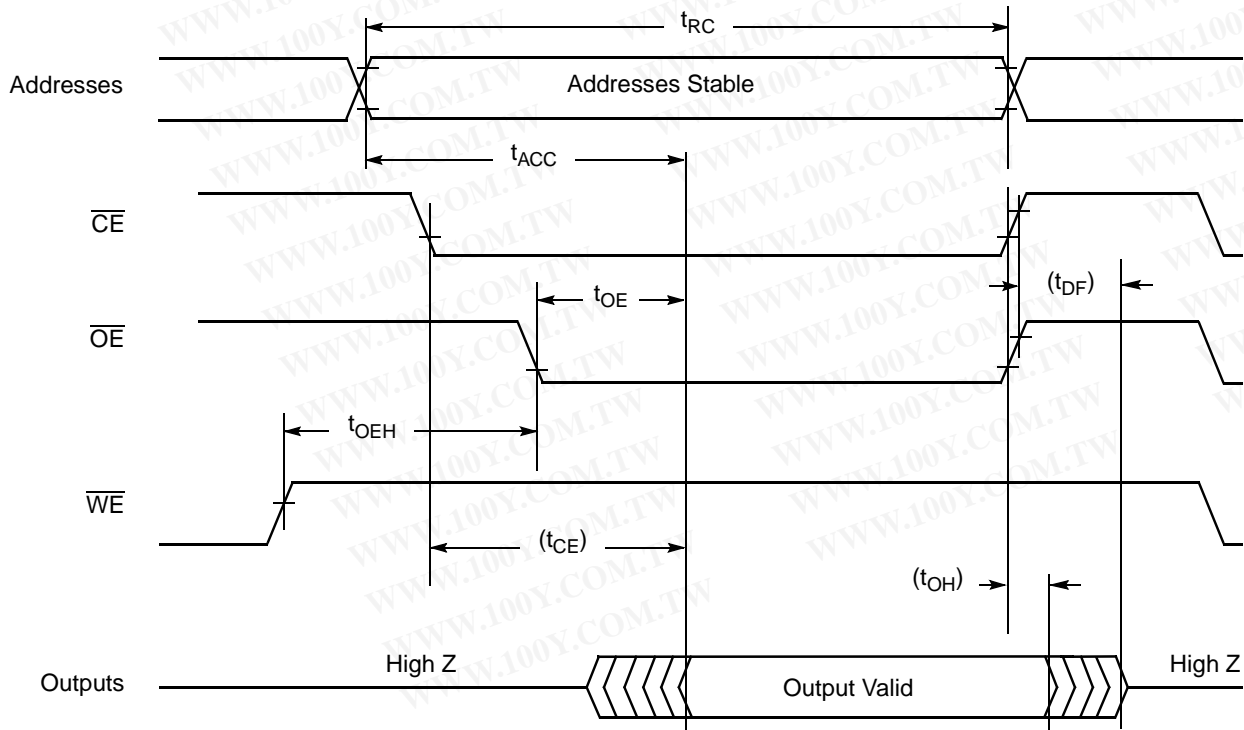
KEY TO SWITCHING WAVEFORMS

| WAVEFORM  | INPUTS                           | OUTPUTS                                   |
|---|----------------------------------|---|
|  | Must be Steady                   | Will be Steady                            |
|  | May Change from H to L           | Will be Changing from H to L              |
|  | May Change from L to H           | Will be Changing from L to H              |
|  | Don't Care, Any Change Permitted | Changing, State Unknown                   |
|  | Does Not Apply                   | Center Line is High-Impedance "Off" State |

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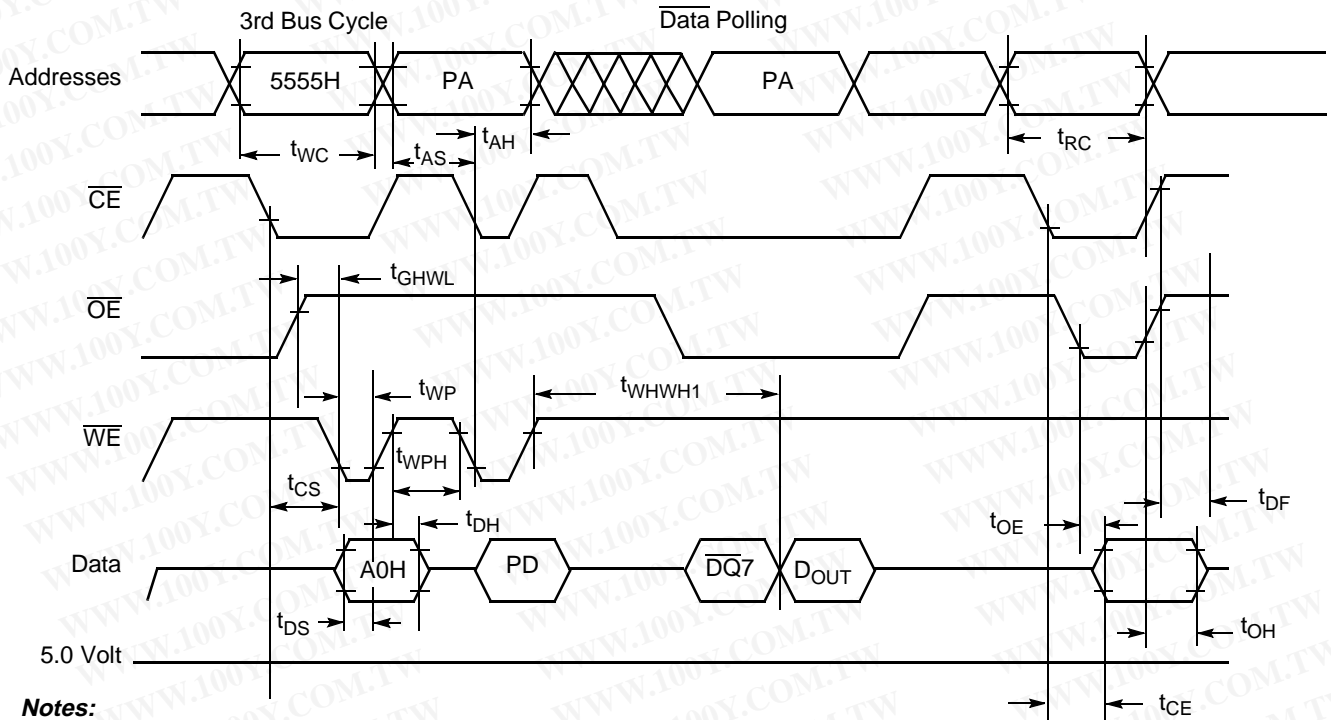
SWITCHING TEST WAVEFORM



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Figure 8. AC Waveforms for Read Operations

SWITCHING WAVEFORMS



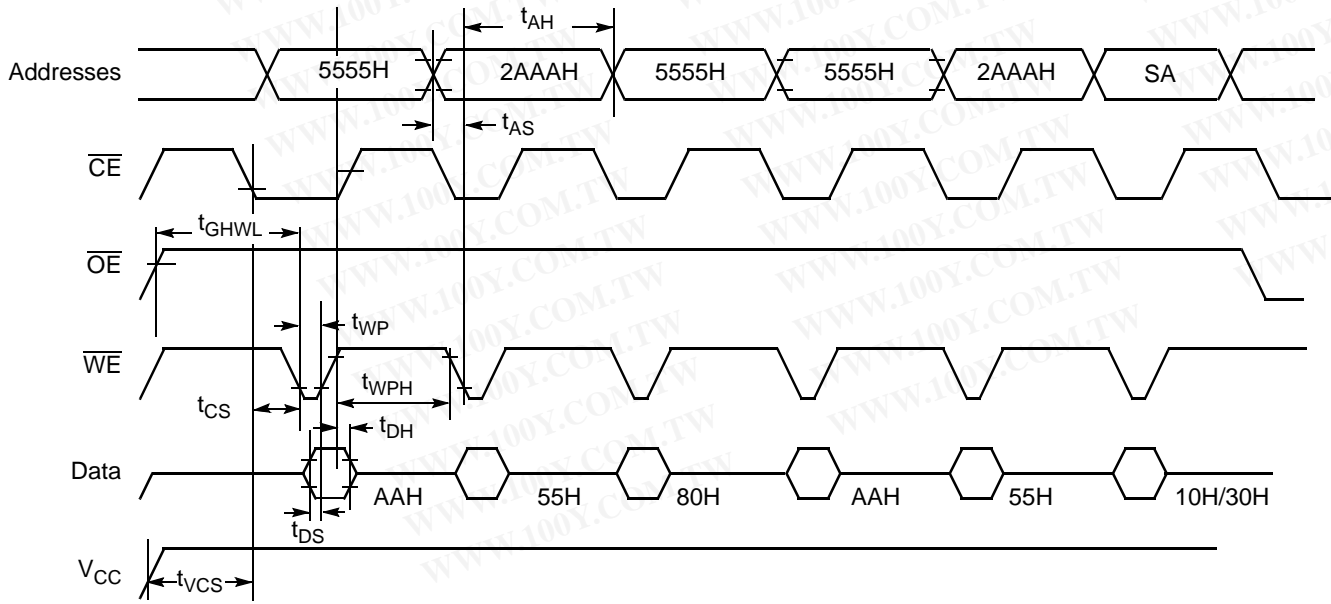
Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3.  $\overline{DQ7}$  is the output of the complement of the data written to the device.
4.  $D_{OUT}$  is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

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Figure 9. Program Operation Timings



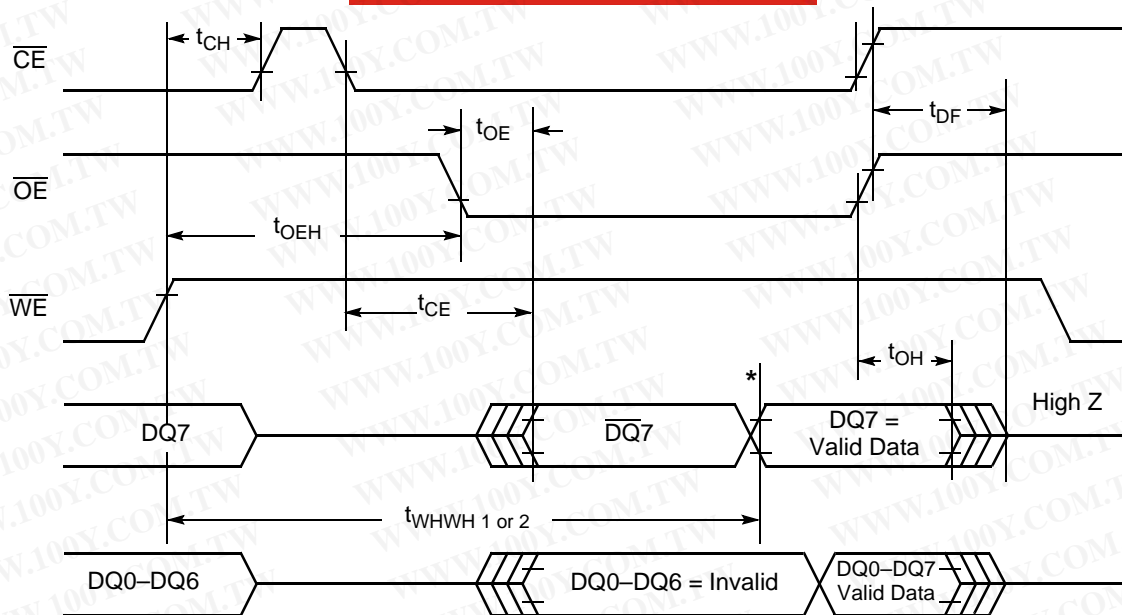
Note:

SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.

18805D-14

Figure 10. AC Waveforms Chip/Sector Erase Operations

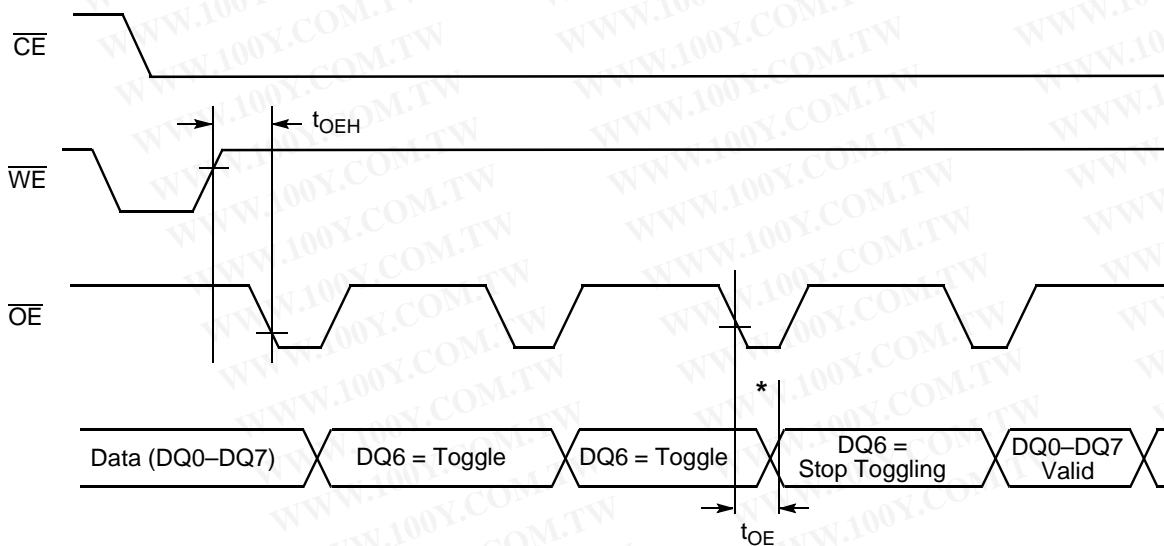
SWITCHING WAVEFORMS



\*DQ7 = Valid Data (The device has completed the Embedded operation).

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Figure 11. AC Waveforms for Data Polling During Embedded Algorithm Operations



\*DQ6 stops toggling (The device has completed the Embedded operation).

18805D-16

Figure 12. AC Waveforms for Toggle Bit I During Embedded Algorithm Operations

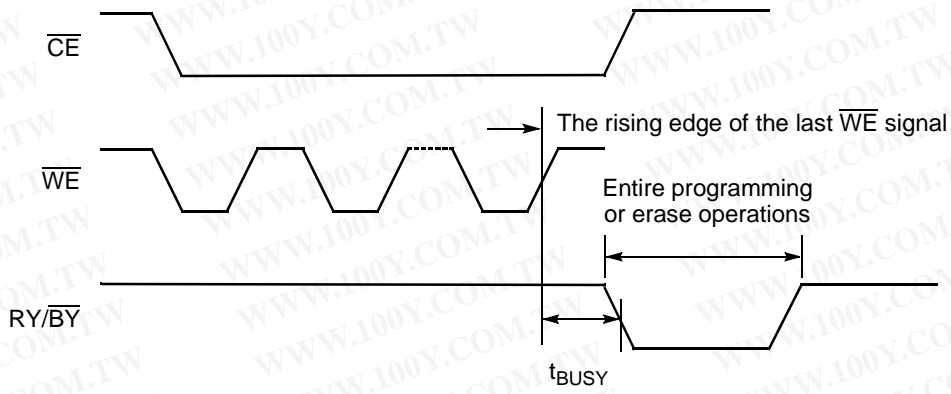


Figure 13. RY/BY Timing Diagram During Program/Erase Operations

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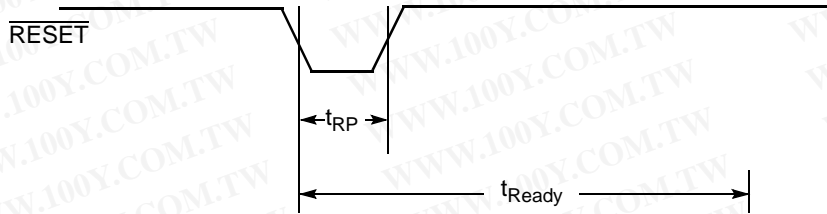
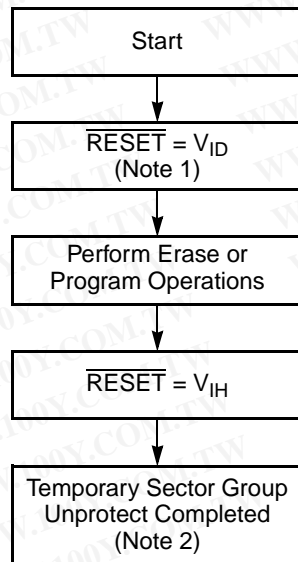


Figure 14. RESET Timing Diagram

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**Notes:**

1. All protected sector groups unprotected.
2. All previously protected sector groups are protected once again.

Figure 15. Temporary Sector Group Unprotect Algorithm

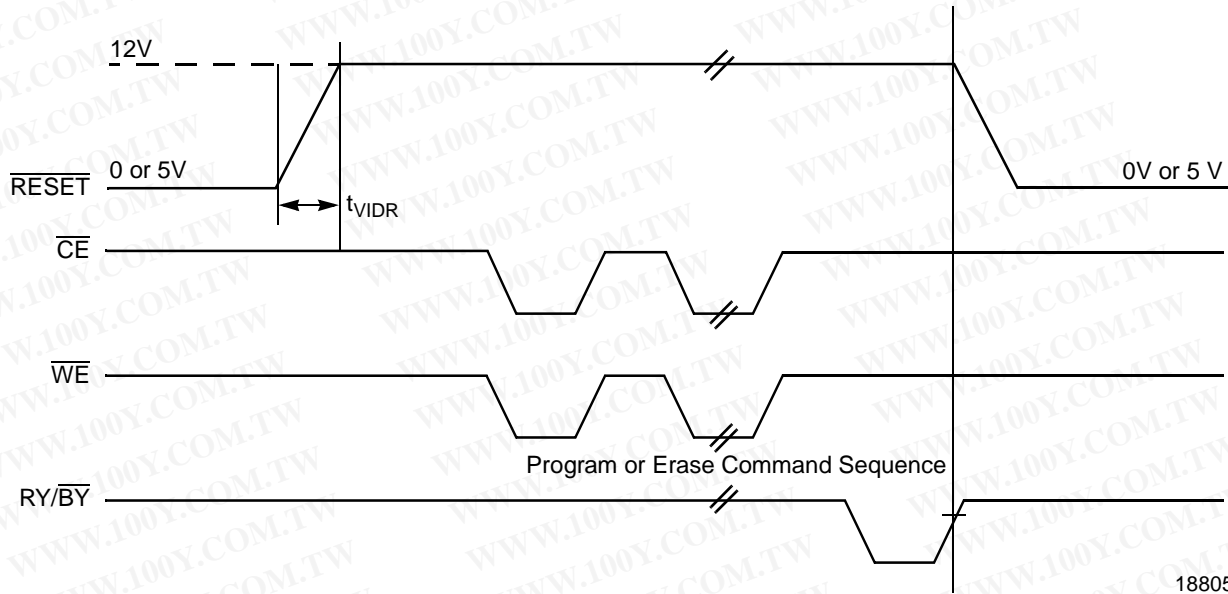
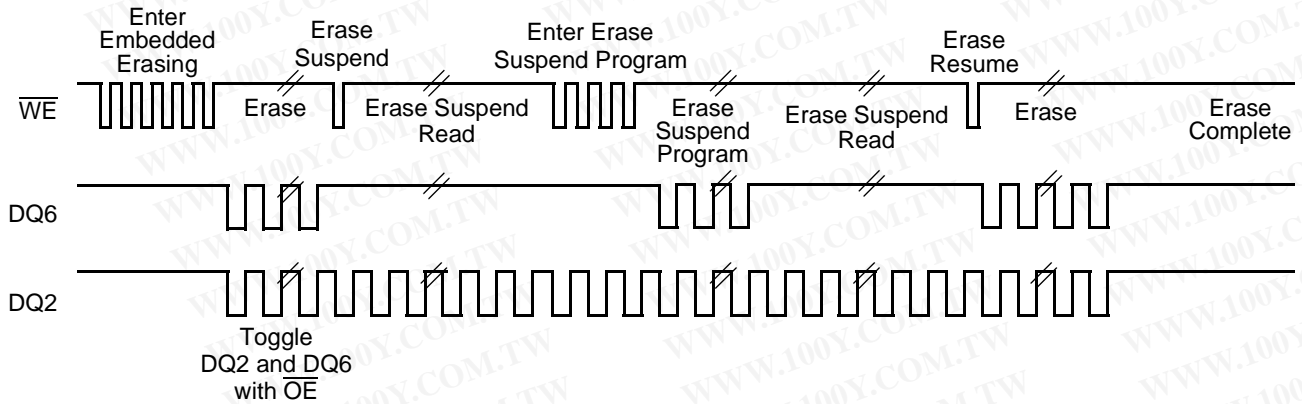


Figure 16. Temporary Sector Group Unprotect Timing Diagram



**Note:**  
DQ2 is read from the erase-suspended sector.

Figure 17. DQ2 vs. DQ6

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## AC CHARACTERISTICS

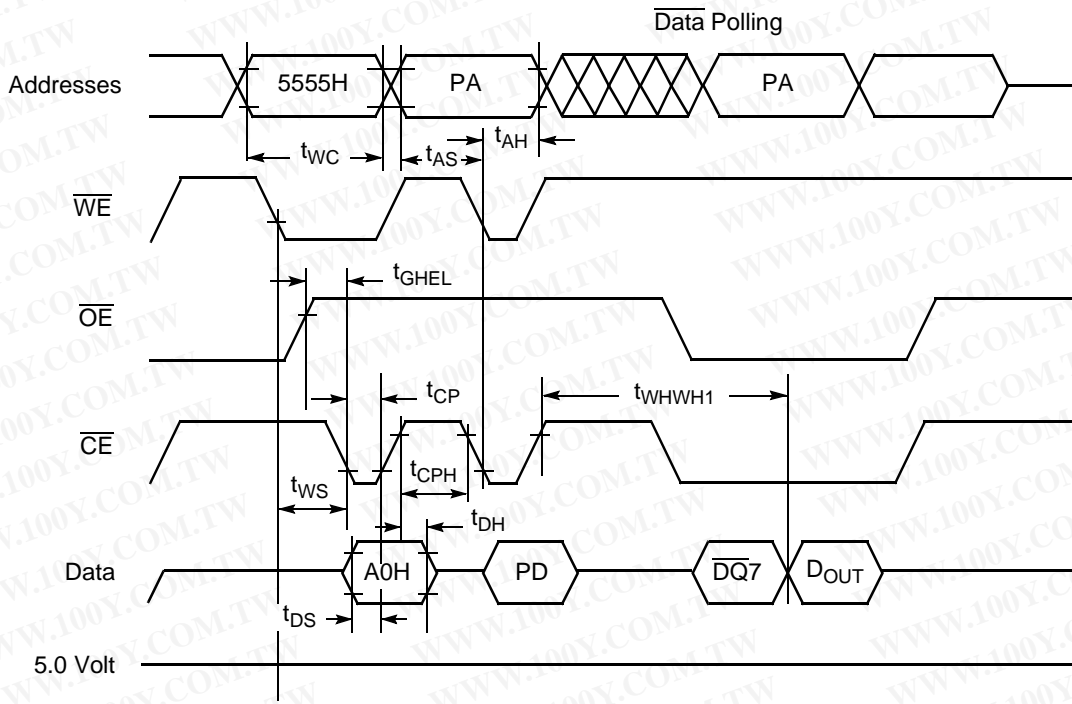
### Write/Erase/Program Operations

#### Alternate $\overline{CE}$ Controlled Writes

| Parameter Symbol |             | Parameter Description                                   |     | Speed Options (Notes 1 and 2) |     |      |      | Unit    |
|------------------|-------------|---|-----|-------------------------------|-----|------|------|---------|
| JEDEC            | Standard    |   |     | -75                           | -90 | -120 | -150 |         |
| $t_{AVAV}$       | $t_{WC}$    | Write Cycle Time  | Min | 70                            | 90  | 120  | 150  | ns      |
| $t_{AVEL}$       | $t_{AS}$    | Address Setup Time                                      | Min | 0                             | 0   | 0    | 0    | ns      |
| $t_{ELAX}$       | $t_{AH}$    | Address Hold Time                                       | Min | 40                            | 45  | 50   | 50   | ns      |
| $t_{DVEH}$       | $t_{DS}$    | Data Setup Time   | Min | 40                            | 45  | 50   | 50   | ns      |
| $t_{EHDX}$       | $t_{DH}$    | Address Hold Time                                       | Min | 0                             | 0   | 0    | 0    | ns      |
|                  | $t_{OES}$   | Output Enable Setup Time (Note 2)                       | Min | 0                             | 0   | 0    | 0    | ns      |
|                  | $t_{OEH}$   | Output Enable Hold Time                                 | Min | 0                             | 0   | 0    | 0    | ns      |
|                  |             | Read (Note 2)<br>Toggle Bit I and Data Polling (Note 2) | Min | 10                            | 10  | 10   | 10   | ns      |
| $t_{GHEL}$       | $t_{GHEL}$  | Read Recover Time Before Write                          | Min | 0                             | 0   | 0    | 0    | ns      |
| $t_{WLEL}$       | $t_{WS}$    | $\overline{CE}$ Setup Time                              | Min | 0                             | 0   | 0    | 0    | ns      |
| $t_{EHWL}$       | $t_{WH}$    | $\overline{CE}$ Hold Time                               | Min | 0                             | 0   | 0    | 0    | ns      |
| $t_{ELEH}$       | $t_{CP}$    | Write Pulse Width                                       | Min | 40                            | 45  | 50   | 50   | ns      |
| $t_{EHEL}$       | $t_{CPH}$   | Write Pulse Width High                                  | Min | 20                            | 20  | 20   | 20   | ns      |
| $t_{WHWH1}$      | $t_{WHWH1}$ | Byte Programming Operation                              | Typ | 7                             | 7   | 7    | 7    | $\mu$ s |
| $t_{WHWH2}$      | $t_{WHWH2}$ | Sector Erase Operation (Note 1)                         | Typ | 1                             | 1   | 1    | 1    | sec     |
|                  |             |   | Max | 8                             | 8   | 8    | 8    | sec     |

**Notes:**

1. This does not include the preprogramming time.
2. Not 100% tested.



**Notes:**

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3.  $\overline{DQ7}$  is the output of the complement of the data written to the device.
4.  $D_{OUT}$  is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

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**Figure 18. Alternate  $\overline{CE}$  Controlled Program Operation Timing**

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## ERASE AND PROGRAMMING PERFORMANCE

| Parameter             | Limits |               |                   | Unit | Comments                                  |
|-----------------------|--------|---------------|-------------------|------|---|
|                       | Min    | Typ           | Max               |      |   |
| Sector Erase Time     |        | 1 (Note 1)    | 8                 | sec  | Excludes 00H programming prior to erasure |
| Chip Erase Time       |        | 32            | 256               | sec  | Excludes 00H programming prior to erasure |
| Byte Programming Time |        | 7             | 300 (Note 3)      | μs   | Excludes system-level overhead            |
| Chip Programming Time |        | 14.4 (Note 1) | 43.2 (Notes 2, 3) | sec  | Excludes system-level overhead            |

**Notes:**

1. 25°C, 5 V  $V_{CC}$ , 100,000 cycles.
2. Although Embedded Algorithms allow for a longer chip program and erase time, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.
3. Under worst case condition of 90°C, 4.5 V  $V_{CC}$ , 100,000 cycles.

## LATCHUP CHARACTERISTIC

|  | Min     | Max              |
|--|---------|------------------|
| Input Voltage with respect to $V_{SS}$ on I/O pins | -1.0 V  | $V_{CC} + 1.0$ V |
| $V_{CC}$ Current                                   | -100 mA | +100 mA          |

Includes all pins except  $V_{CC}$ . Test conditions:  $V_{CC} = 5.0$  Volt, one pin at a time.

## TSOP PIN CAPACITANCE

| Parameter Symbol | Parameter Description   | Test Conditions | Min | Max | Unit |
|------------------|-------------------------|-----------------|-----|-----|------|
| $C_{IN}$         | Input Capacitance       | $V_{IN} = 0$    | 6   | 7.5 | pF   |
| $C_{OUT}$        | Output Capacitance      | $V_{OUT} = 0$   | 8.5 | 12  | pF   |
| $C_{IN2}$        | Control Pin Capacitance | $V_{IN} = 0$    | 7.5 | 9   | pF   |

**Notes:**

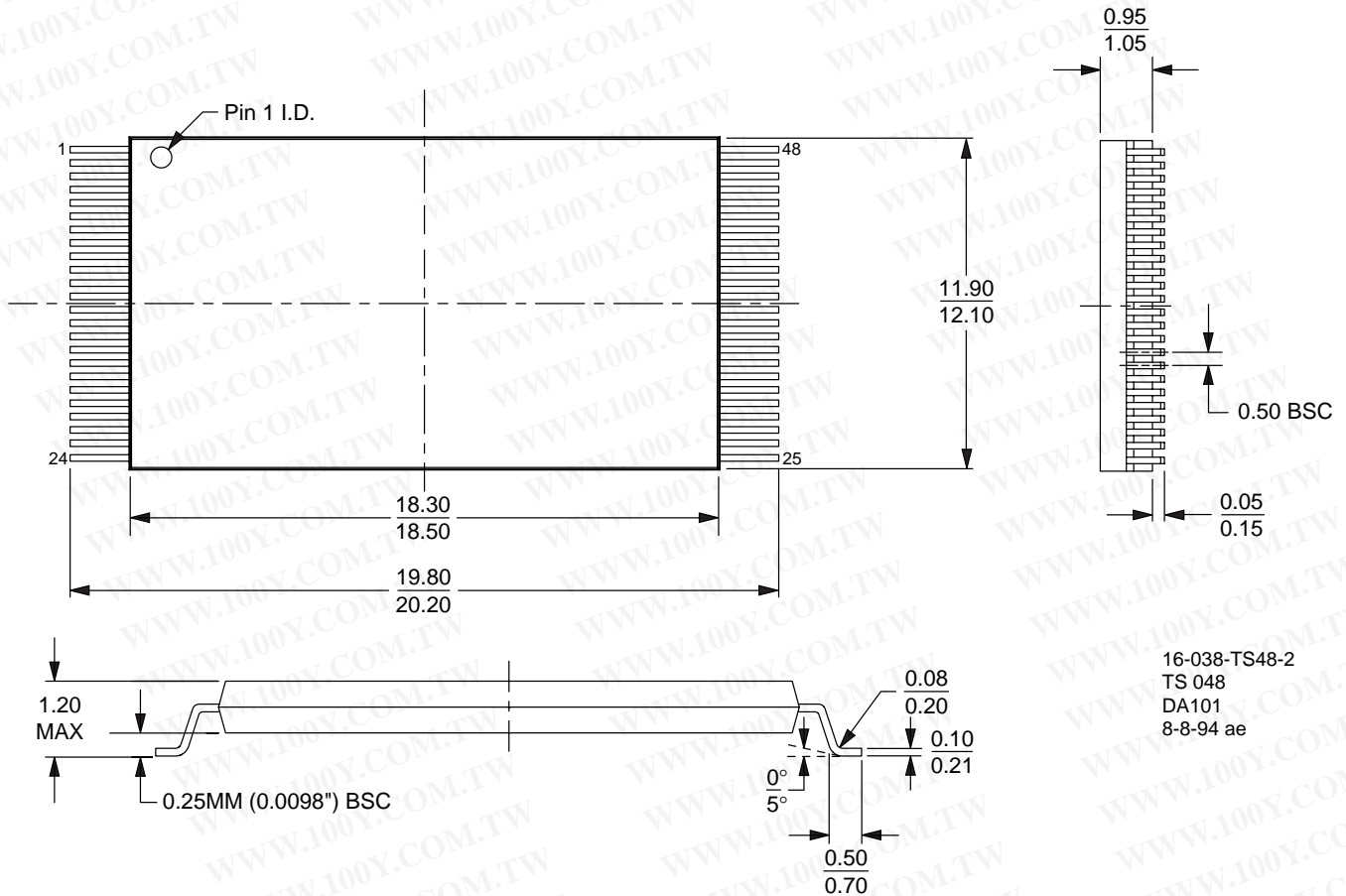
1. Sampled, not 100% tested.
2. Test conditions  $T_A = 25^\circ\text{C}$ ,  $f = 1.0$  MHz.

勝特力材料 886-3-5753170  
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 勝特力电子(深圳) 86-755-83298787  
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**PHYSICAL DIMENSIONS**

**TS 048**

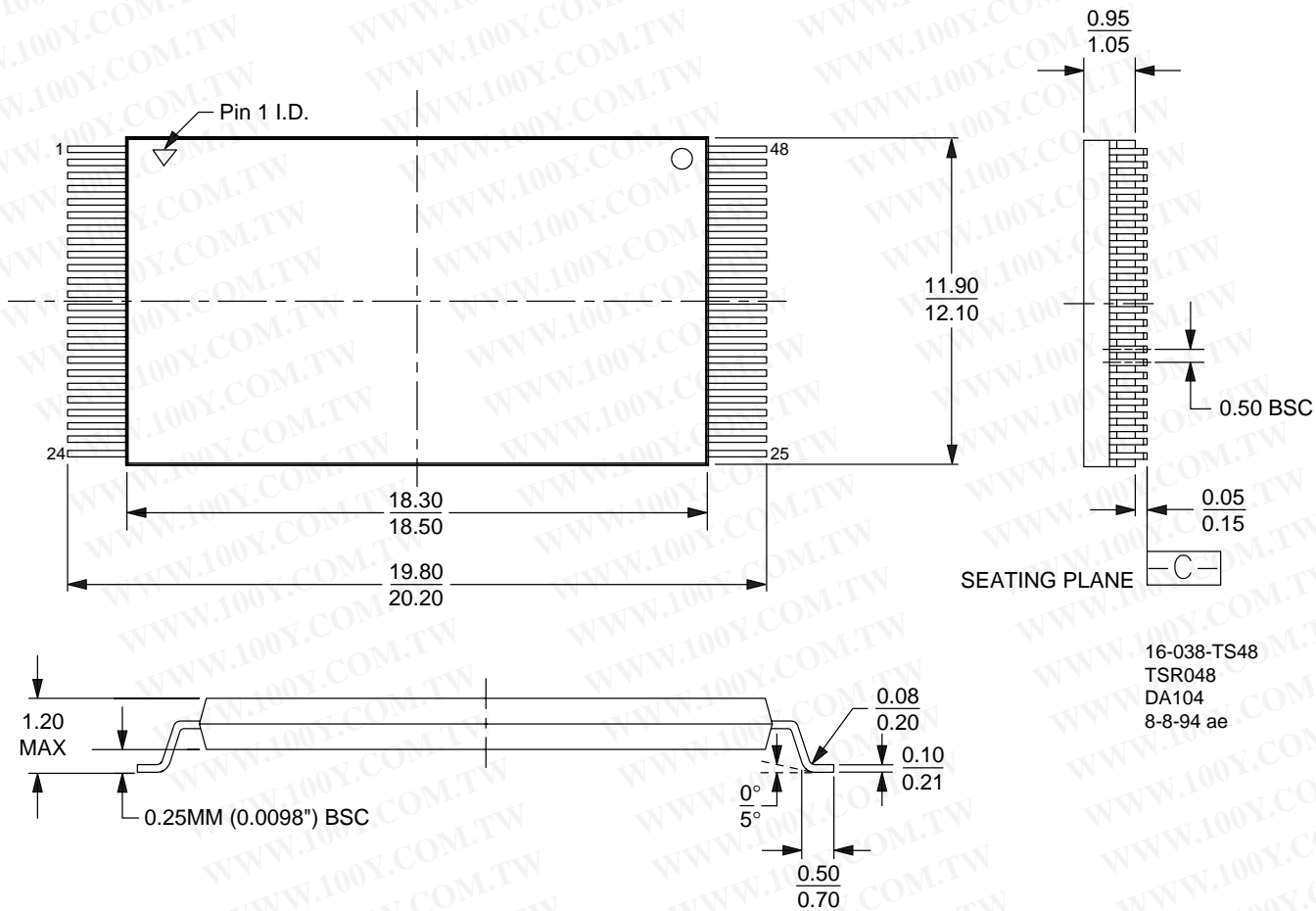
**48-Pin Standard Thin Small Outline Package**



PHYSICAL DIMENSIONS

TSR048

48-Pin Reversed Thin Small Outline Package



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