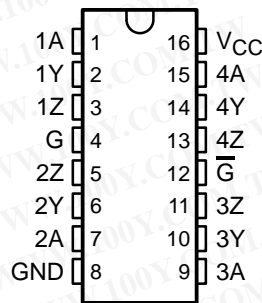


- Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B and ITU Recommendation V.11
- Operates From a Single 5-V Supply
- TTL Compatible
- Complementary Outputs
- High Output Impedance in Power-Off Conditions
- Complementary Output-Enable Inputs

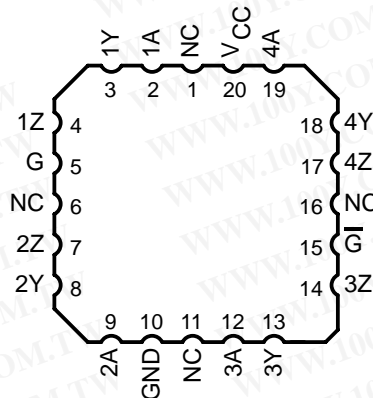
**description/ordering information**

The AM26LS31 is a quadruple complementary-output line driver designed to meet the requirements of ANSI TIA/EIA-422-B and ITU (formerly CCITT) Recommendation V.11. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they are in the high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable (G,  $\bar{G}$ ) input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

**D, DB, N, NS, OR J PACKAGE  
 (TOP VIEW)**



**FK PACKAGE  
 (TOP VIEW)**



**ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	AM26LS31CN	AM26LS31CN
	SOIC – D	Tube	AM26LS31CD	AM26LS31C
		Tape and reel	AM26LS31CDR	
	SOP – NS	Tape and reel	AM26LS31CNSR	26LS31
SSOP – DB	Tape and reel	AM26LS31CDBR	SA31C	
–55°C to 125°C	CDIP – J	Tube	AM26LS31MJ	AM26LS31MJB
	LCCC – FK	Tube	AM26LS31MFK	AM26LS31MFKB

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



# AM26LS31C, AM26LS31M QUADRUPLE DIFFERENTIAL LINE DRIVER

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 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

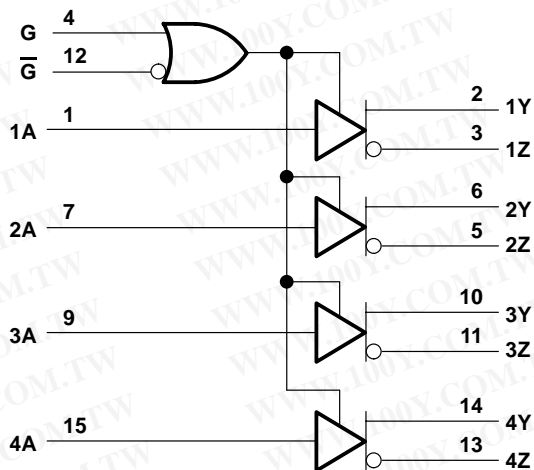
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FUNCTION TABLE  
(each driver)

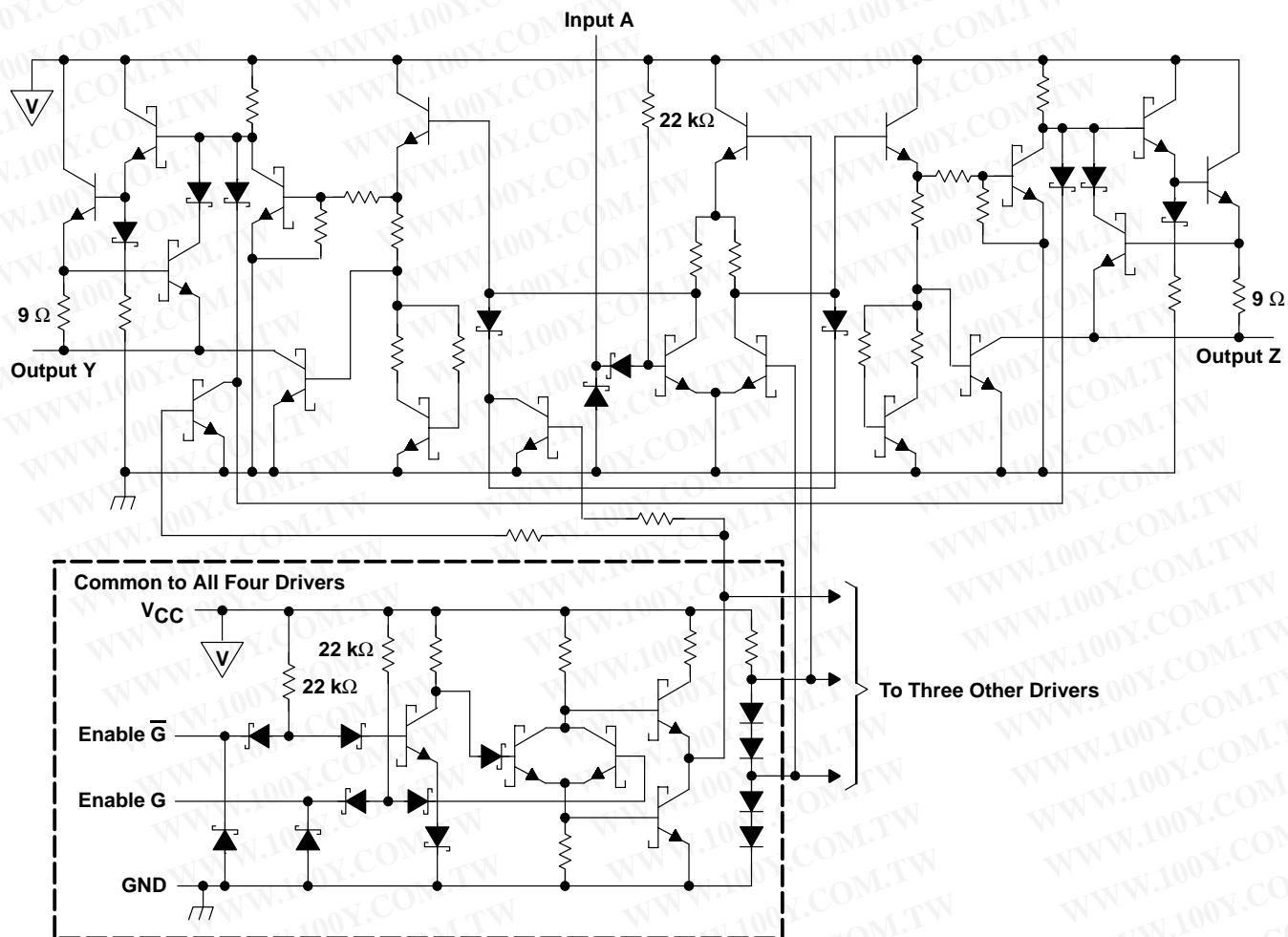
INPUT A	ENABLES		OUTPUTS	
	G	$\bar{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,  
 Z = high impedance (off)

## logic diagram (positive logic)



**schematic (each driver)**



All resistor values are nominal.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$	7 V
Output off-state voltage	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	73°C/W
DB package	82°C/W
N package	67°C/W
NS package	64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential output voltage  $V_{OD}$ , are with respect to network GND.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ ‡	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ( $R\theta_{JA}$ ). Thermal resistances are not production tested and the values given are for informational purposes only.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	AM26LS31C	4.75	5	5.25	V
	AM26LS31M	4.5	5	5.5	
$V_{IH}$ High-level input voltage		2			V
$V_{IL}$ Low-level input voltage					0.8 V
$I_{OH}$ High-level output current					-20 mA
$I_{OL}$ Low-level output current					20 mA
$T_A$ Operating free-air temperature	AM26LS31C	0		70	°C
	AM26LS31M	-55		125	



electrical characteristics over operating free-air temperature range (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -20 mA	T <sub>A</sub> = -55°C		2.4	V
		All other temperatures		2.5	
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 20 mA			0.5	V
I <sub>OZ</sub> Off-state (high-impedance-state) output current	V <sub>CC</sub> = MIN	V <sub>O</sub> = 0.5 V		-20	μA
		V <sub>O</sub> = 2.5 V		20	
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1	mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20	μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.36	mA
I <sub>OS</sub> Short-circuit output current§	V <sub>CC</sub> = MAX	-30		-150	mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, All outputs disabled		32	80	mA

† For C suffix devices, V<sub>CC</sub> MIN = 4.75 V and V<sub>CC</sub> MAX = 5.25 V. For M suffix devices, V<sub>CC</sub> MIN = 4.5 V and V<sub>CC</sub> MAX = 5.5 V.

‡ All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)

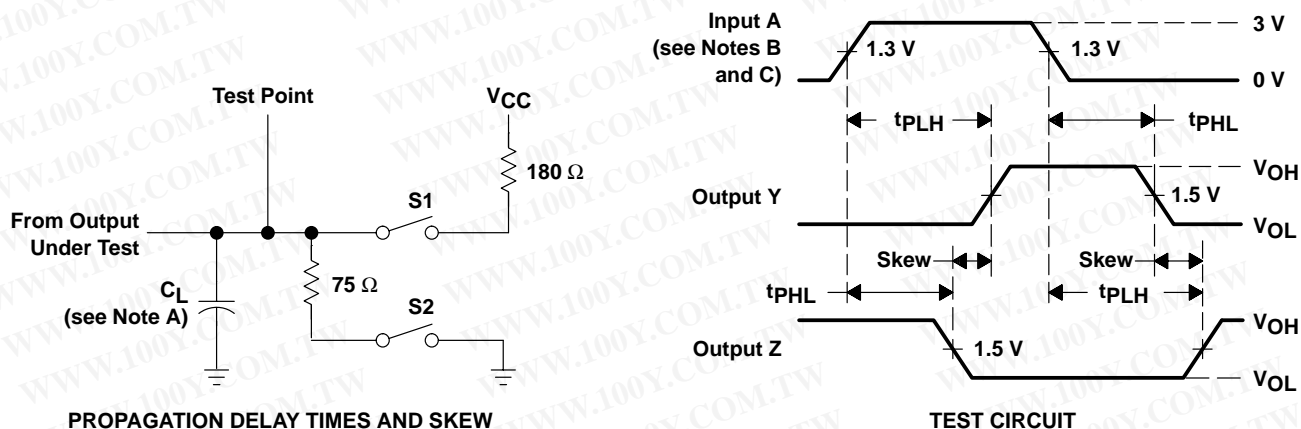
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	C <sub>L</sub> = 30 pF, S1 and S2 open		14	20	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output			14	20	
t <sub>PZH</sub> Output enable time to high level	C <sub>L</sub> = 30 pF	R <sub>L</sub> = 75 Ω		25	ns
t <sub>PZL</sub> Output enable time to low level		R <sub>L</sub> = 180 Ω		37	
t <sub>PHZ</sub> Output disable time from high level	C <sub>L</sub> = 10 pF, S1 and S2 closed		21	30	ns
t <sub>PLZ</sub> Output disable time from low level			23	35	
Output-to-output skew	C <sub>L</sub> = 30 pF, S1 and S2 open		1	6	ns

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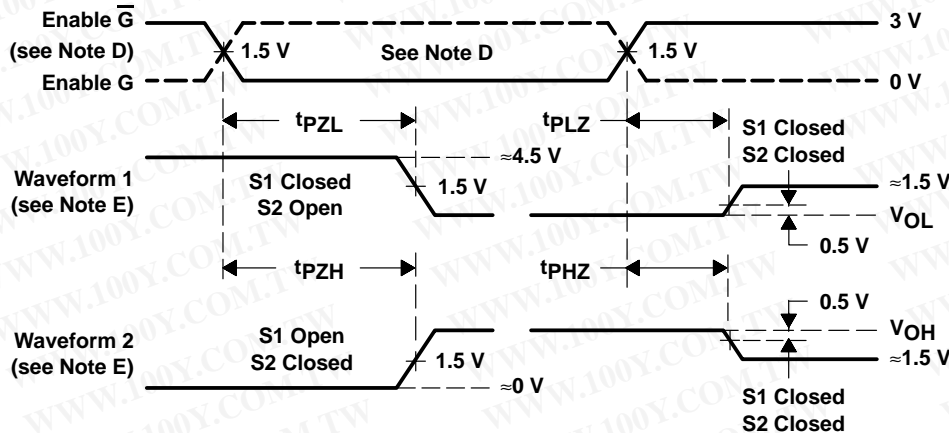
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## PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES AND SKEW

TEST CIRCUIT



ENABLE AND DISABLE TIME WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 15$  ns,  $t_f \leq 6$  ns.  
 C. When measuring propagation delay times and skew, switches S1 and S2 are open.  
 D. Each enable is tested separately.  
 E. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

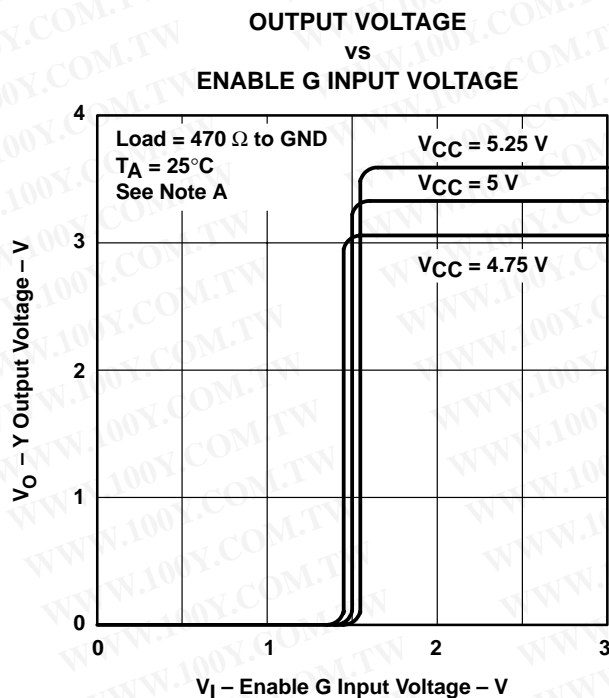


Figure 2

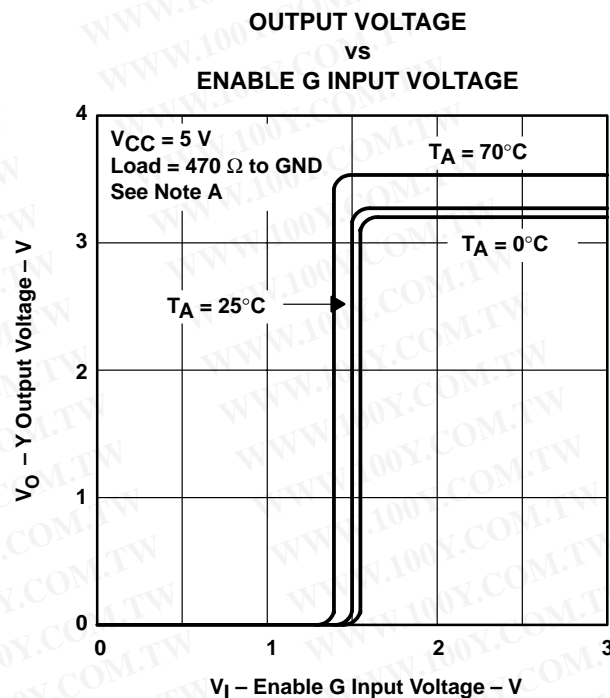


Figure 3

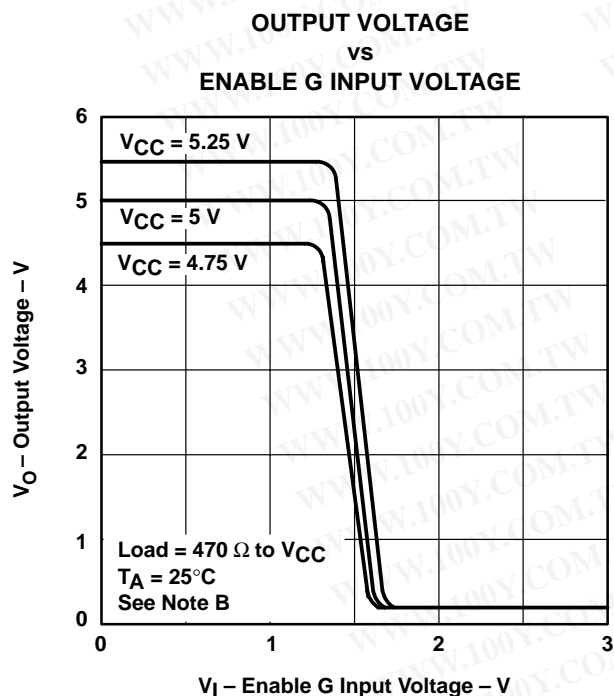


Figure 4

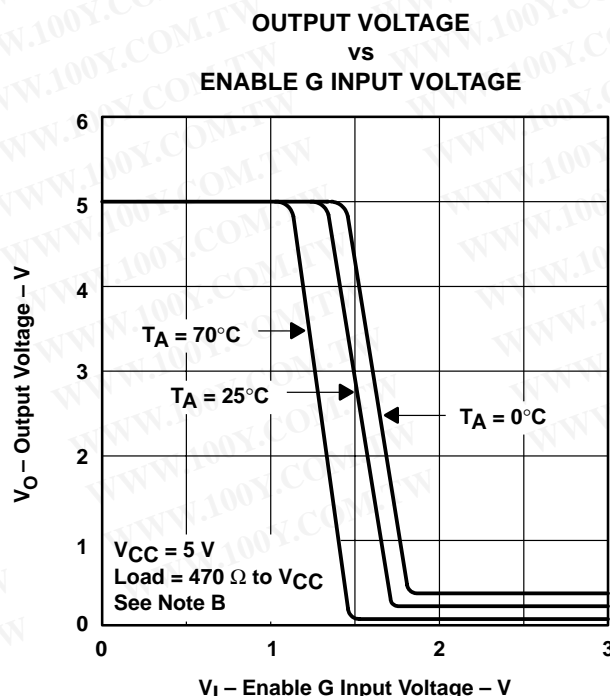


Figure 5

NOTES: A. The A input is connected to  $V_{CC}$  during testing of the Y outputs and to ground during testing of the Z outputs.  
B. The A input is connected to ground during testing of the Y outputs and to  $V_{CC}$  during testing of the Z outputs.

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## TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE  
vs  
FREE-AIR TEMPERATURE

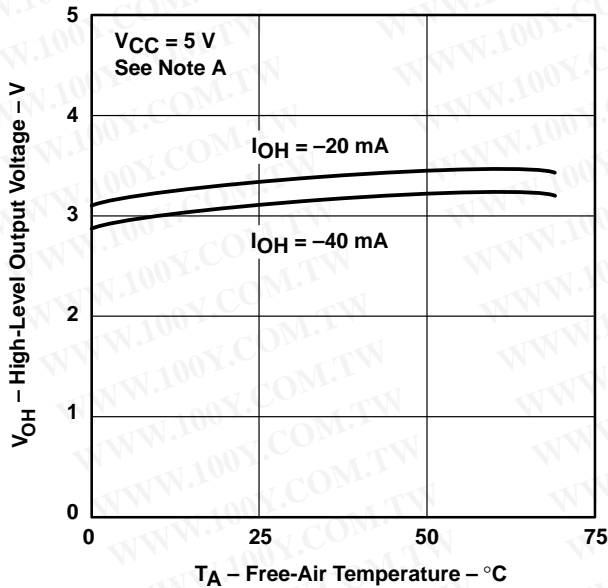


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE  
vs  
HIGH-LEVEL OUTPUT CURRENT

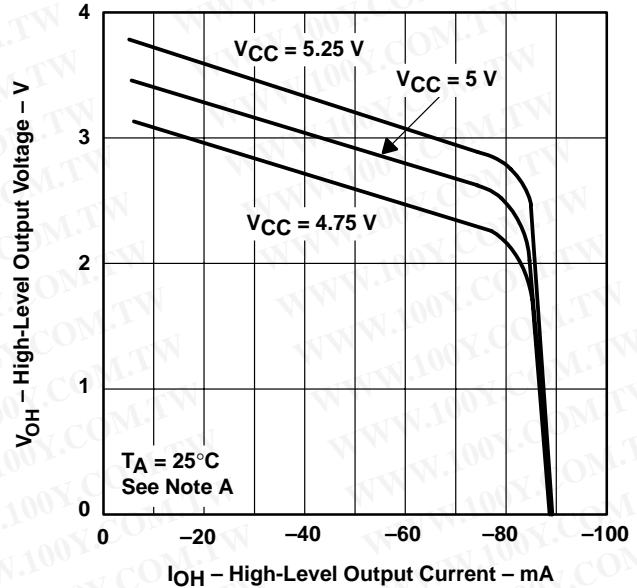


Figure 7

LOW-LEVEL OUTPUT VOLTAGE  
vs  
FREE-AIR TEMPERATURE

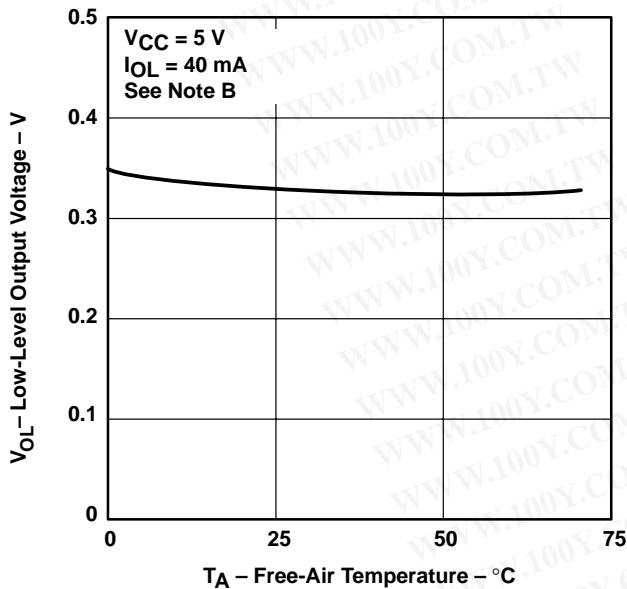


Figure 8

LOW-LEVEL OUTPUT VOLTAGE  
vs  
LOW-LEVEL OUTPUT CURRENT

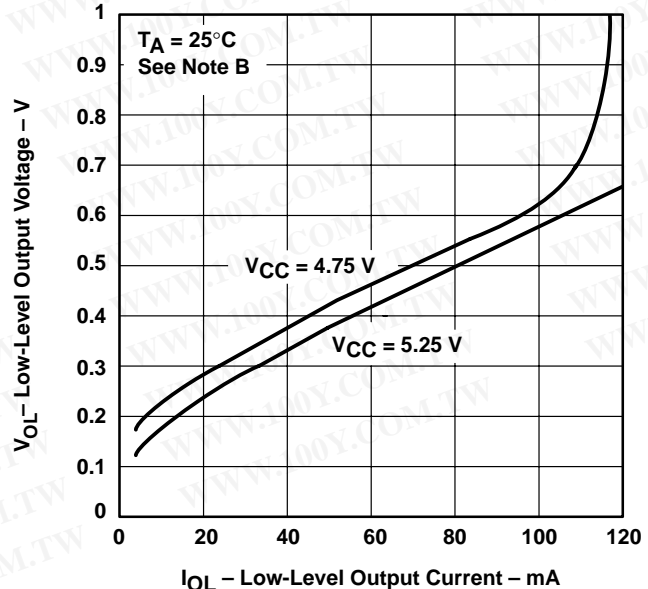
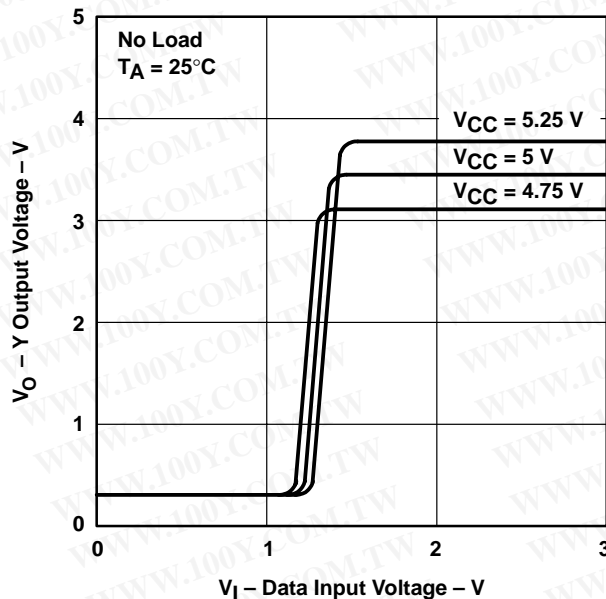


Figure 9

NOTES: A. The A input is connected to  $V_{CC}$  during testing of the Y outputs and to ground during testing of the Z outputs.  
 B. The A input is connected to ground during testing of the Y outputs and to  $V_{CC}$  during testing of the Z inputs.

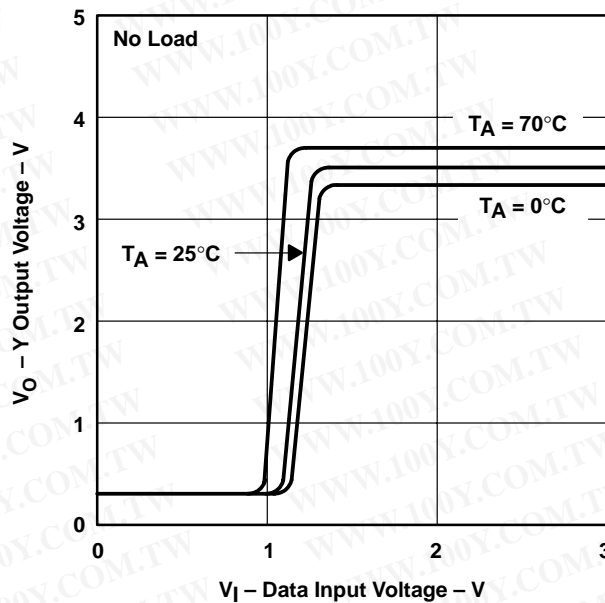
**TYPICAL CHARACTERISTICS**

**Y OUTPUT VOLTAGE**  
**vs**  
**DATA INPUT VOLTAGE**



**Figure 10**

**Y OUTPUT VOLTAGE**  
**vs**  
**DATA INPUT VOLTAGE**



**Figure 11**

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