



CMOS

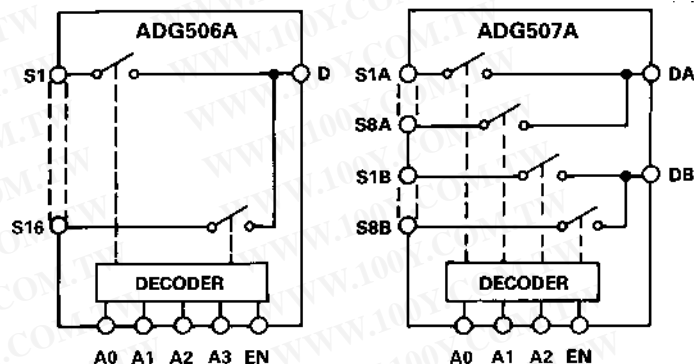
# 8-/16-Channel Analog Multiplexers

## ADG506A/ADG507A

### FEATURES

- 44 V Supply Maximum Rating
- $V_{SS}$  to  $V_{DD}$  Analog Signal Range
- Single/Dual Supply Specifications
- Wide Supply Ranges (10.8 V to 16.5 V)
- Extended Plastic Temperature Range  
( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- Low Power Dissipation (28 mW max)
- Low Leakage (20 pA typ)
- Available in 28-Lead DIP, SOIC, PLCC, TSSOP and LCCC Packages
- Superior Alternative to:  
 DG506A, HI-506  
 DG507A, HI-507

### FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The ADG506A and ADG507A are CMOS monolithic analog multiplexers with 16 channels and dual 8 channels, respectively. The ADG506A switches one of 16 inputs to a common output, depending on the state of four binary addresses and an enable input. The ADG507A switches one of eight differential inputs to a common differential output, depending on the state of three binary addresses and an enable input. Both devices have TTL and 5 V CMOS logic compatible digital inputs.

The ADG506A and ADG507A are designed on an enhanced  $\text{LC}^2\text{MOS}$  process, which gives an increased signal capability of  $V_{SS}$  to  $V_{DD}$  and enables operation over a wide range of supply voltages. The devices can operate comfortably anywhere in the 10.8 V to 16.5 V single or dual supply range. These multiplexers also feature high switching speeds and low  $R_{ON}$ .

### PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance  
 The devices are specified in the 10.8 V to 16.5 V range for both single and dual supplies.
2. Extended Signal Range  
 The enhanced  $\text{LC}^2\text{MOS}$  processing results in a high breakdown and an increased analog signal range of  $V_{SS}$  to  $V_{DD}$ .
3. Break-Before-Make Switching  
 Switches are guaranteed break-before-make so input signals are protected against momentary shorting.
4. Low Leakage  
 Leakage currents in the range of 20 pA make these multiplexers suitable for high precision circuits.

### ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Option <sup>2</sup>
ADG506AKN	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	N-28
ADG506AKR	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	R-28
ADG506AKP	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	P-28A
ADG506ABQ	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Q-28
ADG506ATQ	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Q-28
ADG506ATE	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	E-28A
ADG507AKN	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	N-28
ADG507AKR	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	R-28
ADG507AKP	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	P-28A
ADG507AKRU	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	RU-28
ADG507ABQ	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Q-28
ADG507ATQ	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Q-28
ADG507ATE	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	E-28A

### NOTES

<sup>1</sup>To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices' *Military/Aerospace Reference Manual* (1994) for military data sheet.

<sup>2</sup>E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = 0.3" Small Outline IC (SOIC); RU = Thin Shrink Small Outline Package (TSSOP).

### REV. C

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# ADG506A/ADG507A—SPECIFICATIONS

Dual Supply ( $V_{DD} = +10.8\text{ V to }+16.5\text{ V}$ ,  $V_{SS} = -10.8\text{ V to }-16.5\text{ V}$  unless otherwise noted)

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

Parameter	ADG506A ADG507A K Version		ADG506A ADG507A B Version		ADG506A ADG507A T Version		Units	Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>								
ANALOG Signal Range	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	V min	
	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	V max	
$R_{ON}$	280		280		280		$\Omega$ typ	$-10\text{ V} \leq V_S \leq +10\text{ V}$ , $I_{DS} = 1\text{ mA}$ ; Test Circuit 1
	450	600	450	600	450	600	$\Omega$ max	
	300	400	300	400			$\Omega$ max	$V_{DD} = 15\text{ V} (\pm 10\%)$ , $V_{SS} = -15\text{ V} (\pm 10\%)$
$R_{ON}$ Drift	0.6		0.6		0.6		$\%/^{\circ}\text{C}$ typ	$V_{DD} = 15\text{ V} (\pm 5\%)$ , $V_{SS} = -15\text{ V} (\pm 5\%)$
$R_{ON}$ Match	5		5		5		% typ	$-10\text{ V} \leq V_S \leq +10\text{ V}$ , $I_{DS} = 1\text{ mA}$
								$-10\text{ V} \leq V_S \leq +10\text{ V}$ , $I_{DS} = 1\text{ mA}$
$I_S$ (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	$V_1 = \pm 10\text{ V}$ , $V_2 = \mp 10\text{ V}$ ; Test Circuit 2
	1	50	1	50	1	50	nA max	
$I_D$ (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	$V_1 = \pm 10\text{ V}$ , $V_2 = \mp 10\text{ V}$ ; Test Circuit 3
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
$I_D$ (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	$V_1 = \pm 10\text{ V}$ , $V_2 = \mp 10\text{ V}$ ; Test Circuit 4
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
$I_{DIFF}$ , Differential Off Output Leakage (ADG507A Only)		25		25		25	nA max	$V_1 = \pm 10\text{ V}$ , $V_2 = \mp 10\text{ V}$ ; Test Circuit 5
<b>DIGITAL CONTROL</b>								
$V_{INH}$ , Input High Voltage		2.4		2.4		2.4	V min	
$V_{INL}$ , Input Low Voltage		0.8		0.8		0.8	V max	
$I_{INL}$ or $I_{INH}$		1		1		1	$\mu\text{A}$ max	$V_{IN} = 0$ to $V_{DD}$
$C_{IN}$ Digital Input Capacitance	8		8		8		pF max	
<b>DYNAMIC CHARACTERISTICS</b>								
$t_{TRANSITION}^1$	200		200		200		ns typ	$V_1 = \pm 10\text{ V}$ , $V_2 = +10\text{ V}$ ; Test Circuit 6
	300	400	300	400	300	400	ns max	
$t_{OPEN}^1$	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
$t_{ON}$ (EN) <sup>1</sup>	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
$t_{OFF}$ (EN) <sup>1</sup>	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	$V_{EN} = 0.8\text{ V}$ , $R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $V_S = 7\text{ V rms}$ , $f = 100\text{ kHz}$
	50		50		50		dB min	
$C_S$ (OFF)	5		5		5		pF typ	$V_{EN} = 0.8\text{ V}$
$C_D$ (OFF)							pF typ	$V_{EN} = 0.8\text{ V}$
ADG506A	44		44		44		pF typ	
ADG507A	22		22		22		pF typ	
$Q_{INJ}$ , Charge Injection	4		4		4		pC typ	$R_S = 0\text{ }\Omega$ , $V_S = 0\text{ V}$ ; Test Circuit 9
<b>POWER SUPPLY</b>								
$I_{DD}$	0.6		0.6		0.6		mA typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		1.5		1.5		1.5	mA max	
$I_{SS}$	20		20		20		$\mu\text{A}$ typ	$V_{IN} = V_{IN}$ or $V_{INH}$
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

## NOTES

<sup>1</sup>Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

Single Supply ( $V_{DD} = +10.8\text{ V to }+16.5\text{ V}$ ,  $V_{SS} = \text{GND} = 0\text{ V}$  unless otherwise noted)

Parameter	ADG506A ADG507A K Version		ADG506A ADG507A B Version		ADG506A ADG507A T Version		Units	Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
ANALOG SWITCH								
Analog Signal Range	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	V min V max	
$R_{ON}$	500	1000	500	1000	500	1000	$\Omega$ typ	$0\text{ V} \leq V_S \leq +10\text{ V}$ , $I_{DS} = 0.5\text{ mA}$ ; Test Circuit 1
$R_{ON}$ Drift	0.6		0.6		0.6		$\%/^{\circ}\text{C}$ typ	$0\text{ V} \leq V_S \leq +10\text{ V}$ , $I_{DS} = 0.5\text{ mA}$
$R_{ON}$ Match	5		5		5		% typ	$0\text{ V} \leq V_S \leq +10\text{ V}$ , $I_{DS} = 0.5\text{ mA}$
$I_S$ (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	$V_1 = +10\text{ V}/0\text{ V}$ , $V_2 = 0\text{ V}/+10\text{ V}$ ; Test Circuit 2
$I_D$ (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	$V_1 = +10\text{ V}/0\text{ V}$ , $V_2 = 0\text{ V}/+10\text{ V}$ ; Test Circuit 3
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
$I_D$ (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	$V_1 = +10\text{ V}/0\text{ V}$ , $V_2 = 0\text{ V}/+10\text{ V}$ ; Test Circuit 4
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
$I_{DIFF}$ , Differential Off Output Leakage (ADG507A Only)		25		25		25	nA max	$V_1 = +10\text{ V}/0\text{ V}$ , $V_2 = 0\text{ V}/+10\text{ V}$ ; Test Circuit 5
DIGITAL CONTROL								
$V_{INH}$ , Input High Voltage		2.4		2.4		2.4	V min	
$V_{INL}$ , Input Low Voltage		0.8		0.8		0.8	V max	
$I_{INL}$ or $I_{INH}$		1		1		1	$\mu\text{A}$ max	$V_{IN} = 0$ to $V_{DD}$
$C_{IN}$ Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}^1$	300		300		300		ns typ	$V_1 = +10\text{ V}/0\text{ V}$ , $V_2 = +10\text{ V}$ ; Test Circuit 6
	450	600	450	600	450	600	ns max	
$t_{OPEN}^1$	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
$t_{ON}$ (EN) <sup>1</sup>	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
$t_{OFF}$ (EN) <sup>1</sup>	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
OFF Isolation	68		68		68		dB typ	$V_{EN} = 0.8\text{ V}$ , $R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $V_S = 3.5\text{ V rms}$ , $f = 100\text{ kHz}$
	50		50		50		dB min	
$C_S$ (OFF)	5		5		5		pF typ	$V_{EN} = 0.8\text{ V}$
$C_D$ (OFF)								
ADG506A	44		44		44		pF typ	$V_{EN} = 0.8\text{ V}$
ADG507A	22		22		22		pF typ	
$Q_{INJ}$ , Charge Injection	4		4		4		pC typ	$R_S = 0\text{ }\Omega$ , $V_S = 0\text{ V}$ ; Test Circuit 9
POWER SUPPLY								
$I_{DD}$	0.6		0.6		0.6		mA typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		1.5		1.5		1.5	mA max	
Power Dissipation	10		10		10		mW typ	
		25		25		25	mW max	

NOTES

<sup>1</sup>Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

Truth Table (ADG506A)

A3	A2	A1	A0	EN	On Switch
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Truth Table (ADG507A)

A2	A1	A0	EN	On Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

# ADG506A/ADG507A

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> .....	44 V
V <sub>DD</sub> to GND .....	25 V
V <sub>SS</sub> to GND .....	-25 V
Analog Inputs <sup>2</sup>	
Voltage at S, D .....	V <sub>SS</sub> - 2 V to V <sub>DD</sub>
.....	+ 2 V or
.....	20 mA, Whichever Occurs First
Continuous Current, S or D .....	
Pulsed Current S or D .....	20 mA
1 ms Duration, 10% Duty Cycle .....	
Digital Inputs <sup>2</sup>	40 mA
Voltage at A, EN .....	
.....	V <sub>SS</sub> - 4 V
.....	to V <sub>DD</sub> + 4 V or
.....	20 mA, Whichever Occurs First

## Power Dissipation (Any Package)

Up to +75°C .....	470 mW
Derates above +75°C by .....	6 mW/°C

## Operating Temperature

Commercial (K Version) .....	-40°C to +85°C
Industrial (B Version) .....	-40°C to +85°C
Extended (T Version) .....	-55°C to +125°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10 secs) .....	+300°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

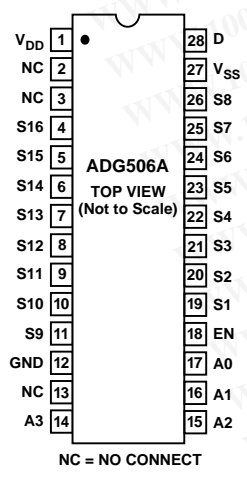
## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG506A/ADG507A feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

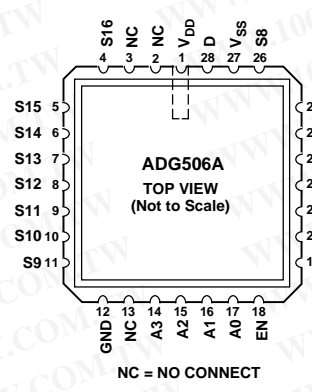


## PIN CONFIGURATIONS

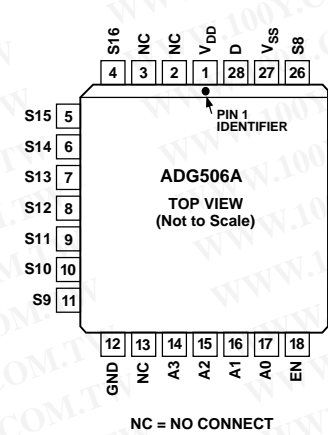
### DIP, SOIC



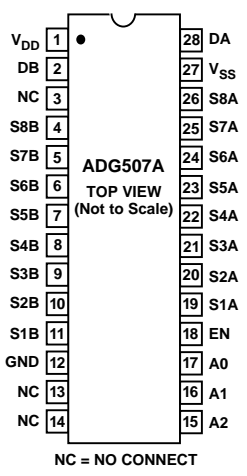
### LCCC



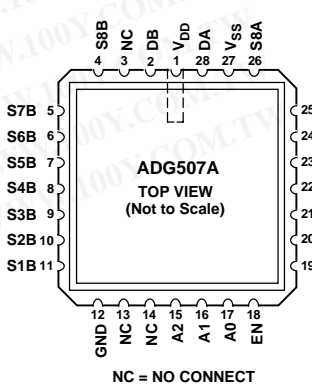
### PLCC



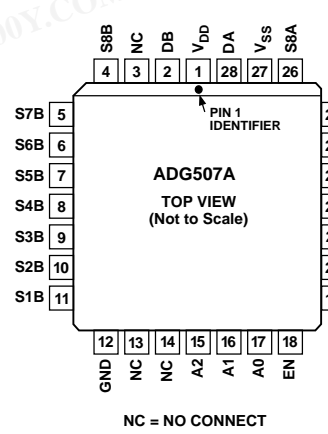
### DIP, SOIC, TSSOP



### LCCC



### PLCC



# Typical Performance Characteristics—ADG506A/ADG507A

The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5 V.

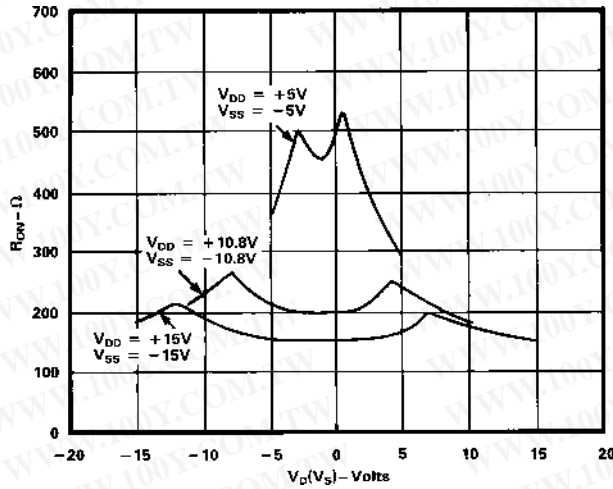


Figure 1.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Dual Supply Voltage,  $T_A = +25^\circ\text{C}$

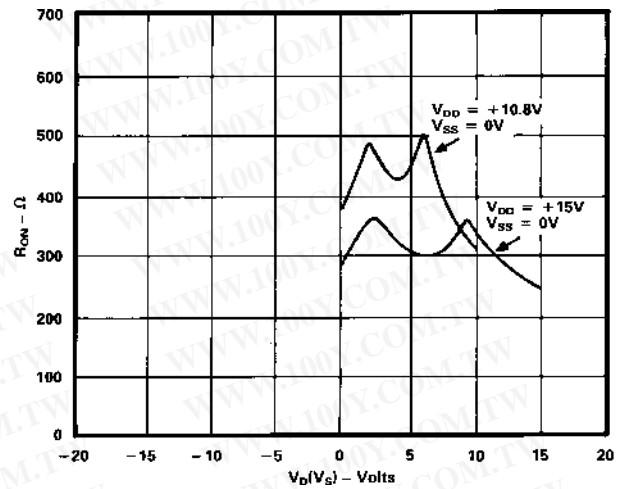


Figure 4.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) Single Supply Voltage,  $T_A = +25^\circ\text{C}$

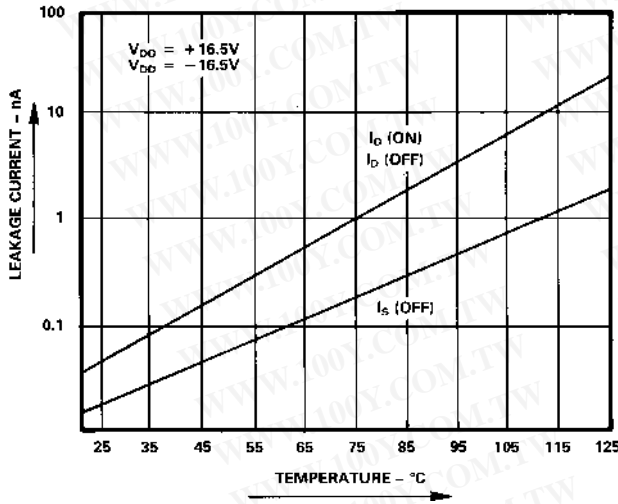


Figure 2. Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)

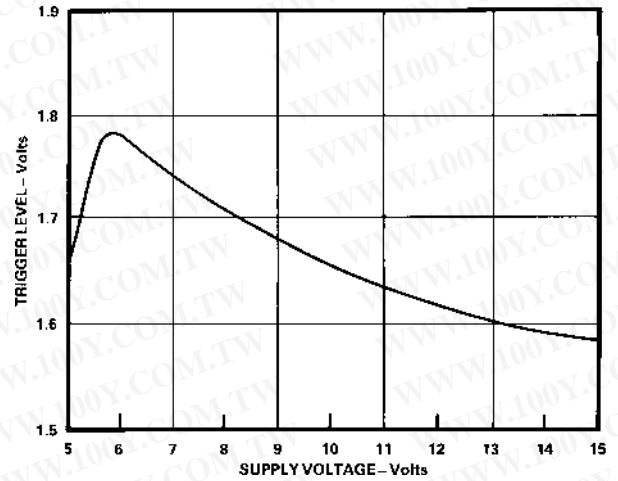


Figure 5. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply,  $T_A = +25^\circ\text{C}$

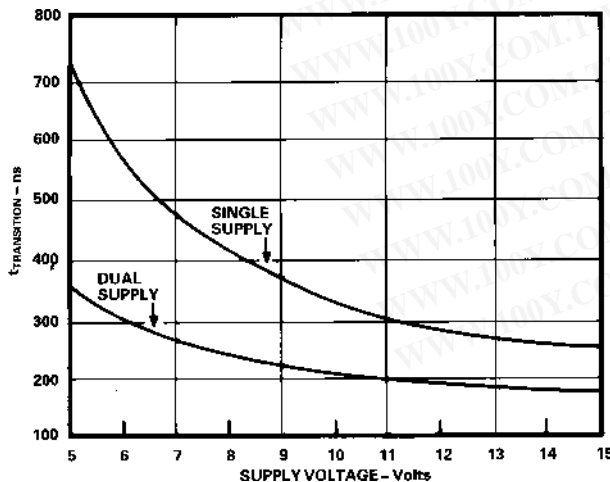


Figure 3.  $t_{TRANSITION}$  vs. Supply Voltage: Dual and Single Supplies,  $T_A = +25^\circ\text{C}$  (Note: For  $V_{DD}$  and  $|V_{SS}| < 10\text{V}$ ;  $V1 = V_{DD}/V_{SS}$ ,  $V2 = V_{SS}/V_{DD}$ . See Test Circuit 6)

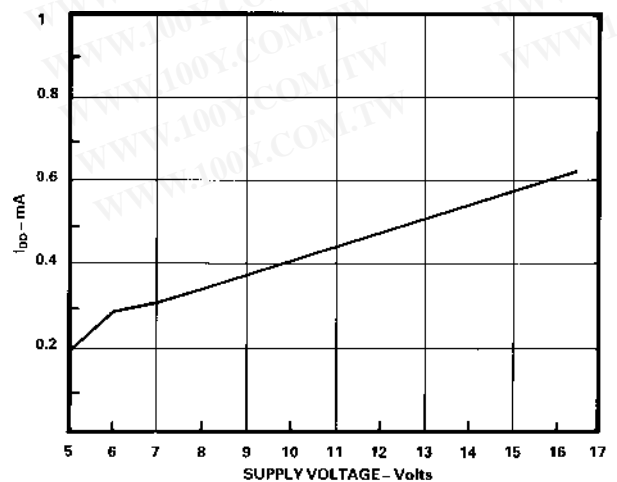
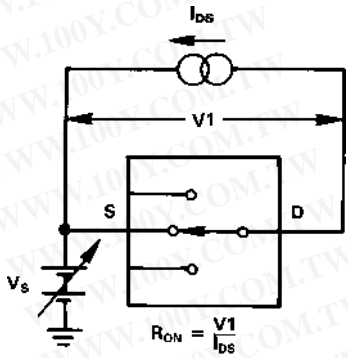


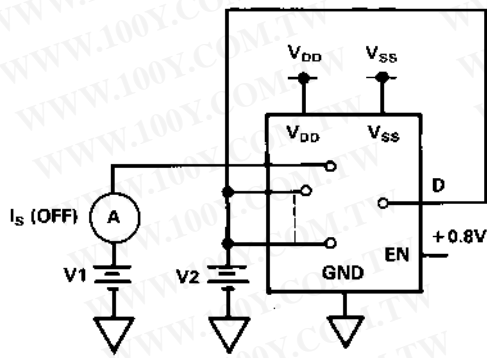
Figure 6.  $I_{DD}$  vs. Supply Voltage: Dual or Single Supply,  $T_A = +25^\circ\text{C}$

# ADG506A/ADG507A-Test Circuits

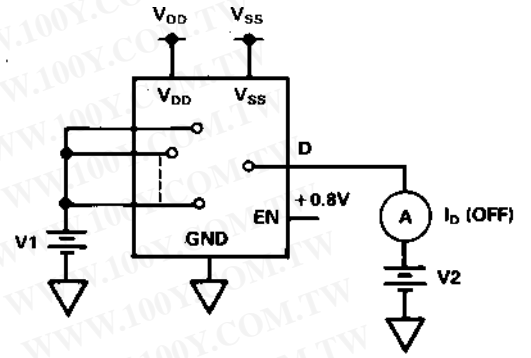
Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3 V.  $t_R = t_F = 20$  ns.



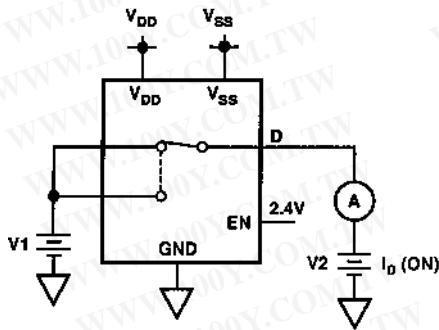
Test Circuit 1.  $R_{ON}$



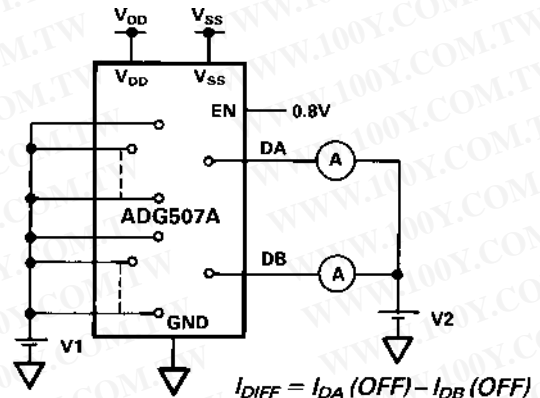
Test Circuit 2.  $I_s(OFF)$



Test Circuit 3.  $I_d(OFF)$

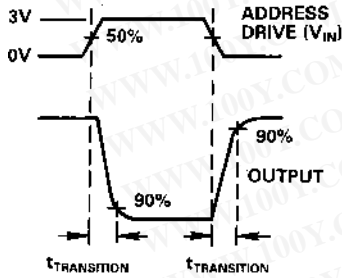


Test Circuit 4.  $I_d(ON)$



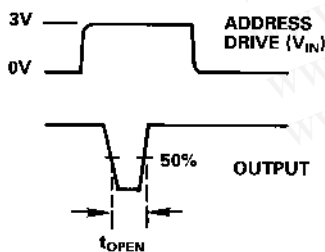
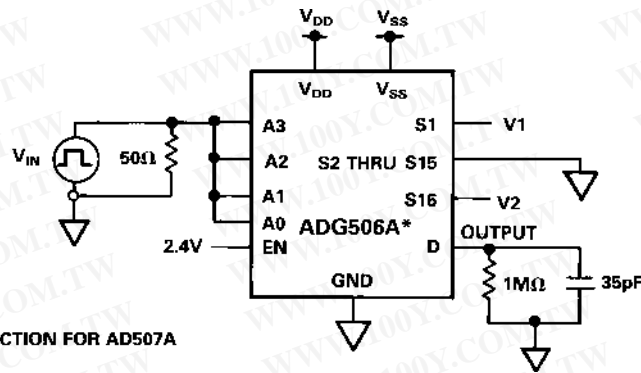
$$I_{DIFF} = I_{DA}(OFF) - I_{DB}(OFF)$$

Test Circuit 5.  $I_{DIFF}$



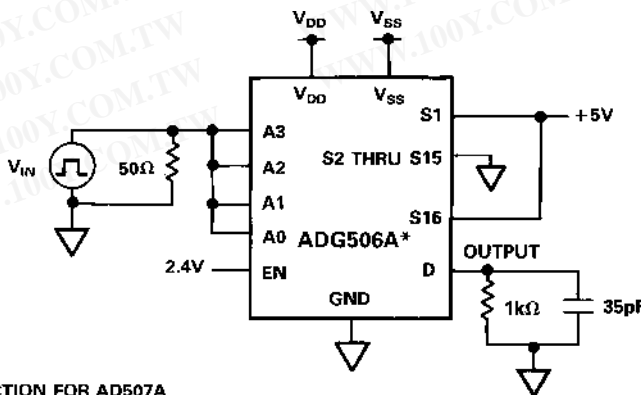
\*SIMILAR CONNECTION FOR AD507A

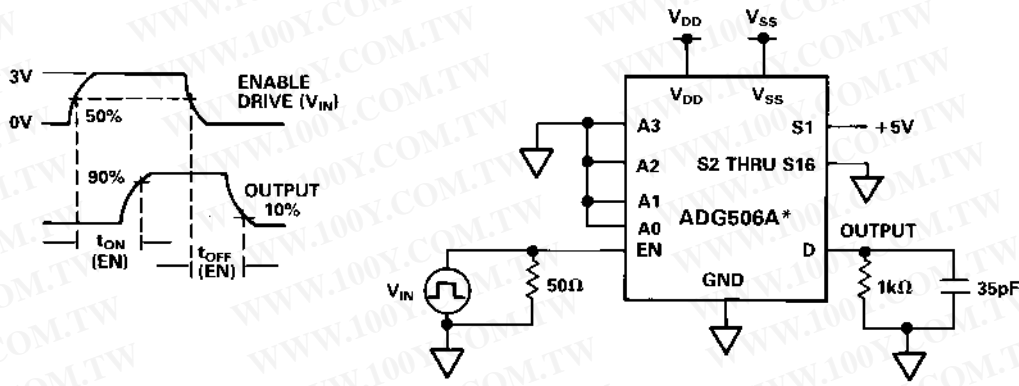
Test Circuit 6. Switching Time of Multiplexer,  $t_{TRANSITION}$



\*SIMILAR CONNECTION FOR AD507A

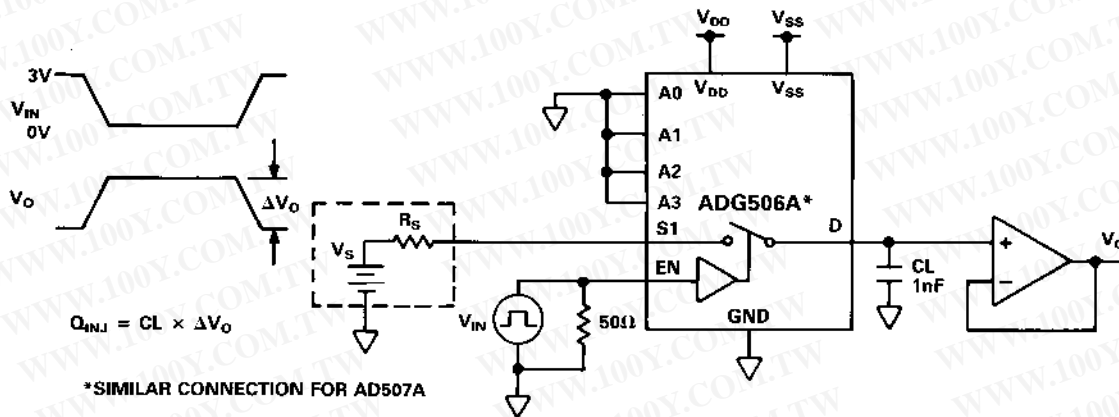
Test Circuit 7. Break-Before-Make Delay,  $t_{OPEN}$





\*SIMILAR CONNECTION FOR AD507A

Test Circuit 8. Enable Delay,  $t_{ON}$  (EN),  $t_{OFF}$  (EN)



$$Q_{INJ} = CL \times \Delta V_O$$

\*SIMILAR CONNECTION FOR AD507A

Test Circuit 9. Charge Injection

### SINGLE SUPPLY AUTOMOTIVE APPLICATION

The excellent performance of the multiplexers under single supply conditions makes the ADG506A/ADG507A suitable in applications such as automotive and disc drives where only positive power supply voltages are normally available. The following application circuit shows the ADG507A connected as an 8-channel differential multiplexer in an automotive, data acquisition application circuit.

The AD7580 is a 10-bit successive approximation ADC, which has an on-chip sample-and-hold amplifier and provides a conversion result in 20  $\mu$ s. The ADC has differential analog inputs and is configured in the application circuit for a span of 2.5 V over a common-mode range 0 V to +5 V. Wider common-mode ranges can be accommodated. See the AD7579/AD7580 data sheet for more details. The complete system operates from +12 V (+10%) and +5 V supplies. The analog input signals to the ADG507A contain information such as temperature, pressure, speed etc.

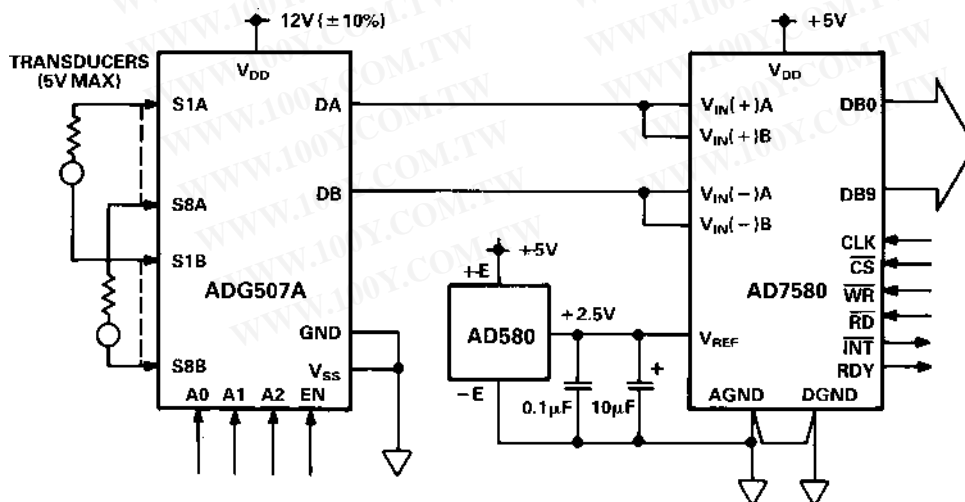


Figure 7. ADG507A in a Single Supply Automotive Data Acquisition Application

# ADG506A/ADG507A

## TERMINOLOGY

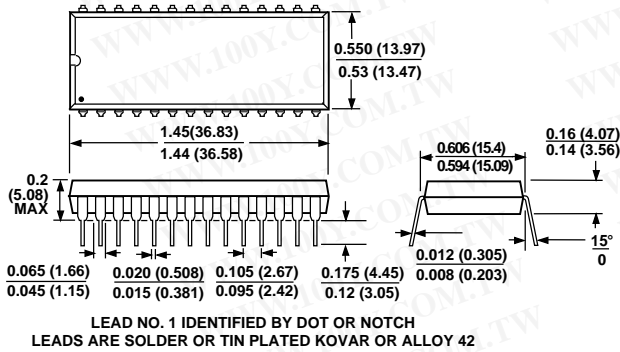
$R_{ON}$	Ohmic resistance between terminals D and S
$R_{ON\ Match}$	Difference between the $R_{ON}$ of any two channels
$R_{ON\ Drift}$	Change in $R_{ON}$ versus temperature
$I_S$ (OFF)	Source terminal leakage current when the switch is off
$I_D$ (OFF)	Drain terminal leakage current when the switch is off
$I_D$ (ON)	Leakage current that flows from the closed switch into the body
$V_S$ ( $V_D$ )	Analog voltage on terminal S or D
$C_S$ (OFF)	Channel input capacitance for "OFF" condition
$C_D$ (OFF)	Channel output capacitance for "OFF" condition
$C_{IN}$	Digital input capacitance
$t_{ON}$ (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition

$t_{OFF}$ (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
$t_{OPEN}$	"OFF" time measured between 50% points of both switches when switching from one address state to another
$V_{INL}$	Maximum input voltage for Logic "0"
$V_{INH}$	Minimum input voltage for Logic "1"
$I_{INL}$ ( $I_{INH}$ )	Input current of the digital input
$V_{DD}$	Most positive voltage supply
$V_{SS}$	Most negative voltage supply
$I_{DD}$	Positive supply current
$I_{SS}$	Negative supply current

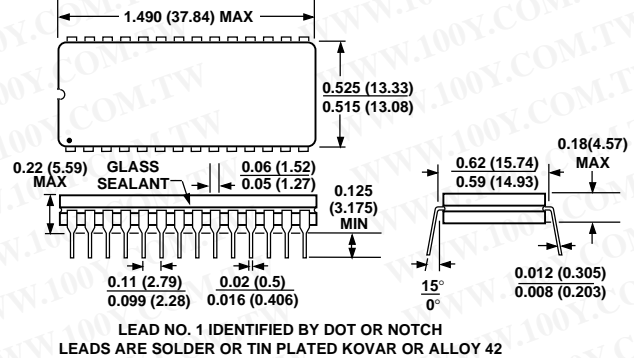
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

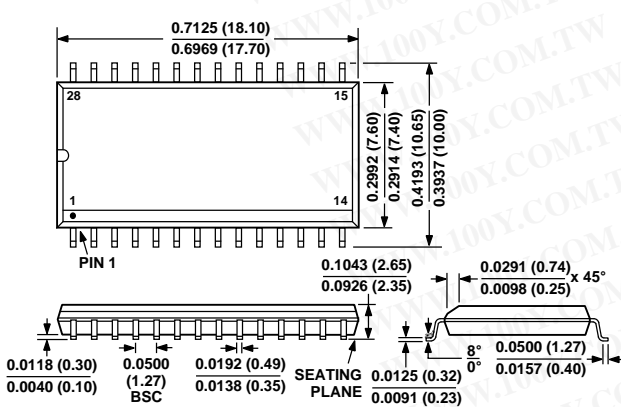
28-Lead Plastic DIP (Suffix N)



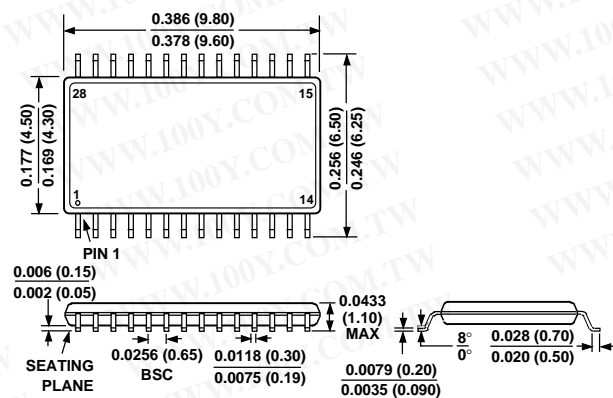
28-Lead Cerdip (Suffix Q)



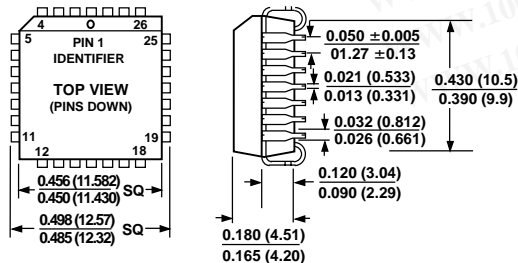
28-Lead SOIC (Suffix R)



28-Lead TSSOP (Suffix RU)



28-Terminal Plastic Leaded Chip Carrier (Suffix P)



28-Terminal Leadless Ceramic Chip Carrier (Suffix E)

